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A CONTRIBUTION TO THE CHARACTERIZATION OF RADIATION-INDUCED SOFT ERRORS IN SIGMA-DELTA MODULATORS AND SRAM MEMORIES

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Doctoral Programme of Electronic Engineering

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Daniel Malagón Periánez

Thesis Tutor: Sebastián Antonio Bota Ferragut

Thesis Tutor: Gabriel Torrens Caldentey

Doctor by the Universitat de les Illes Balears

This thesis has been written by Mr. Daniel Malagón Periánez under the supervision of Dr. Sebastián Antonio Bota Ferragut and of Dr. Gabriel Torrens Caldentey.

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Dr. Sebastián Antonio Bota Ferragut

Thesis director

Dr. Gabriel Torrens Caldentey

Thesis co-director

Daniel Malagón Periánez

PhD student

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“All our science, measured against reality,

is primitive and childlike - and yet it is

the most precious thing we have.”

Albert Einstein (1879-1955)

A mis padres, por ser el pilar fundamental de todo mi aprendizaje y por haberme transmitido los valores del conocimiento.

A mi hermano, por acompañarme siempre.

A Rocío por su paciencia y apoyo.

Resum

Aquesta tesi es centra en els anomenats Single-Event Effects (SEE) causats per la recol·lecció de càrrega degut a l'impacte d'una partícula energètica en un node d'un circuit microelectrònic.

En les últimes dècades la tecnologia microelectrónica ha experimentat un escalat constant permetent el disseny i implementació de sistemes més ràpids, més complexos i compactes. Aquest escalat ve acompanyat per la disminució de la tensió d'alimentació i la reducció de les mides dels transistors, fenòmens que tenen per efecte col·lateral un augment en la probabilitat de que una partícula ionitzant que interactua amb el substrat semiconductor puga generar la càrrega suficient per induir efectes transitoris que afectin el correcte funcionament del circuit electrònic i causar aquests SEEs. D'aquesta forma, els efectes de la radiació ionitzant ja no són un problema específic exclusivament relacionat amb aplicacions espacials o aviònica, convertint-se en una preocupació important per a la fiabilitat dels dispositius electrònics emergents.

Aquests SEEs es poden dividir en els anomenats Single-Event Upsets (SEU) si produeixen un canvi en l'estat lògic d'un element de memòria i els anomenats Signle-Event Transients (SET) si es genera una variació transitòria en el voltatge d'un o més nusos en un circuit combinacional. Ambdós SEEs es produeixen degut a la generació de parells electró-forat com a conseqüència de les interaccions de partícules amb la xarxa cristal·lina de silici que forma el susbstrat dels dispositius d'estat sòlid en els circuits integrats. Les partícules alfa, neutrons, protons, ions pesats i altres partícules ionitzants poden interactuar amb dispositius d'estat sòlid i afectar així el seu comportament. Aquest efecte sols es produeix quan la càrrega recol·lectada sobrepassa un determinat valor llindar (càrrega crítica), la qual depèn de la tecnologia de fabricació, del disseny a nivell de circuit, disposició dels components i de les característiques transitòries de la corrent induïda.

Aquesta tesi s'ha centrat en l'estudi dels SEUs en dos dissenys diferents de cel·les SRAM, ressaltant un estudi comparatiu entre les cel·les de mida mínima de sis transistors (6T) i de vuit transistors (8T). D'aquesta manera, el treball aquí presentat mostra els resultats de l'exposició de les SRAMs a diferents entorns operatius tals com una font alfa, una font de protons, una font de neutrons i un camp mixt d'alta energia, caracteritzat aquest últim per contindre espectres de partícules més energètiques, (fins als GeV) i un conjunt més ampli d'espècies de partícules (incloent pions carregats).

També s'estudia l'estabilitat dels convertidors analògic-digitals (A/D) per SET, utilitzant un disseny de modulador $\Sigma\Delta$ per a calcular si per a nivells raonables de càrrega induïda, la inestabilitat pot ser activada per SET.

Resumen

Esta tesis se centra en los llamados Single-Event Effects (SEE) causados por la generación de carga eléctrica debido al impacto de una partícula energética en un nodo de un circuito fabricado con tecnología microelectrónica.

En las últimas décadas la tecnología ha experimentado una evolución constante permitiendo el diseño e implementación de sistemas más rápidos, más complejos y compactos mediante el desarrollo de tecnologías microelectrónicas nanométricas. Este escalado viene acompañado con la reducción de la tensión de alimentación y de las medidas de los dispositivos, aspectos que tienen como efecto colateral un aumento en la probabilidad de que una partícula ionizante pueda generar la carga eléctrica suficiente para inducir efectos transitorios que afecten el correcto funcionamiento de circuitos electrónicos y causar estos SEEs. De esta manera, los efectos de la radiación ionizante ya no son un problema específico exclusivamente relacionado con aplicaciones espaciales o aviónica, convirtiéndose en una preocupación importante para la fiabilidad de los dispositivos electrónicos emergentes.

Estos SEEs se pueden dividir en los llamados Single-Event Upsets (SEU) si producen un cambio en el estado lógico de un elemento de memoria y los llamados Single-Event Transients (SET) si se genera un cambio transitorio en el voltaje en uno o más nudos de un circuito combinacional. Ambos SEEs se producen debido a la generación de pares electrón-hueco como consecuencia de las interacciones de partículas ionizantes con la red cristalina del silicio que forma el substrato de los dispositivos de estado sólido de los circuitos integrados. Las partículas alfa, neutrones, protones, iones pesados y otras partículas ionizantes pueden interactuar con dispositivos de estado sólido y afectar así su comportamiento. Este efecto sólo se produce cuando la carga recolectada en un nudo sobrepasa un determinado valor umbral (carga crítica), la cual depende de la tecnología de fabricación, del diseño a nivel de circuito, emplazamientto de sus dispositivos y de las características transitorias de la corriente inducida.

Esta tesis se ha centrado en el estudio de SEUs en dos diseños diferentes de celdas SRAM, resaltando un estudio comparativo entre las celdas de tamaño mínimo con seis transistores (6T) y con ocho transistores (8T). De esta manera, el trabajo aquí presentado muestra los resultados de la exposición de las SRAMs a diferentes entornos operativos tales como una fuente alfa, una fuente de protones, una fuente de neutrones y un campo mixto de alta energía, caracterizado este último por contener espectros de partículas más energéticas, (hasta los GeV) y un conjunto más amplio de especies de partículas (incluyendo piones cargados).

También se estudia los problemas de estabilidad de los convertidores analógicos a digitales (A / D) causados por eventos transitorios, usando un diseño de modulador ΣΔ para calcular si, para niveles razonables de carga inducida, la inestabilidad puede ser activada por un SET.

Abstract

This thesis focuses in the so-called Single-Event Effects (SEE) caused by the charge collection due to the impact of an energetic particle in a sensitive circuit node in microelectronic circuits.

In the last decades, electronic technology has experienced a constant evolution allowing the design and implementation of faster, more complex and more compact systems by the development of modern microelectronic nanometer technologies. This scaling entails the decrease of the supply voltage and transistor sizes, which has as a collateral effect: the increase of the probability of a particle to generate enough charge to induce transient effects in one or more circuit nodes affecting the proper operation of electronic circuits. In this way, ionizing radiation effects are not a specific problem exclusively related to the space or avionic applications anymore. In fact, they have become a major concern for reliability and dependability of emerging electronic devices.

These SEEs can be divided into: i) the so-called Single-Event Upsets (SEU), if there is a change in the logic state of a memory element, and ii) the so-called Single-Event Transients (SET), if a voltage transient in a combinational circuit is generated. Both SEEs are produced because the collection effects related to electron-hole pairs generated by particle interactions with silicon lattice that forms the substrate of the solid-state devices in integrated circuits. Alpha particles, neutrons, protons, heavy ions and other ionizing particles may interact with solid-state devices impacting their behavior. This effect only occurs when the collected charge surpasses a given threshold value (critical charge) that depends on the specific fabrication technology, circuit level design, layout, and induced current transient characteristics.

This thesis has focused on the study of SEUs on two differently-designed SRAM cells, proposing a comparative study between minimum-sized six transistors (6T) bit-cells, and eight transistors (8T) minimum-sized bit-cells. In this way, the work presented here shows results of SRAMs exposure to different operational environments such as an alpha source, a proton source, a neutron source, and a high-energy accelerator mixed-field. The latter is characterized by more energetic particle spectra (extending beyond the GeV range) and a broader set of particle species (including charged pions).

In addition, the instability effects in analog-to-digital (A/D) converters due to single effects has also been studied. The study has been performed using a design of a ΣΔ modulator to calculate if, for reasonable levels of induced charge, instability can be triggered by SET.

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Abbreviated terms

AP: Analog Selected Area Preparation System

BL: Bit-line (BL1 y BL2)

BPSG: Borophosphosilicate Glass

CERN: European Organization for Nuclear Research (Conseil Européen pour la Recherche Nucléaire)

CHARM: CERN High-energy Accelerator Radiation Mixed facility

CMOS: Complementary Metal-Oxide Semiconductor

DRAM: Dynamic Random Access Memory

FiT: Failure-in-Time

FPGA: Field-Programmable Gate Array

HEP: High Energy Physics

LET: Linear Energy Transfer

LHC: Large Hadron Collider

MBU: Multiple Bit Upset

MCU: Multiple Cell Upset

MOS: Metal Oxide Semiconductor

MOSFET: Metal-Oxide Semiconductor Field-Effect Transistor

OTA: Transconductance amplifier

PS: Proton Synchrotron

Q_c: Collected charge

Q_{crit}: Critical charge

RAM: Static Random Access Memory

RBL: Read Bit-line

RWL: Read Word-line

SE: Soft Error

SEB: Single Event Burnout

SEE: Single Event Effect

SEFI: Single Event Functional Interrupt

SEL: Single Event Latchup

SER: Soft Error Rate

SET: Single Event Transient

SEU: Single Event Effect

SOI: Silicon on Insulator

SRAM: Static Random Access Memory

TID: Total Ionizing Dose

WBL: Write bit-line

WL: Word-line

WWL: Write Word-line

ΣΔ: Sigma Delta

ΣΔM: Sigma Delta Modulator

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CHAPTER 1

INTRODUCTION

1.1 Context and overview

The purpose of this this work is to increase the existing knowledge on microelectronics behavior under radiation. In particular, it focuses in a type of effects known as Single Event Effects (SEE). SEE can be regarded as electrical noise induced by ionizing particles generated by radioactive isotopes present as impurities in the circuit package or in the materials used for device manufacture, or by high-energy particles present in the environment such as in space or in specific harsh locations like particle accelerators and nuclear power plants. The interaction between a single high energy particle and the silicon atoms of the crystalline substrate structure results in ionization phenomena that can alter the expected operation of a circuit.

In every technology generation, the size of the devices that form the integrated circuits (ICs) has been reduced to improve their performances and increase their density to reduce costs. Since the 70's to nowadays, the technology node has been scaled from 10 micrometers to about 10 nanometers, which means that the current technological manufacturing processes of ICs are in the nanometer region. As an example, with a 22 nanometer technology it is possible to place one thousand transistors in the area occupied by a transistor made with a 0.7 μm technology (Moore's Law). The supply voltage of the devices has also been reduced. However, because of the limitation imposed on the threshold voltage scaling to avoid an excessive increase of leakage current [YAM07], supply voltage scaling has been more moderated than the predictions of the International Technology Roadmap for Semiconductors (ITRS) [ITR00].

For these reasons, radiation has become not only a serious concern for circuits operating in harsh environments with a remarkable presence of high-energy particles such as modern accelerators for high energy physics experiments, nuclear power plants, avionics or outer space, but it also has become a reliability issue in critical applications operating at sea level environments [LER07, BAU05].

SEE are produced by different mechanisms [SCH04, TOR12]. The interaction of atmospheric neutrons with electronic devices has been identified as the major source of SEE in avionic applications, although at the outer layers of Earth's atmosphere, the circuits can be affected also

by other source of radiations like protons, pions or kaons [GAR14]. Finally, for most advanced technologies (deca-nanometers technologies) it has been clearly demonstrated that the impact of particles such as protons, pions or even muons [DIC83]-,[SIE11] can induce nuclear cascade showers on circuits, producing SEEs as a result.

At ground level or sea level, the neutron flux is approximately divided by a factor of 300 with respect to the flux at avionics altitudes; therefore, the main sources of SEE at sea level are alpha particles generated from traces of radioactive contaminants present in the materials used in CMOS technology [ZIE04],[AUT10]. ^{10}Boron, was commonly used in the microelectronics industries as dopant, or in borophosphosilicate glass (BPSG) layers, and it is known for its ability to interact with thermal neutrons and emit alpha particles. In this case, a reaction, $^{10}B(n,\alpha)^{7}Li$ occurs, and the energy deposited by the reaction products can induce an SEE [BAU95]. For this reason, BPSG is no longer used in recent technologies, even with low dopant levels [MAK07], this issue can suppose a significant contribution to the error rate in circuits working in environments having a high level of thermal neutrons.

The existence of so many sources of radiation and different interaction mechanisms with the circuit materials makes modeling the Soft Error Rate (SER) related to SEE a difficult task.

1.2 Motivation and objectives

Due to the microelectronic technology scaling, the electrical charge needed to disturb the operation of a single transistor, and therefore produce a fault in circuit operation, is expected to decrease [MAK07]. Furthermore, as the number of transistors in a circuit is also rising, the soft error rate caused by ionizing radiation tends to grow with the evolution of technology.

Analog and digital circuits obey different operating principles, for this reason it is interesting to analyze the effect of radiation on both analog and digital components. Specifically, we will focus on the analysis of the effect of radiation on SRAM memories integrated in a 65 nm CMOS technology, as an example of a digital component, and on Sigma Delta Modulators ($\Delta\Sigma$M), as an example of analog component.

SRAM (Static Random Access Memory) memories have been selected as the object of our study since they are widely used in state-of-the-art microprocessors and systems on chips, and present in other many applications including particle detectors used in high energy physics experiments, for example, SRAM memories are used as Radiation Sensors in the Large Hadron Collider (LHC) [DAN14].

The size of transistors in SRAM cells are one of the best examples of Moore's law, since the area occupied by each cell had been decreased from one generation to another, approaching the expected trend very closely. To satisfy the performance demand in current electronic systems, it is required in many cases to provide the systems with high capacity integrated SRAMs memories. As a consequence, the ratio of area dedicated to SRAM memory has increased. SRAMs are increasingly relevant in a growing number of safety-critical application fields, ranging from automotive to aerospace. Currently, SRAM memory in an integrated circuit can reach 50% [ZHU06] of the total area, and there are even forecasts indicating that in the coming years, this figure may reach 90% [PAV08]. A large amount of SRAM memory generally improves circuit performance, but also has an adverse impact on area, which is translated into a higher cost. For this reason, designers try to integrate the largest possible number of SRAM cells per unit area. This often leads to minimum-size cell designs to squeeze the full technology potential. SRAMs are usually designed with transistors close to the minimum size and the highest possible density. In addition, to reduce power consumption, it is interesting to use low voltages.

Analog-to-Digital (A/D) Converters are almost ubiquitous in modern SoCs. Since the outside world is, in essence, analog, they are used to make the translation to the digital processing world. This is true for consumer electronics but also for space applications. Any sensor acquisition chain, any scientific instrument requires at some point an A/D converter. Similarly, wireless transceivers also contain A/D converters to safely send data. In the field of instrumentation, one of the most relevant architecture is possibly the Sigma-Delta (ΣΔ) converter, despite being proposed for the first time in the early 1960s, its use has only been widespread in recent years, thanks to the advances in silicon-based technologies. It uses relatively low complexity analog hardware, which brings good technological scaling capabilities using standard CMOS technology. Power consumption can be much reduced since a large part of the processing is done by a digital filter.

The impact of SEE on SRAMs and ΣΔ Modulators were reported in [DAN14],[TUR96],[TUR12]. Both devices have different behaviors under radiation, and its analysis is hampered by the presence of several physical mechanisms by which SEE occurs, as will be described in the next section. Within this context, this thesis focuses on a type of radiation effect called “Single Event Upset” on SRAMs and "Single Event Transients" on ΣΔ, both are the result of the interaction of a single particle with the circuit and both are characterized by being non-desctructive. The interacting particle creates electron-hole pairs so that part of the electric charge can be collected by a sensitive node, affect the voltage, and generate errors in the circuit. In particular, in an SRAM, it can alter the content stored in one or more cells without damaging them so that they can be rewritten and operate normally. It is

reported [NIC11] that, in each technological generation, the error rate increases. This is due to the reduction of the transistors sizes, the decrease of the supply voltage, and the total memory area increment due to the increase in the number of cells. However, this trend is not so obvious considering the error rate in one individual cell. This is due to the fact that the reduction in the dimensions of a cell has two opposite effects. On the one hand, it decreases the amount of charge necessary to change the state of the cell and, on the other hand, it reduces the likelihood of interaction of a particle. In fact, there are studies that compare the susceptibility of cells from different technology nodes, which claim that a clear trend, especially if it comes from different manufacturers [TOR12] is not appreciated. The conclusion is that the difference in susceptibility between cells of different technology nodes is conditioned largely by other parameters that have to do with the specific characteristics of each manufacturing process, and even the particular memory design. In fact, authors state that there are significant differences even between SRAM memories of the same technology node but from different manufacturers.

In ΣΔ Modulators, the reduction of the dimensions of the transistors and the decrease of the supply voltage contributes to reducing the amount of electrical charge needed to generate noise in the electrical currents. This effect may trigger instability and lead to long-lasting conversion errors.

In this thesis we present a contribution to the study of these effects, on the one hand, we have performed, using electrical simulation, an analysis of the effect of the electrical disturbances produced by the radiation on the operation of a ΣΔ Modulator, and, on the other hand, the characterization of the behavior under radiation of two different SRAM architectures from experimental measurements performed under four different environments.

CHAPTER 2

INFLUENCE OF RADIATION ON ELECTRONIC DEVICES

Due to the continuous technological scaling, higher device densities, and lower voltages present in newer technologies, radiation effects on electronic devices will probably increase. This chapter describes the main interactions mechanisms of radiation with matter. It also covers some of the more common radiation effects in electronic devices.

2.1 Atmospheric environment

If we consider the region that stretches from sea level on Earth to the planetary space vicinity, it is possible to define three radiation environments: terrestrial radiation sources, atmospheric neutrons and muons, and radiation in Van Allen belts. There is an inner Van Allen belt about 100-1000km, which extends about 10000 km from sea level, and an outer belt from 15000 to 60000 km from Earth's surface, in whose region radiation levels are variable. The energy of the particles found in these regions ranges from 1 keV to 7 MeV for electrons and from 1 keV to 300 MeV for protons [VEL07]. Galactic Cosmic Rays (GCR), which can pass through the Van Allen belts, interact with the Earth's atmosphere creating showers of secondary particles. From these particles, neutrons and muons reach the surface in the largest proportion [NIC11].

In the past, at sea level or ground level the interaction of thermal neutrons with the BPSG in the package of the devices on integrated circuits, capable of generating alpha particles indirectly, (as even with very low energies) could cause errors due to the proximity of the source [YAN79] was considered the major responsible for SEE. With the suppression of BPSG layers in recent fabrication technologies, neutron induced SEUs in SRAM based systems are now mostly attributed to high-energy neutrons [GOR04].

Although recent studies show that muons are also capable of inducing SEUs through direct ionization [SIE10_b, SIE11], it is known that neutrons are the most important source of radiation [GAI11] that induce SEEs in the terrestrial context. Depending on the altitude and latitude, the neutron flux is different. Despite of that, its energy spectrum is considered

independent of altitude [NOR04]. It is known that neutrons cannot cause SEEs in integrated circuits directly, but they can generate secondary particles, which can cause SEEs.

The first failures due to radiation effects were found in space applications, since in the environment in which these systems operate, there is higher particle flux than at ground level. Although radiation-induced phenomena in electronic circuits were suggested for the first time in 1962 [WAL62], the first documented soft error in space (4 events in 17 years of satellite operation) was published in 1975 [BIN75]. In recent years, there has been an increasing interest in radiation induced effects at ground level and at avionics altitude. For this reason, this section introduces the main characteristics of the atmospheric spectra at different altitudes. Table I shows the main characteristics of the spectra of the atmosphere at different altitudes.

Table I. Nominal annual high-energy hadrons (HEH) for different atmospheric environments and the respective typical HEH percentage composition, R factor*, and hardness energies. Altitudes included for latitude and longitude of 46N° and 6E° (Geneva, Switzerland). (n_{int}=intermediate neutrons(300eV-1MeV)),source [GAR14]

Altitude	$\emptyset_{HEH}$ (/cm^2/yr)	Composition (%)				R	Hardness Energy(MeV)	
		n	p	$\pi^{\pm}$	n_{int}		$H_{50\%}$	$H_{10\%}$
375 m	~$1.7 \cdot 10^5$	93	7	0	21	0.12	100	380
10 km	~$1.7 \cdot 10^7$	82	18	0	18	0.08	130	920
20 km	~$3.8 \cdot 10^7$	68	38	0	14	0.06	200	$3.2 \cdot 10^3$

The hardness factors H50 and H10 quantifies the range of energies of high-energy hadrons in a radiation environment. To calculate these factors, it takes the simulated high energy hadron spectrum and makes the reverse integral, normalized to 1 at 20MeV. The values at 50% and 10% (H50 and H10) correspond to the proportion of the HEH fluence above this energy [THO16].

As it can be observed in Table I, the energy increases rapidly with altitude. At 20 km, the spectra are more energetic than in The Large Hadron Collider tunnel at CERN (Geneva, Switzerland). However, at ground and avionics levels, flux seem below those found in the critical accelerator zones [GAR14].

**R factor is the ratio between the equivalent thermal neutron flux and the HEH flux.*

In addition, neutron flux varies greatly with altitude [DOD03] and, although its energy spectrum is practically the same at a ground level than about 9km in altitude, the observed flux is about 400 times greater at these atmospheric levels [NOR04], see Fig 2.1.

This means that atmospheric and stratospheric radiation make the atmosphere a harsh environment which can be a problem for electronic devices.

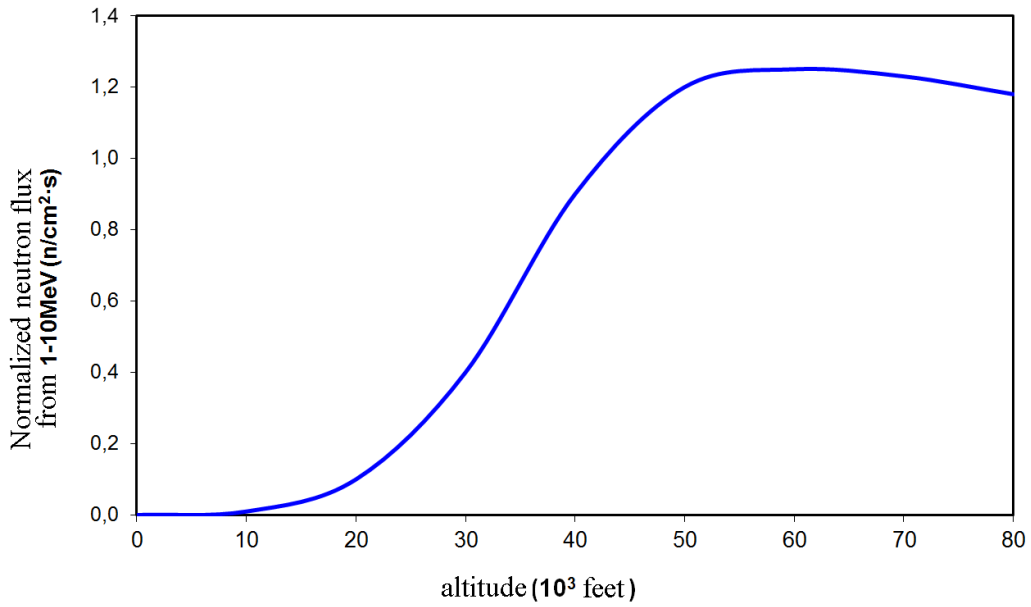


Figure 2. 1. Neutron flux as a function of altitude according to a model based on measurements of Boeing company (source [NOR93]).

2.2 Influence of radiation with matter

Different radiation sources and particles could produce effects when interacting with matter. Depending on the incoming particle, the energy, and the target material, the effects will be different.

Particles can be dived into two groups regarding its interaction with matter: charged particle and neutral particles. Charged particles are alpha particles, beta particles, heavy ions and protons. Neutral particles are neutrons and photons (gamma rays, X rays). The radiations effects vary depending on the type of particle: charged particles and neutral or non-charged particles. On one hand, charged particles as electrons (beta particles), protons, alphas, and fission fragment ions pass through the matter and cause direct ionization. On the other hand, neutral radiation as

photons (gamma and X rays), and neutrons cause ionization indirectly. Table II compares some radiations characteristics, including the particle charge and the ionization mechanism.

Table II: Comparison of Ionizing Radiation

Characteristic	Alpha (α)	Proton (p)	Beta (β) orElectron (e)	Photon (γ or X ray)	Neutron (n)
Symbol	${}^{4}_{2}\alpha \; or \; He^{2+}$	${}^{1}_{1}p \; or \; H^{1+}$	${}^{0}_{-1}e \; or \; \beta$	${}^{0}_{0}\gamma$	${}^{1}_{0}n$
Charge	+2	+1	-1	neutral	neutral
Ionization	Direct	Direct	Direct	Indirect	Indirect

It is also important to distinguish between ionizing and non-ionizing radiation, being ionizing radiations those which carry enough energy to break bonds between molecules and ionize atoms and therefore these are capable of removing electrons from atoms and converting them into charged particles (negatively charged electrons, and positively charged ions). The energy needed to produce this effect is typically about few eV, as for example in silicon, where the ionization energy is 3.6 eV [GAR14- GAR09]. The other kind of radiation, non-ionizing particles, are those which do not have enough energy to remove electrons from atoms.

For similar energies, heavier particles are slower, and they are stopped easier inside matter, so they deposit their entire energy over a shorter distance, see Figure 2.2.

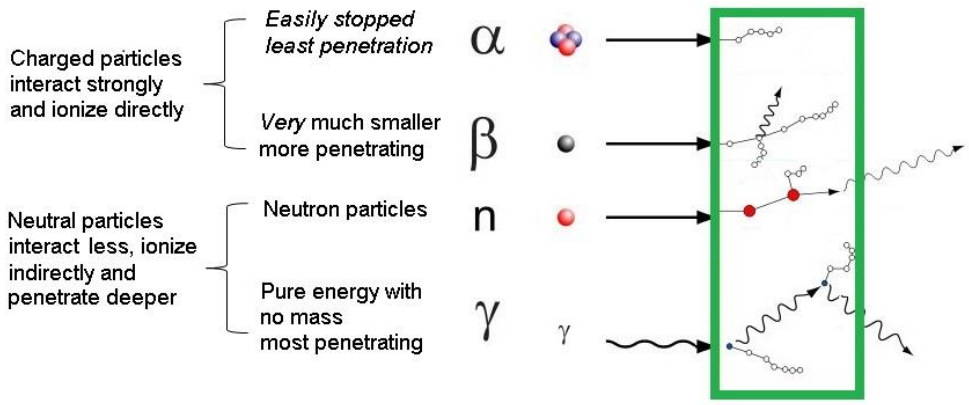


Figure 2. 2. Interaction of ionizing radiation with matter.

2.2.1 Interaction of charged particles with matter

Heavy charged particles (ion, proton or alpha particles) or light charged particles (beta particles) interact with matter through Coulomb forces. They lose energy hitting the material in each interaction, stopping after thousands of collisions [VEL11].

Charged particles interact with the nucleus of the target material and deflect them through elastic scattering, or fragment them through inelastic scattering. Secondary fragments created by interactions can be protons, neutrons or heavy particles, depending on the target material and energy from the beam particles.

An important parameter of the target material is the stopping power. We define it as the rate at which a charged particle moving through the material loses the energy. It is a measure of lost energy per unit of length traversed, so that, its units are MeV/cm. The total stopping power is the sum of the stopping power from nuclear interactions ($\boldsymbol{S_{nuc}}$) and Coulomb interactions ($\boldsymbol{S_{Col}}$), since both interactions can occur between charged particles and the matter.

$$\boldsymbol{S_{total} = S_{nuc} + S_{Col}} \qquad \textbf{2. 1}$$

$$\boldsymbol{S_{total} = -\frac{dE}{dx}} \qquad \textbf{2. 2}$$

When the particle passes through the matter it absorbs energy ($\boldsymbol{E}$), and the amount of energy that corresponds to Coulomb interactions is called Linear Energy Transfer (LET), so it is the stopping power of Coulomb interactions with an opposite sign [VEL11]. The LET makes reference to the charge deposition or the amount of energy transferred through ionization per unit length of distance through the target and usually is denoted respect to the density (ρ) of the traversed material, so it is given in MeV/mg/cm^2.

$$\boldsymbol{LET = \frac{1}{\rho}\frac{dE}{dx}} \qquad \textbf{2. 3}$$

where ρ is the material density, $\boldsymbol{\Delta E}$ the energy variation of the particle and $\boldsymbol{\Delta x}$ is the traversed distance inside the material. If $\boldsymbol{\Delta E}$ is higher than the critical energy $\boldsymbol{\Delta E_{crit}}$ (depends upon the material and means the minimal energy to create electron-hole pairs), a single event effect could occur.

The immunity of a device against SEEs depends on its $\boldsymbol{LET_{th}}$ (Linear Energy Transfer threshold). It is defined as the minimum LET capable of causing a SEE in a particle flux of 10^7ions / cm2. The $\boldsymbol{LET_{th}}$ is usually smaller as the device accumulates Total Ionizing Dose (TID).

An initial approach to compute this parameter consists in considering the device as a simple capacitor with capacitance $\boldsymbol{C}$ in which a particle deposits a charge $\boldsymbol{Q}$ capable of inducing changes in the voltage, then an SEU will occur when LET>$\boldsymbol{Q_{crit,}}$ .Considering $\boldsymbol{LET_{th}}$ as the necessary LET to produce a voltage increase (ΔV) high enough to produce a SEU:

$$\boldsymbol{LET_{th}} \propto \Delta \boldsymbol{V} = \frac{\boldsymbol{Q}}{\boldsymbol{C}} \qquad \textbf{2. 4}$$

As the size of these devices decreases, so does their capacity, and the charge necessary to induce an SEU is lower. Although the width and length of the devices have decreased, the depth of the devices normally remains constant, so this approach is close to reality.

2.2.2 Interaction of neutral particles with matter

2.2.2.1 Photons interaction with matter

Photons, include gamma rays (γ), ultra-violet rays (UV), X-rays, etc., all of them transport electromagnetic radiation at the speed of light and have no mass or charge. The effects caused by this kind of radiation can be photo electric absorption, pair production or Compton scattering.

- Photo electric absorption: Photon is absorbed by an atom, and it emits an energetic photo-electron.
- Compton scattering: Photon interacts with an electron in the material losing energy and glance off with a different wavelength.
- Pair production: Photon is absorbed, and his energy is used to create an electron-positron pair.

2.2.2.2 Neutrons interaction with matter

Neutrons are considered heavy particles that interact with matter through collisions with nuclei only through the strong nuclear force. The effects in matter can be:

- A capture process: absorption of the neutron and creation of one or more heavy charged particles.
- Clashing with other particles: scattering of the neutron which interacts with the nucleus, but both particles survive to the reaction and reappear with different directions and energies.

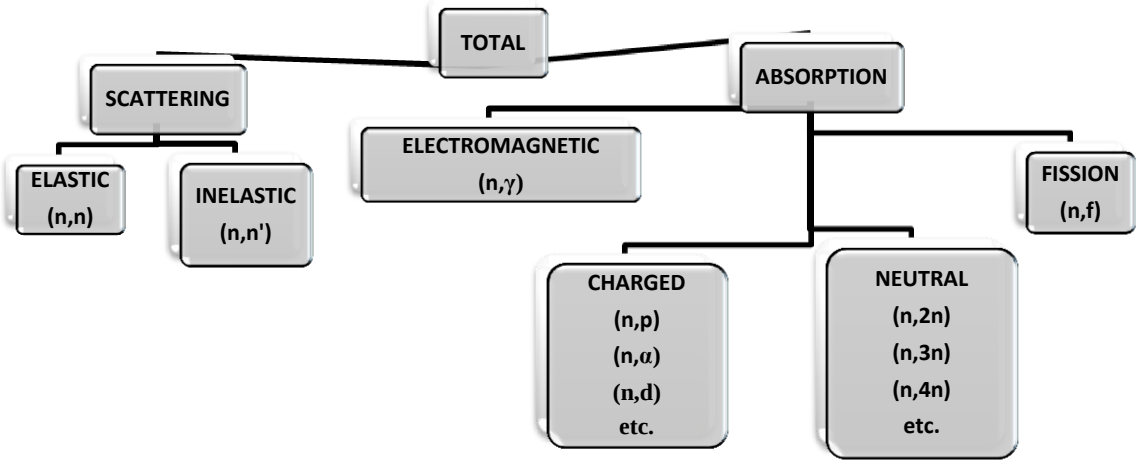


Figure 2. 3. Different neutron interactions. The parentheses show the incoming and outgoing particle [RIN91].

The probability that a reaction occurs depends on the cross section, **σ**, which is referred to as the sensitivity of a device for particles of a certain energy in which SEEs can be found [VEL11] and represents the probability for an event to occur on the sensitive area of the device.The cross section depends on the energy from the neutron and the atomic number of the target nucleus.

In cosmic rays, there are neutrons of different energies. For our purpose, and depending upon the energy, they will be classified into epithermal neutrons, fast neutrons, and ultra-fast neutrons. An epithermal neutron will be a neutron with a kinetic energy of below 1 MeV. Fast neutrons will be neutrons with energy above 1MeV, and below 20 MeV and ultra-fast neutrons will be neutrons with energy greater than 20 MeV. The small kinetic energy of epithermal neutrons makes them exchange energy through elastic scattering with the nucleus, in addition, epithermal neutrons will sometimes get absorbed. Fast and ultra-fast neutrons have greater energy and deposit more energy when interacting with the nucleus.

2.3 Radiation effects on CMOS devices

Soft errors induced by radiation are an increasingly important threat on integrated circuits (ICs) manufactured in advanced CMOS technologies [GAI11]. If an extensive explanation of complex theoretical performance of electrical conductivity in crystalline solids with which modern technologies are manufactured is wanted, the use of tools such as quantum mechanics is needed; however, until today it has been enough the use of classical models of electron wave packets with effective mass and speed, derived or arising from their interaction with the crystal lattice.

To understand what happens in electronic devices exposed to radiation it is important to know not only what kind of devices we are dealing with, but also the technology used. We will focus in the dominant effects in transistors of Complementary Metal Oxide Semiconductor technology devices (CMOS technology), since bipolar devices are not present in the devices used in this work. This technology combines two kind of transistors on the same substrate, and it is nowadays one of the most frequently used logic families.

In these transistors, the semiconductor is modified adding atoms with different valence electrons giving n-doped or p-doped semiconductor, which form NMOS or PMOS devices. Any logic gates can be created in a CMOS technology. A basic two-stage CMOS operational amplifier configuration is showed in Figure 2. 4(a) and an SRAM cell with this technology is shown in Figure 2. 4(b).

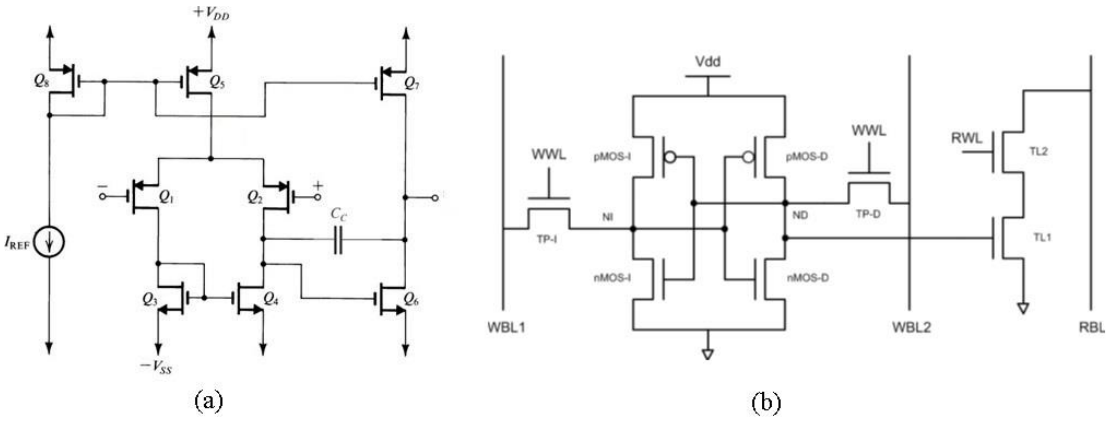


Figure 2. 4. (a) Two stage CMOS op-ampl. (b) Eight transistor CMOS implementation of an SRAM cell.

Although radiation exerts a faint influence in accumulative effects as displacement damage on MOS transistors, these devices are profoundly amenable to ionizing effects. The ionizing radiation effects described in section 2.2 are responsible for adding charge in CMOS nodes [MAK07]. Thus, ionization can change a few important electronic parameters of MOS transistors, as the threshold voltage V_t or the leakage current.

When a particle strikes an electronic device, depending upon the charge of the particle and its mass, it can generate directly or indirectly (through other particles) a track of positively and negatively charged ions.

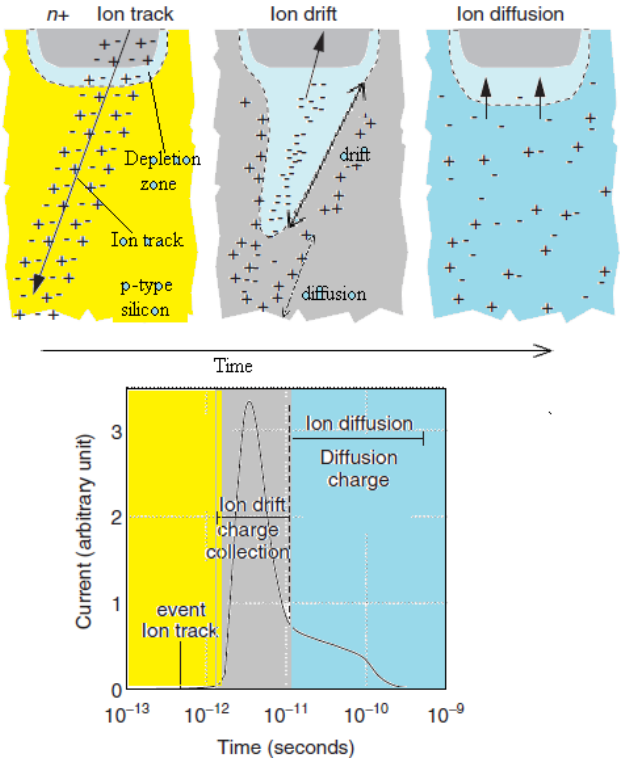


Figure 2. 5. Charge collection and current induced in a silicon junction after an ion strike.

In the semiconductor, this ionization event creates a charged track that will consist of mobile electrons and holes, as shown in Figure 2. 5 (top).

If enough energy is delivered in a particle collision, and this energy is deposited near the sensitive node of a CMOS device (e.g. drain of a MOS transistor), a spike of the drain current could be observed, see Figure 2. 5 (down), and the device will be affected by SEE.

It is called critical charge $\boldsymbol{Q_{crit}}$ to the minimal charge necessary to create SEE. This parameter describes the sensitivity of memory circuits to transient effects.

In devices, the critical charge $\boldsymbol{Q_{crit}}$ is defined as the minimum charge to change from a "1" to "0" or vice versa. $\boldsymbol{Q_{crit}}$ can also be defined as the difference between the stored charge in the node and the minimum charge which is required to read correctly the data [PIC78].

Consider a square device with dimensions of L×L, the critical charge, $\boldsymbol{Q_{crit}}$, is proportional to the surface of this square.

$$\boldsymbol{Q_{crit} \propto L^2} \qquad \textbf{2. 5}$$

In an SRAM, the critical charge needed to generate pairs and create a bit-flip depends on the size of the critical node, the voltage on the cell and the feedback time on the cell. According to Roche et al. [ROC99], the simple model first proposed is:

$$Q_{crit} = C_N VDD + I_{DP} T_F \quad \textbf{2. 6}$$

where C_N is the node capacitance, VDD is the supply voltage, I_{DP} is the max PMOS drain conduction current and T_F is the flipping time of the cell. This equation shows that if the voltages of the devices are lower, the deposited charge needed to generate SEE is lower, increasing SEU susceptibility.

Different effects on CMOS technologies are considered in the next section.

2.4 Radiation effects classification

Both charged particles and non-charged particles interact with matter and can produce undesired effects in semiconductor devices. These can be very different, from displacement of atoms in the structure to the corruption of the stored data on the devices due to charge injection. We will classify the type of radiation-induced effects into two categories: Cumulative effects and Single Event Effects (SEE).

2.4.1 Cumulative effects

They are potentially destructive effects, which have been caused by accumulated dose over time.

2.4.1.1 Displacement damage (DD): It is the result of nuclear reactions, normally scattering, that cause changes in the semiconductor lattice changing the crystal electrical characteristics. It is normally measured in neutrons/cm^2, according to ASTM (the international standards organisation) standards, which assume that these effects are proportional to 1 MeV equivalent neutron fluence [VAY10,GAR14]. So, units are the same as for the neutron fluence. This is related to the non-ionizing energy loss of the particles in materials, leading to the displacement of its atoms and potentially limiting its performance.

2.4.1.2 Total Ionizing Dose (TID): It is the dose accumulated by the device due to ionizing radiation over time and, in radiation environments, it is related to the ionization of the radiation field particles, and the trapped charge generated by radiation in the oxides of the components [GAR14]. This kind of effects can cause the degradation in MOS devices. It is measured in Grays (Gy, 1 Gy=1 J/kg), although rad is commonly used also as unit of absorbed radiation dose, defined as 1 rad = 0.01 Gy.

2.4.2 Single Event Effects (SEEs)

This kind of radiation effect groups all effects caused by the interaction of a single particle with the component's sensitive region.

Single event effects are usually measured and classified by the parameter called "cross section", analogous to the nuclear cross section "σ" and it is measured in cm^2. Cross section per bit is usually used in SRAM memories, to obtain a parameter than do not depends on the memory capacity of the SRAM, and the number of SEUs found in the memory.

$$\sigma = \frac{Nº\ of\ SEE}{\emptyset} \qquad \textbf{2. 7}$$

$$\sigma_{SRAM} = \frac{Nº\ of\ SEU}{K*\emptyset} \qquad \textbf{2. 8}$$

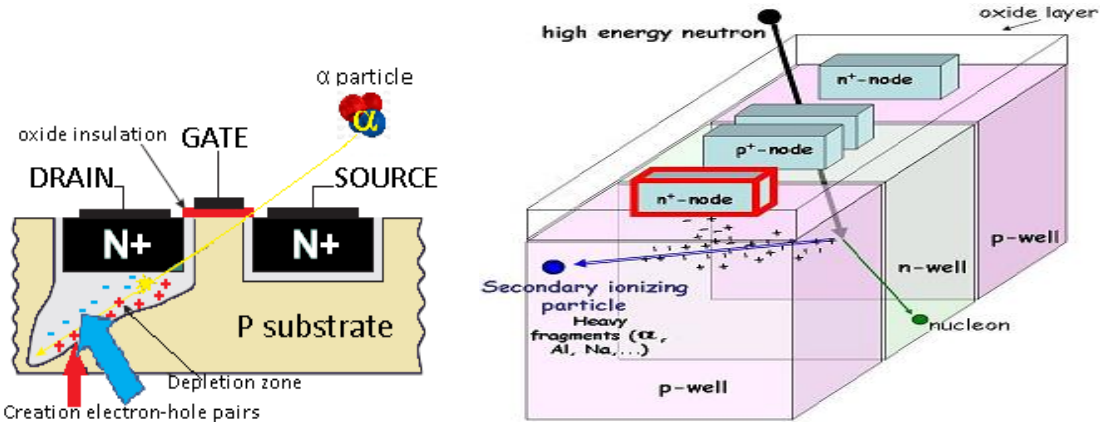
where σ is the cross section, K is the size of the SRAM memory in bits, and Ø is the fluence (particles/cm^2) which is the integrated flux (particles/cm^2·s).

These are classified into Soft errors, which are effects that cause some form of corruption of a stored element as an SRAM device, and they are nondestructive and can be corrected rewriting, restarting, resetting or power cycling the device.

By contrast, single event effects are classified as hard errors are destructive errors that are impossible to recoverable.

2.4.2.1 Soft Errors or non-destructive SEEs

2.4.2.1.1 Single Event Upsets (SEUs): This kind of errors produces a single bit flip induced either by direct ionization (from a traversing particle) or by a recoiling nucleus emitted from a nuclear reaction. It is a change of state of a storage cell (e.g. from 0 →1 in SRAMs) induced directly by a particle with enough energy to generate charge and ionize (like alphas particles) the sensitive volume of the electronic device (Figure 2. 6-a), or indirectly (like neutrons) through the secondary particles produced by elastic or inelastic collision with the matter nuclei (Figure 2. 6-b). SEUs affects both bipolar and MOS technologies.



a) b)

Figure 2. 6. SEU generated in a CMOS structure a) which is affected by an alpha particle (direct ionization). b) (SRAM) which is affected by a high-energy neutron (indirect ionize).

2.4.2.1.2 Multi-Cell Upset (MCU) and Multi-Bit Upset (MBU): MCUs occur when two or more bits (physically adjacent or not) become corrupted by a single particle. Otherwise, if two or more bits become corrupted by the same event, and they are in the same logical word, the effect is called Multiple Bit Upset (MBU).

2.4.2.1.3 Single Event Transient (SET): This kind of error produces a momentary voltage spike at a node in semiconductors produced by the electric field separation of the charge induced by an ion passing through or close to a circuit junction. The noise or perturbation is very short, hence they are called transients, but depending on when or where it occurs, it could propagate through the whole system. This kind of errors could be produced in a digital device or in an analog device, like Sigma Delta Modulators as it will be seen in chapter 4, and bring the

disturbance to the output signal. SET is a crucial problem for modern technologies as the transistor dimensions and critical charges to generate SEEs have been decreased.

2.4.2.1.4 Single Event Functional Interrupt (SEFI): caused by nuclear interaction of a single ion strike that causes the interruption of the affected device normal operation. They are a subgroup of SEU effects related to high-density programmable devices.

2.4.2.2 Hard errors or destructive SEEs

2.4.2.2.1 Single Event Latchup (SEL): Sometimes it is possible to classify this kind of effects as nondestructive. However, they are potentially destructive events which can affect CMOS-based devices. A SEL occurs when the charge generated by the ionizing particle activates a parasitic bipolar transistors formed between the substrate and doped regions of the transistors and forming an open path between supply and ground causing a short circuit. When a latch up occurs, the current increases and if the power supply is maintained, the device can be destroyed by thermal effects.

2.4.2.2.2 Single Event Gate Rupture (SEGR): it refers to a dielectric breakdown and the formation of a conducting path in the gate oxide due to a high field generated by high current. The charges created by an energetic particle crossing the semiconductor are collected and propagate up to the insulator interface, making the electric field across the dielectric exceeds a critical value. SEGR can be found in nonvolatile memories like EEPROMs, during the write or erase when the voltage is applied to the transistor's gates. It is impossible to avoid an SEGR becoming destructive.

2.4.2.2.3 Single Event Burnout (SEB): destructive triggering of a vertical n-channel transistor accompanied by a regenerative feedback. This occurs in power MOSFETs biased in the OFF state (i.e., blocking a high drain-source voltage) when a heavy ion passing through it deposits enough charge to turn the device on.

2.4.2.2.4 Single Event Snapback (SES): This kind of error produces a similar effect that SEL, affecting mainly to NMOS transistor. It occurs when a high-LET

particle strongly ionizes the MOS structure and turn on the inherent parasitic bipolar transistor. Unlike SEL, in this case, the circuit could recover its operation and it is not necessary the reduction of main supply voltage. It could be done by sequencing electric signals. It is known that SES is destructive if the local current density is high enough to cause critical overheating [KOG89].

Single event effects that produce an error in the operation of the circuit and that corrupt the data but do not permanently damage it, are generically called *soft errors* (SE), and it is possible to recover the circuit and resume normal operation after a soft error.

This work focuses solely on SEE and more specifically on SEUs in SRAMs, and SETs in analog devices as ΔΣM.

2.5 Radiation mitigation techniques

There are several techniques that can be applied to mitigate SEUs or designing "radiation-hard" integrated circuits. Some of these techniques are stemmed from applications in the aerospace and nuclear industries. The techniques to mitigate SEUs aim to reduce SER to meet the specifications that are required in the circuit for a given application. The component or system designed to be used in radiation sensitive devices, and which can tolerate radiation-induced errors, will be called "radiation tolerant". Tolerance requirements for soft errors are often given in terms of Failure-in-Time (FiT) [NIC05], defined as the number of failures per billion (10^9) hours of the circuit operation.

The radiation resistance of a device depends, among others, on the materials or design used to manufacture the electronic components. The present chapter focuses in some of the radiation hardening techniques used to mitigate errors.

There are two main groups of radiation mitigation techniques used in the fabrication process of an IC, Radiation Hardening By Process (RHBP), and Radiation Hardening By Design (RHBD).

2.5.1 Radiation Hardening by Process (RHBP)

Hardening by Process is based on the modification of doping procedures, the use of special materials, or the use of special processing steps to minimize the effects of radiation on

performance. Dopant concentration has increased with technology scaling to maintain relatively high values of threshold voltage, as a consequence, higher levels of trapped charge in the oxide are required to influence the electric field in the transistors [ALL12]. In addition, the smaller minimum feature size present in each standard CMOS technology process could reduce the cross-section for SEUs.

2.5.1.1 Epitaxial layers: it is a lightly doped layer structure grown on the highly doped substrate [DOD94_b]. The lower substrate resistance reduces the formation of PNPN paths and therefore, the risk of SEL.

2.5.1.2 Silicon on insulator (SOI): SOI technology consists essentially in separating the active part of the circuit from the silicon bulk by an oxide which may be a buried oxide (BOX), over the silicon substrate [SCH032]. The mechanism that gives SOI technology a higher robustness to radiation is based on the fact that the volume in which the charge collected can be deposited by the energetic particles is much smaller than in a conventional technology [FER06].

In Figure 2. 7, a comparison between the SER of a SOI technology and the SER of a conventional one is shown.

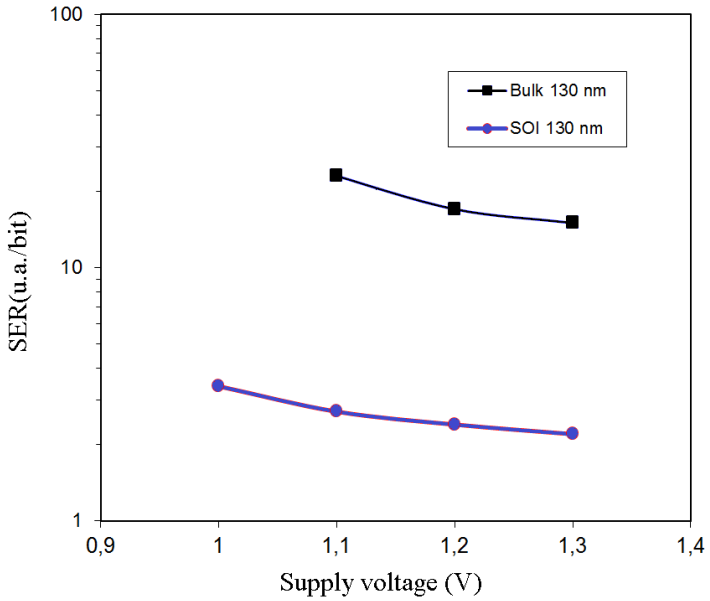


Figure 2. 7. Comparison between the SER of a SOI technology with a conventional one (source [ROC03]).

2.5.2 Radiation Hardening By Design (RHBD)

RHBD includes some of the most common and effective techniques in standard manufactured processes of Application Specific Integrated Circuits (ASICs) aimed at limiting the negative consequences of radiation on leakage current, voltage threshold and SEEs [BRA16].

2.5.2.1 Triple wells: the main advantage of triple wells is the possibility to bias the well potential to a different voltage with respect to the bulk substrate. In the triple well process, assuming a p-type substrate, the PMOS transistors are built in an n-well, however, the p-well of the NMOS devices is constructed within a deep n-well. So, both device types are isolated from the substrate by a reversed biased junction. Triple wells reduce the SER sensitivity as the electrons generated deep inside the substrate are more efficiently collected by the extended n buried zone and then better evacuated through n-well binds. This is typically exploited by biasing the body of the NMOS to the same voltage of the source and avoiding the body-effect in the piled transistors used in analogue circuits. Triple wells have shown to reduce alpha-particle and neutron-induced soft error rate cross-sections in 130 nm and 90 nm SRAMs and latches. However, the same argument calling for good contacting of the substrate applies to the buried n-well and care must be taken in reducing the resistance by frequent well contacts [ALL12].

2.5.2.2 Enclosed Layout Transistor (ELT): The Enclosed Layout Transistor is the most effective technique to avoid or reduce the parasitic conduction channel induced by TID and has been extensively used in High Energy Physics (HEP) applications [ANE96]. In ELT the drain is placed inside the gate, and any leakage current must flow through the gate, rather than along the oxide because special layout style with an inner diffusion surrounded by the transistor gate and an outer diffusion, see Figure 2.8.

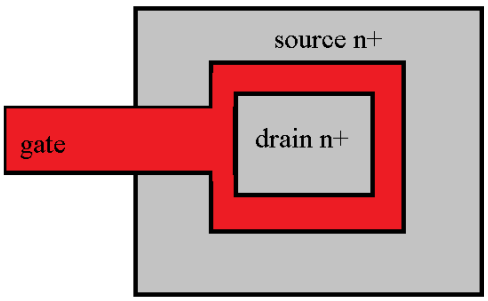


Figure 2.8. Layout of ELT

2.5.2.3 Guard rings: also called guard bands, are effective with many radiation effects and consist, in CMOS technology, in surrounding n-channel devices with a p+ guard ring and p-channel devices with an n+ guard ring, requiring only an increase in area (Figure 2. 9). Ref [FAC10] shows how even partial guard rings are effective in reducing the leakage current between diffusions belonging to adjacent transistors almost by two orders of magnitude.

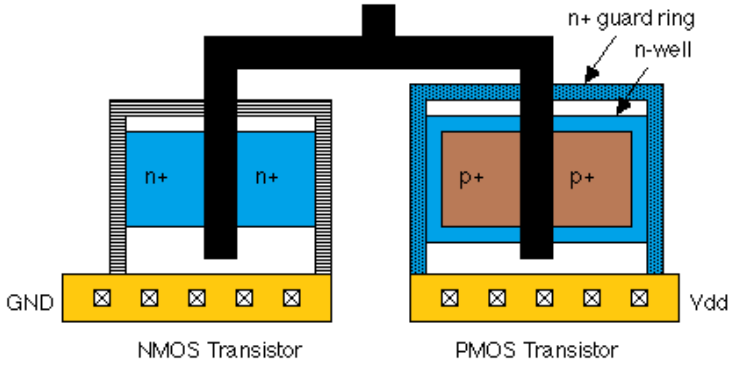


Figure 2. 9. CMOS transistors with guard rings

2.5.2.4 N-well contacts: In a pMOS device, n-wells and additional contacts can limit the called parasitic bipolar amplification effect, in which the ionization electrons in the well temporarily distort the electric field and activate the parasitic bipolar by forward biasing the source-body junction injecting additional electrons in the cell, and change the duration of SET pulses generated [BRA16].

2.5.2.5 Shortening the SET duration: This technique consists in limiting the speed of a circuit by adding capacitance or resistance, which is equivalent to reject long pulses, because when the length of a transient is too short and the electronic component or the memory element does not have time to respond to a SET; it is equivalent to a glitch and will not propagate.

2.5.2.6 Spatial redundancy: in this case, the data or information is stored at different locations so that an error affects only one node and the upset will not be able to propagate. Several memory elements with multiple storage nodes have been developed. This technique is considered a passive technique because it does not detect failures, but the failures are masked.

An example is Triplication, or Triple Mode Redundancy (TMR), which consists of three elements processing the same information, and an arbitration circuit output, typically a majority output [BON11]. TMR can also be used in more complex circuits or functional blocks, and can be combined using special layout techniques and temporal redundancy [BRA16].

2.5.2.7 Temporal redundancy: to use these techniques, extra hardware elements are required to store delayed versions of the input at a different time Δt respect to the input stored at time t. With three flip-flops, see Figure 2. 10, only one pulse shorter than Δt will present a wrong value, and the correct value will be shown at the output of the voter.

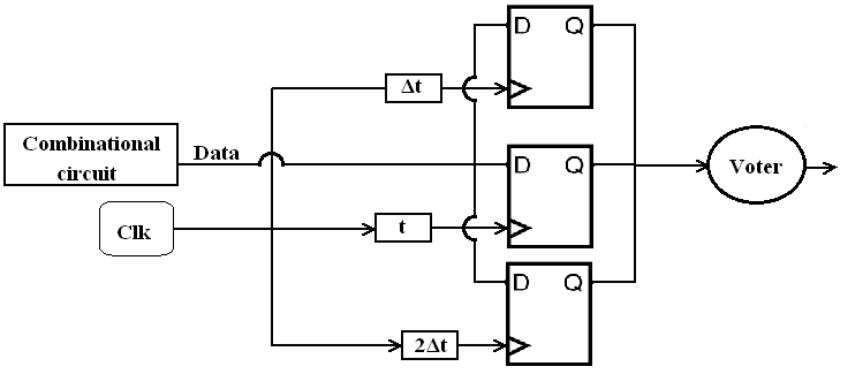


Figure 2. 10. Temporal redundancy storing data at delayed versions of the input.

Another way to do that is to repeat the measurement at different times and compare the results (see Figure 2. 11) so that if the values stored at different times do not match, then there is a failure. Both ways mean an increase in the propagation time for the logic and limit the maximum frequency achievable.

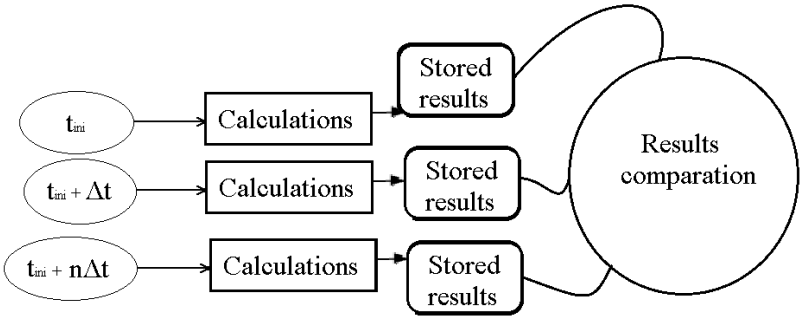


Figure 2. 11. Temporal redundancy computing data at different times.

2.5.2.8 Encoding: This is called also information redundancy, and consists in adding redundant information using Error Detection Codes (EDC) or Error Correction Codes (ECCs) [NIR96]. One of the most used ECCs is the Hamming Encoding (HE), based on the Hamming distance which is the number of different bits between two data strings with the same length. For single-bit correction of an m-bit data packet, using HE k additional parity bits are required [RAB02], so that:

$$2^k \geq m + k + 1 \qquad \textbf{2. 9}$$

Thus, single-bit error correction requires $\log_2 m + 1$ additional bits, in this way, for longer data packets, the relative overhead decreases substantially [BRA16].

2.6 Simulations techniques

Radiation robustness is hard to predict, as its value depends on many factors like the source and type of particle under consideration. Despite of that, simulation represents the first and early analysis in an assessment of the sensitivity to faults of a device or component. For those reasons, simulations must be often complemented by experimental results. It is appropriate to simulate how particles interact with electronic device materials taking into account the structure size, the structure material, the critical energy and the sensitive volume in the circuit under test.

This section presents the description of current pulses for circuit simulation, which are used to determine the magnitude of critical charge in an electric simulation as in the ΣΔ case.

Also, this section shows on the simulation tools used to extract information about the radiation environment, which is as similar as possible to test environments and will be discussed in chapter 3. Device response is covered in chapter 5.

2.6.1 Electric simulation

An approach to obtain the critical charge consists in using a circuit simulator and consider the charge collected at sensitive nodes and compute the minimum charge needed to upset the behaviour of the system under study.

The radiation effects on the circuit nodes affected by the radiative interaction are typically described by the collected charge Q_{ncoll} at the sensitive node n. This charge deposition is usually modelled by a double exponential current generator of short duration.

The double exponential current generator is directly applied at the node, see Figure 2. 12.

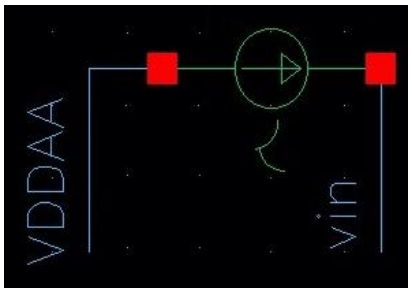


Figure 2. 12. An example of the double exponential source used to simulate SEEs in CADENCE/VIRTUOSO.

$$I_{exp} = \frac{Q_{ncoll}}{\tau_f - \tau_i} \times \left(e^{-\frac{t}{\tau_f}} - e^{-\frac{t}{\tau_i}} \right) \qquad \textbf{2. 10}$$

where τ_i is the rise time or the time taken by a signal to change from a specified low value to a specified high value and τ_f is the fall time or the time taken for the amplitude of the pulse to decrease from the peak value to the minimal specified value. For these double exponential pulses, a tenfold ratio between the rise and the fall time constants (10ps and 100ps respectively) [MAV07] is usually considered see Figure 2. 13.

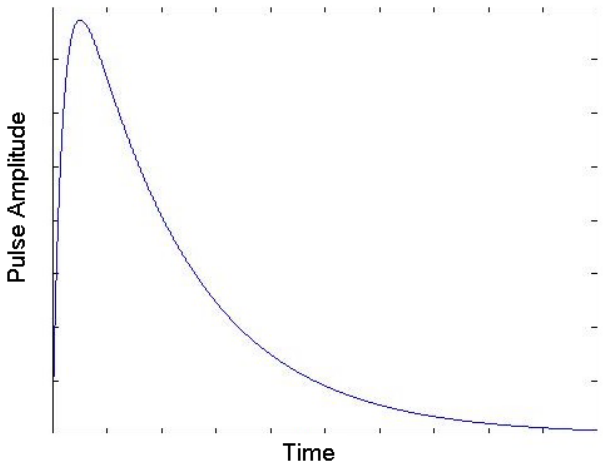


Figure 2. 13. Double exponential pulse shape.

The capacity at a sensitive node is related to the technology. In this thesis, where CMOS technologies are used, the critical charge in the ΣΔs is between 300fC-1pC, which is quite different to the SRAMs, where usually it is between 1-2 fC. Other studies report a critical charge about 20-30 fC in DRAM or SDRAM [NIC11].

Models in which this double exponential is introduced consider these effects similar to the effects of the ionization track on devices due to radiation particle interactions.

This approach will be shown throughout the chapter 4 to simulate the behaviour of a ΣΔ Modulator which is supposed impacted by radiation at different nodes.

2.6.2 CRÈME and MULASSIS approach

To investigate the direct ionization and nuclear reaction events occurring in both cell types in the sensitive volume of SRAMs, different simulation tools will be used: CRÈME Monte Carlo online tool [CRE96], which uses phenomenological models to predict SEE rates and it is developed between NASA, Vanderbilt University School of Engineering [MEN12,TYL97,WEL10], and the multi-layered shielding simulation software tool (MULASSIS) developed as part of the European Space Agency (ESA) activities in the Geant4 collaboration [LEI02]. Both tools allow a simplified manner of visualizing the potential impact of a radiation type, in terms of SEE induction.

CRÈME MC was used in the case of alpha or proton beams, as the CRÈME MC tool does not provide information in the case of indirect ionization such as neutron beams. To simulate neutron interactions it was used Geant4 toolkit and MULASSIS and also CRÈME MC to simulate the secondary particle effects, as electrons or protons generated.

2.6.3 Sensitive volume

When a charged particle hits crystalline silicon, it generates charge in the form of electron-hole pairs that may be collected by drift and diffusion and transported to circuit nodes, generating a current pulse that modifies the voltage of the affected node. This is the mechanism by which SEUs are produced. If the deposited charge is large enough to change the logic-stored value in an SRAM cell (critical charge), an SEU is produced. This critical charge or bit-cell sensitivity to

radiation depends on many factors as technology node, supply voltage, temperature, and characteristics of the incident radiation [REI04], and on the specific shape of the current pulse generated by the collection of charge at the sensitive node [JAI07]. To estimate the possibility of producing SEUs, it is necessary to know how much charge could be collected by the incident radiation on the device. The charge collected at circuit node *j* is the sum the energy deposited in N*j* sensitive volumes scaled by a weight $\alpha_{j,i}$ for ($0 \leq i < N_j$) and the mean ionization potential, I(*Z*) of the material (3.6 eV/ehp in silicon) [SIE10].

$$\boldsymbol{Q_{coll,j} = \sum_{i=1}^{N_j} \alpha_{j,i} \times I(Z) \times E_{dep,j,i}} \qquad \textbf{2. 11}$$

The collected charge depends on the energy deposited by the particles or ionizing radiation, so this deposited energy will be taken into account to estimate the possibility of generating a charge collection, which exceeds that critical charge capable of generating SEUs.

The sensitive volumes were chosen to emulate the region in the chip in which energy deposition from an ionizing particle can affect the operation of a device such as 6T SRAM and the 8T SRAM. It is important to note that, in the case of total ionizing dose, the volume should be associated with an insulating layer in the structure [SIE10].

The collected charge by particles is calculated as shown in equation 12 [WAR05]. The path length in the volume is called ***l*** and LET, in units of MeV-cm /mg, is the Linear Energy Transfer or stopping power in the target material. Equation 12 assumes a constant LET through the sensitive volume, which is valid for all primary ions used in this chapter, as alphas or protons.

$$\boldsymbol{Q_{coll}(pC) = 0.01035 \cdot LET \cdot l(\mu m)} \qquad \textbf{2. 12}$$

It is important to note that the critical charge in the typology of cells that integrate the SRAMs used is $\mathbf{Q}_{crit}$ = 1.72 fC [TOR12].

The sensitive volume (SV) geometry was supposed as a Rectangular Parallelepiped (RPP) where the sensitive area in the 6T and the 8T cell areas are assumed as 1.01 μm^2 and 1.39 μm^2 respectively. It has to be taken into account that these are 16 kb memories or 16384 bits. The total sensitive areas in the DUT are 16548 μm^2 and 22774 μm^2 for the 6T SRAM and 8T SRAM respectively, see Figure 2. 14. It was taken into account the dimensions of each memory bank without including the control unit in each bank.

For single event effects, the sensitive volume is often associated with the depletion region [SIE10], for this reason, it was chosen the interface with SiO_2 and silicon in the last layer on the chip, see Figure 2. 15. Only silicon and SiO_2 are considered in the sensitive volume and its surroundings.

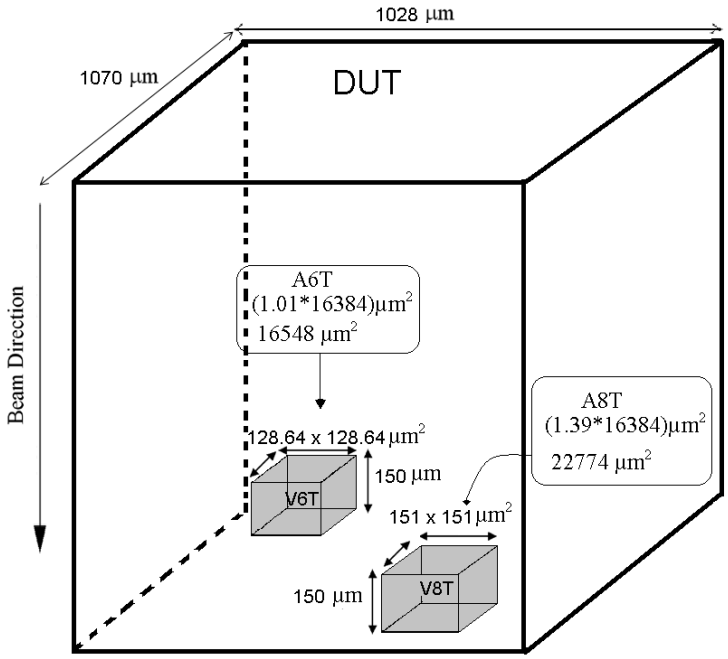
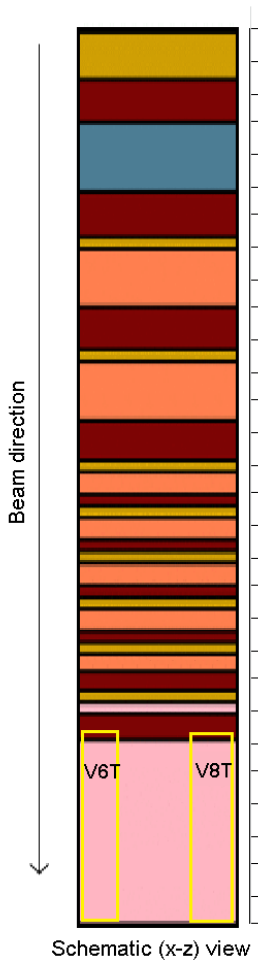


Figure 2. 14. The RPP "sensitive volume" inside the structure of pure silicon. Only the energy deposited in the sensitive volume is tabulated.

To emulate the impact in the device, it was defined in CRÈME MC a planar stack structure consisting of multiple layers of electronic materials which formed the DUT. It is possible to observe in Figure 2. 15 that the sensitive volumes are highlighted in the layer 29 for the volumes V_{6T} and V_{8T}.



Layer	Material	Thickness (µm)
1	Si_3N_4	0.660
2	SiO_2	0.550
3	aluminum	1.595
4	SiO_2	0.576
5	Si_3N_4	0.036
6	copper	1.040
7	SiO_2	0.540
8	Si_3N_4	0.054
9	copper	1.040
10	SiO_2	0.486
11	Si_3N_4	0.054
12	copper	0.242
13	SiO_2	0.086
14	Si_3N_4	0.036
15	copper	0.242
16	SiO_2	0.086
17	Si_3N_4	0.036
18	copper	0.242
19	SiO_2	0.086
20	Si_3N_4	0.036
21	copper	0.242
22	SiO_2	0.086
23	Si_3N_4	0.036
24	copper	0.198
25	SiO_2	0.216
26	Si_3N_4	0.027
27	silicon	0.110
28	SiO_2	0.270
29	silicon	150.000

Figure 2. 15. Stack structure consisting of multiple layer materials. The highlighted squares emphasize the sensitive volume in the SRAMs exposed to the simulation.

Being CRÈME MC a physics-based Monte Carlo simulation code where each incident particle is tracked, the number of particles affects both the counting statistics associated with the results and run time. It was chosen a different amount of simulated particles at different simulation times to be as close as possible to the experimental fluences tested in this thesis.

2.6.4 Alpha CRÈME estimation

The first simulation, which tries to emulate a performed accelerated radiation test using an Americium-241 alpha source, corresponds to an accelerated test using a 5.5 MeV alpha particle beam to a total fluence of $5.71745 \cdot 10^8$ particles/cm^2. For an alpha particle beam of this energy, the linear energy transfer (LET) value is estimated to be 0.58 MeV-cm^2/mg. It is important to note that for an alpha particle with an energy of 5.5 MeV, the penetration range in silicon, calculated by [ZAI04], is 27.76 µm, so it the sensitive volumes of silicon regions were adjusted

to a depth of ~28 µm, assuming that an alpha particle which reaches the silicon region will not overcome that depth.

Figure 2. 16 shows a calorimetry histogram produced after the alpha beam exposure to estimate the deposited energy in the different volumes V_{6T} and V_{8T} and compare them with the energy deposited in the total device V_{CHIP}.

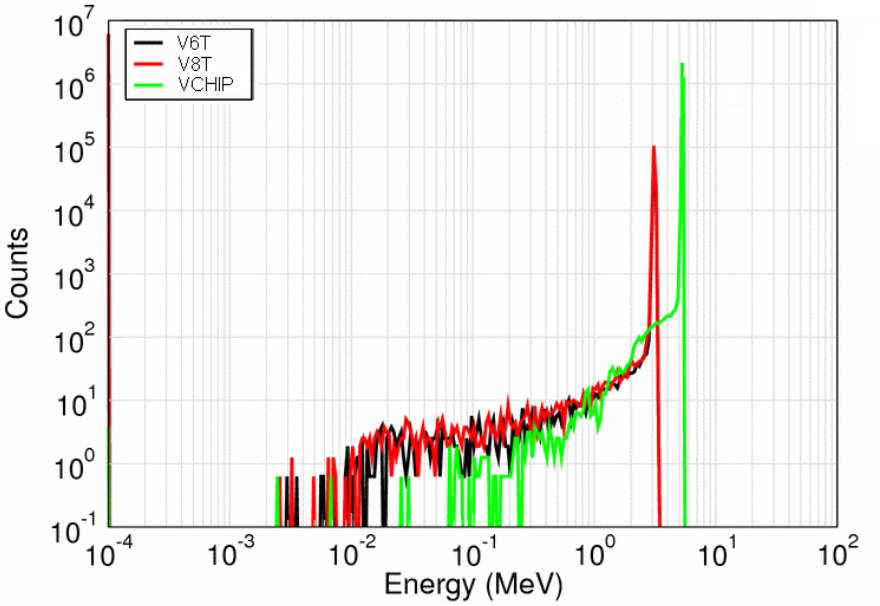


Figure 2. 16. Counts as function of energy deposited in 5.5 MeV Alpha beam simulation.

It is possible to observe that a higher amount of energy is deposited in the first layers, which correspond to the complete chip V_{CHIP}, and the sensitive volumes assumed to SEU in V_{6T} and V_{8T} are quite similar in terms of deposited energy. Although a lot of particles deposit the energy in the first layers, it is possible to say that there are large amounts of energy deposited in the V_{6T} and V_{8T} zones enough to assume that these will cause SEUs, since in silicon, it is necessary that E_{dep}>3.6 eV/ehp in a sensitive node.

According to Equation 2.12, alpha particles that reach the silicon region with the energies estimated in Figure 2. 16, and whose LET is estimated by "*LET calculator"* [ZAI04] could induce a collected energy of up to 223 fC in the silicon volume, which would far exceed the Q_{crit} necessary to produce an SEU.

2.6.5 Proton CRÈME estimation

The second simulation emulates an accelerated radiation test similar to the one performed in the cyclotron at the CNA described in section 3.1.2.1. The simulation consists of a 17 MeV proton beam to a total fluence of $1.10697 \cdot 10^8$ particles/cm^2. For a proton beam of this energy, the linear energy transfer (LET) value is estimated to be 0.023 MeV-cm^2/mg. The sensitive volumes of silicon regions were adjusted to a depth of 150 µm, as the penetration range in silicon, calculated by [ZAI04], is 1790 µm, so it is assumed that a proton could reach the silicon region and deposit his energy or pass through the silicon bulk without interaction.

Figure 2. 17 shows a calorimetry histogram produced after the proton beam reaches the DUT. In this case, although the stopped protons in first layers have high energies; the spectrum for the silicon layers on V_{6T} and V_{8T} is much longer, and this spectrum occupies a range of energies enough to produce a collected charge in the sensitive volumes that can produce SEUs.

As in the previous alpha case, according to equation 2.12, protons reaching the silicon region with energies estimated in Figure 5.8 and a LET of 0.023 MeV-cm^2/mg could induce a collected energy of up to 139,7 fC in the silicon volume, which would far exceed that Q_{crit} necessary to produce an SEU.

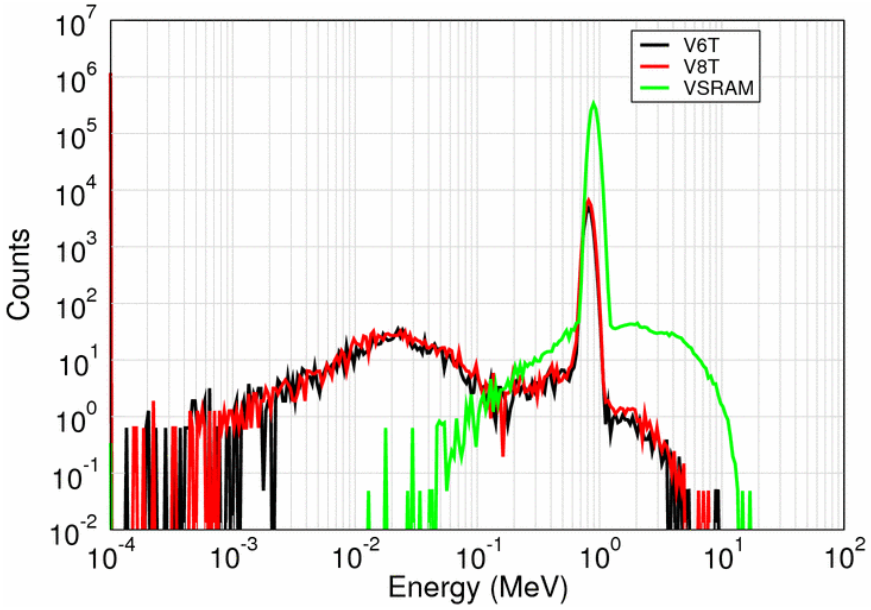


Figure 2. 17. Counts as function of energy deposited in 17 MeV proton beam simulation.

2.6.6 Neutron SPENVIS estimation

For the neutron flux estimation in the SV, MULASSIS from *SPace ENVironment Information System* (SPENVIS) was used. It is a Geant4-based tool that provides a general one-dimensional multi-layered space radiation analysis. To emulate an accelerated radiation test similar to the one performed in the Tandem at the CNA described in section 3.1.3.2, a multi-layered device similar to that shown in Figure 2. 15 using Multi-Layered Shielding Simulation was assumed. The neutron flux and particles produced flux by neutrons in different layers of the device were simulated. The simulation consists in a 5.8-8.5 MeV non-mono-energetic neutron beam with a linear distribution flux, see equation 2.13, and an angular incident distribution between 0º-58º.

$$\left[\frac{d\emptyset}{dE} \times E\right] = A \times E + B \quad [cm^{-2}\,(s^{-1})] \qquad \textbf{2. 13}$$

A distribution flux was assumed to be a linear distribution, but it was adjusted to be as similar as possible to the logarithm distribution from the expected Tandem CNA neutron flux, which will be seeing in chapter 3, see Figure 2. 19. Thus, the constant values in equation 2.13 are A=$51 \cdot 10^3$ and B=$-53 \cdot 10^3$.

A neutron incidence of 10^7 n/cm^2 reaching the DUT was simulated. As known, neutrons produce SEE by indirect ionization. In this case, it would be helpful to know the generated flux of secondary particles which could produce direct ionization reaching the sensitive volumes in the device. So, to estimate the probability of finding SEE in the DUT, the simulation is made to estimate these secondary protons, alpha particles or electrons.

The obtained data for proton and electron, generated on different layers of the device (see Figure 2. 15), is shown in Figure 2.20 and in Figure 2.21. It is possible to observe that, although neutron fluence reaching first layers in the device and silicon layer (SV) at the end of the device is quite similar (see Figure 2. 18), the secondary particle fluxes generate by neutron interaction in the device are significantly different. It is important to emphasize that these secondary particles are able to change the state of the SRAM by direct ionization.

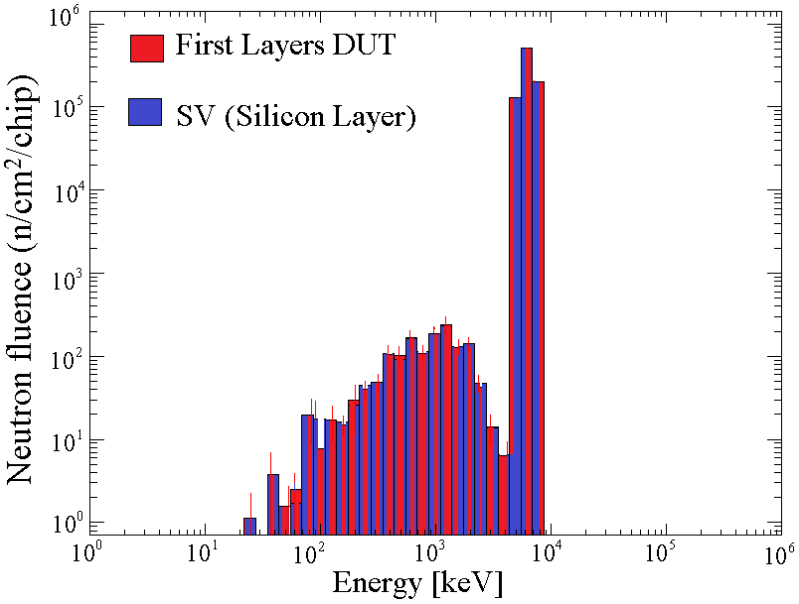


Figure 2. 18. Neutron fluence analysis at first boundary of the DUT (red) and at the last one boundaries SV regions (blue).

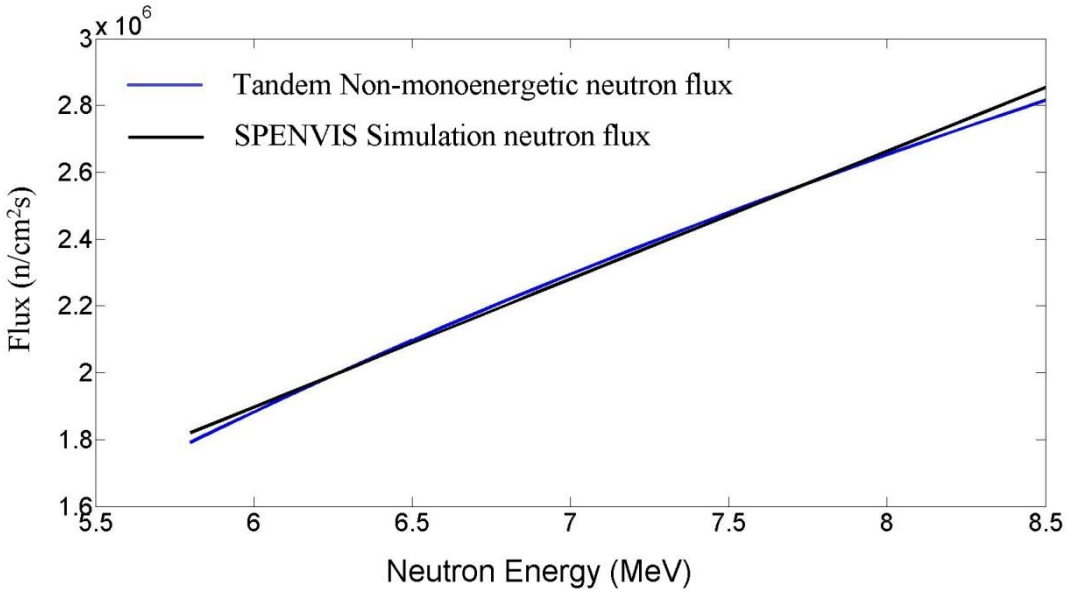


Figure 2. 19. Expected Tandem CNA neutron flux (n/m^{2}s) vs SPENVIS Simulationas as function of the energy.

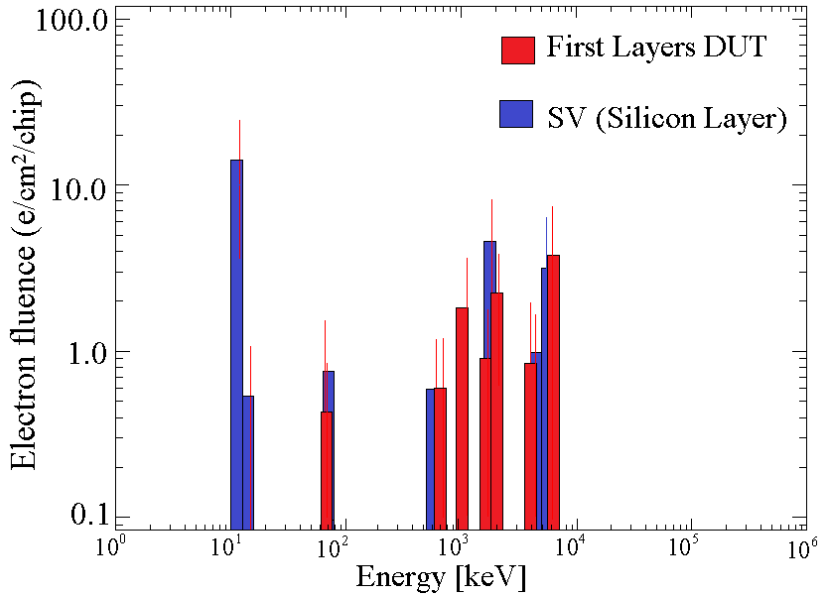


Figure 2. 20. Electron fluence analysis at first boundary of the DUT (red) and at the last one boundaries SV regions (blue).

It is important to note that the SPENVIS simulation corresponds to ~1.6 seconds of the flux tested in this thesis, so the charge collected from protons, and electrons due to neutron interaction during the real case in section 3.1.3.2 is ~10^4 higher.

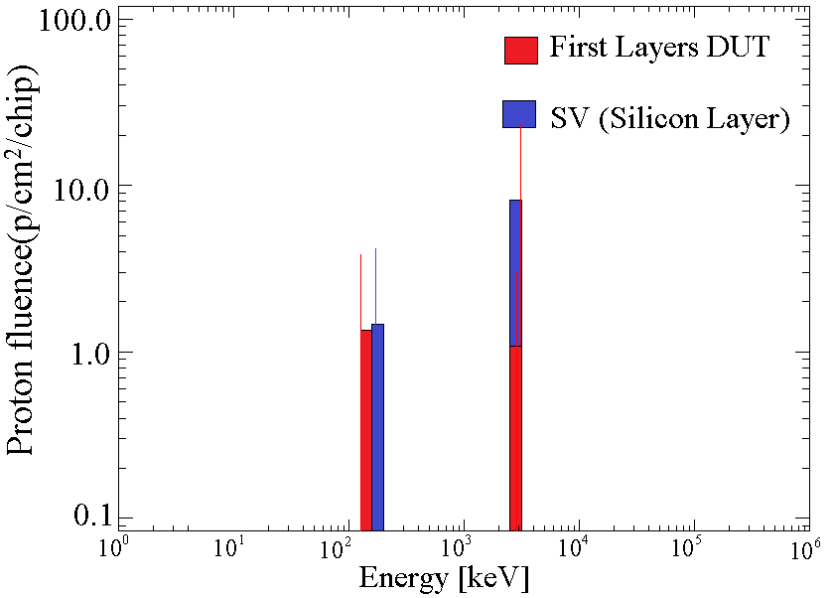


Figure 2. 21. Proton fluence analysis at first boundary of the DUT (red) and at the last one boundaries SV regions (blue).

It is important to know if these secondary particles are capable of generating SEU by indirect ionization. CRÈME MC was used to estimate if electrons or protons with these energies are able to deposit enough charge during similar situations as those considered in this thesis, which will be discussed in next chapters. Using CRÈME simulations it is possible to observe that

secondary particles like electron or proton with fluxes as those shown in the Figure 2. 20 and Figure 2. 21 are capable of generating counts in the SV with energies like the ones shown in Figure 2. 22 and Figure 2. 23.

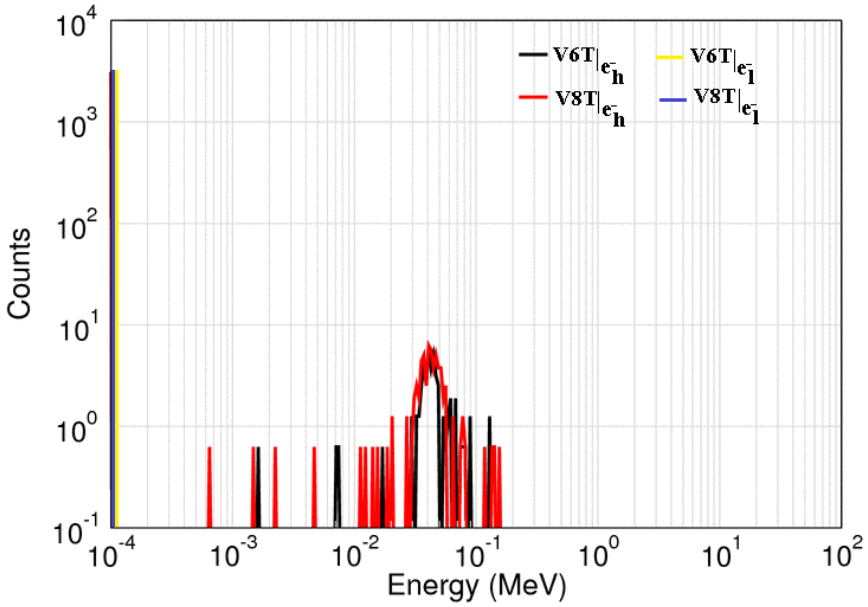


Figure 2. 22. Counts as function of energy deposited in SVs by lower energy secondary electrons (e^-_l =0.01 MeV) and higher-energy electrons (e^-_h=7 MeV).

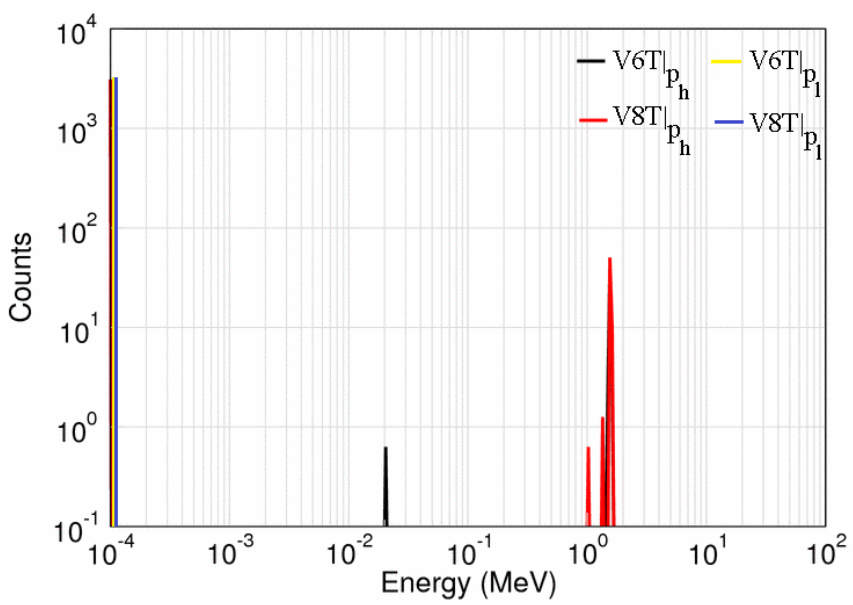


Figure 2. 23. Counts as function of energy deposited in SVs by lower energy secondary protons (p_l =0.2 MeV) and higher-energy protons (p_h=2 MeV).

Taking into account Figure 2.22 and the data obtained about the total counts which correspond to ~$3 \cdot 10^5$ e^-/cm^2, it is possible to estimate that the number of electrons generated in the SVs during the complete simulation are not enough to generate charge collected and induce SEUs. It

is because it is necessary overcome a Q_{crit}=1.72 fC which corresponds to a minimum of ~$1.076 \cdot 10^4$ e^- counts in a sensible node and the collected charge was below 70 e-/SV for both V_{6T} and V_{8T} over the total area.

Nevertheless, although Figure 2.20 represents a total fluence for protons equivalent to that of electrons, ~$3 \cdot 10^5$ p/cm^2, the interaction with protons requires using the equation 2.12 to estimate that a proton reaching a sensible area is able to collect charge at a sensitive node within the SVs.

The charge collected from the interaction of protons is estimated, knowing that for lower energy protons ~0.2 MeV corresponds to a LET_{pl}= 0.34 MeV/mg/cm^2, and for higher protons induced ~2 MeV correspond a LET_{ph}= 0.1132 MeV/mg/cm^2. So those correspond to a possible collected charge of 520 fC to induced protons to lower energies and 170 fC to induced protons to higher energies, both of which would far exceed the Q_{crit} necessary to produce an SEU. Note that this proton fluence corresponds to a TID not higher to 25 krads in the worst case (higher LET).

Monte Carlo simulations of energy deposition have shown that electron and protons are generated by fast neutrons-DUT interactions and that proton-induced charges are likely to be collected in regions which are considered sensible to SEUs.

The simulations for thermal neutron (30 keV) using SPENVIS tools did not give results to generation proton or electron in the DUT.

Note that the secondary particles as alpha were not estimated because these particles are not included in CRÈME or SPENVIS tools, but this kind of particles are generated in high probability by neutron-silicon interaction, so further would increase the probability of finding SEUs by indirect ionization.

2.6.7 HEH CRÈME estimation

Due to a number of different particles and energy range over a HEH environment, to estimate the charge collected in this case, it is considered an interplanetary environment rich in high-energy particles and therefore, potentially having an impact on the SEE. The operational and experimental environments considered in this thesis will be introduced throughout this chapter 3. Test configurations at CHARM closely reproduce the environments at an accelerated rate similar to a GCR environment.

In this case, it simulates a space environment using the CREME96 online tool considering a CREME96/FLUX model for Galactic Cosmic Rays (GCR) with Solar Minimum (Cosmic-Ray Maximum) conditions, and a near-Earth interplanetary/Geosynchronous orbit. If the atomic

numbers of the species to be included in the simulation are Z=1 and Z=2, the flux obtained is shown in .

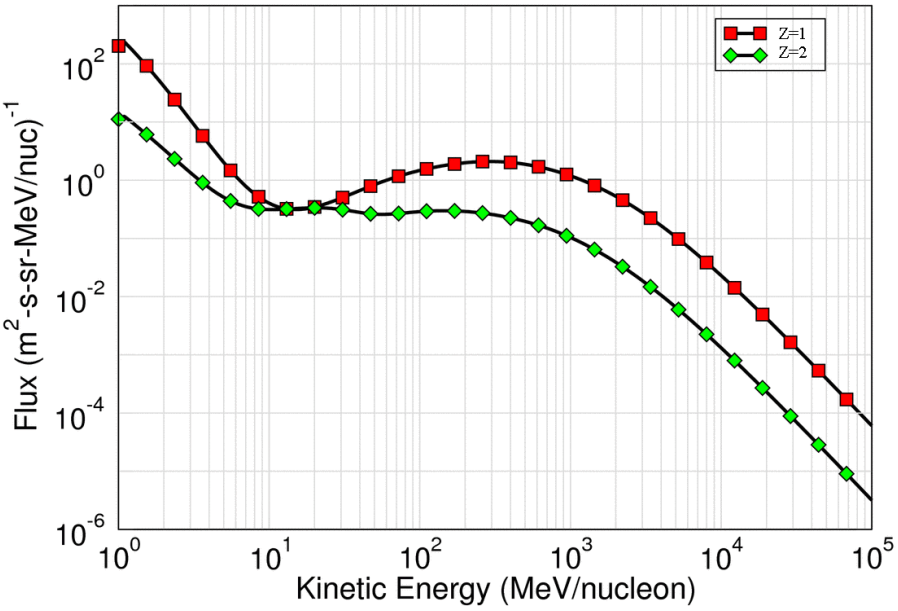


Figure 2. 24. Simulated Interplanetary differential particle energy spectra using the CREME online tool.

As it can be seen, at space environments fluxes peak at energy near 500 MeV per nucleon and these are extending to very large energies still with a significant flux.

The results of the simulation to exposure the DUT in the Figure 2. 15 to the flux in the Figure 2. 24, of ~$1 \cdot 10^7$ HEH/$\underline{A_{chip}}$, (equivalent to a fluence of ~$9 \cdot 10^8$ HEH/cm^2), are shown in Figure 2. 25.

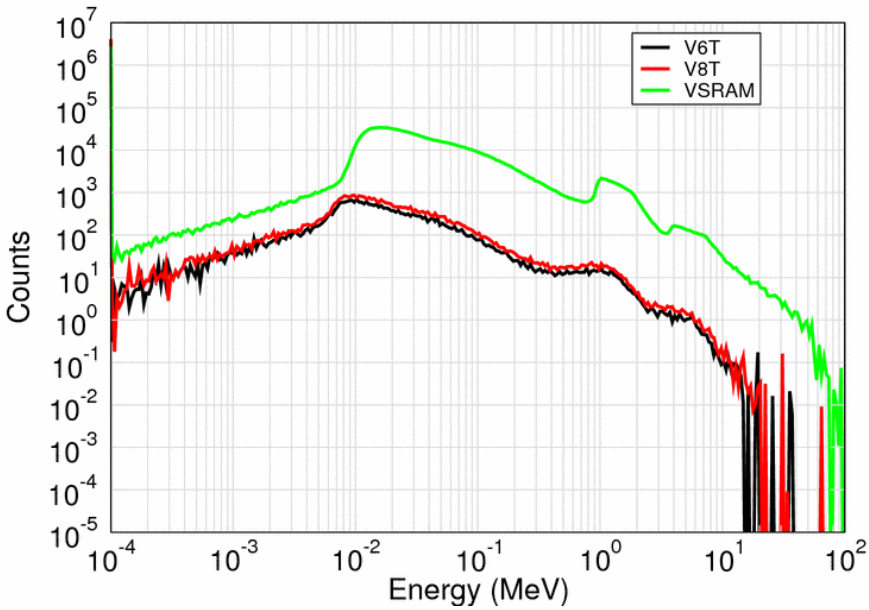


Figure 2. 25. Counts as function of energy deposited in a HEH beam simulation.

It seems clear that, if the counts and energies of these particles interacting with the device, which includes protons, are greater than those shown in previous sections, the charge collected should be higher in all cases, so that the charge collected at the sensitive nodes would be more likely and there would be a greater possibility to find SEUs in a HEH environment. Thus, because the counts in all energy range is large enough even at higher energies, it seems logical to suppose that SEUs are generated by HEH interaction with the DUT in an interplanetary environment. An empirical result realized in CHARM/CERN facilities will be shown in chapter 3 to compare with the simulation results and to obtain SER in SRAM devices, which have been simulated in this chapter.

So, having into account the deposited energy in all simulations cases and using the equation 2.12, it is possible to get an overview about the deposited charges into the sensitive volumes comparing the deposited charge for alphas in the cases of alpha source exposition and the protons charge deposition in all other cases. Figure 2. 26 shows an example of the deposited charge by particles as a function of the energy which reaches the sensitive volumes in the above simulations.

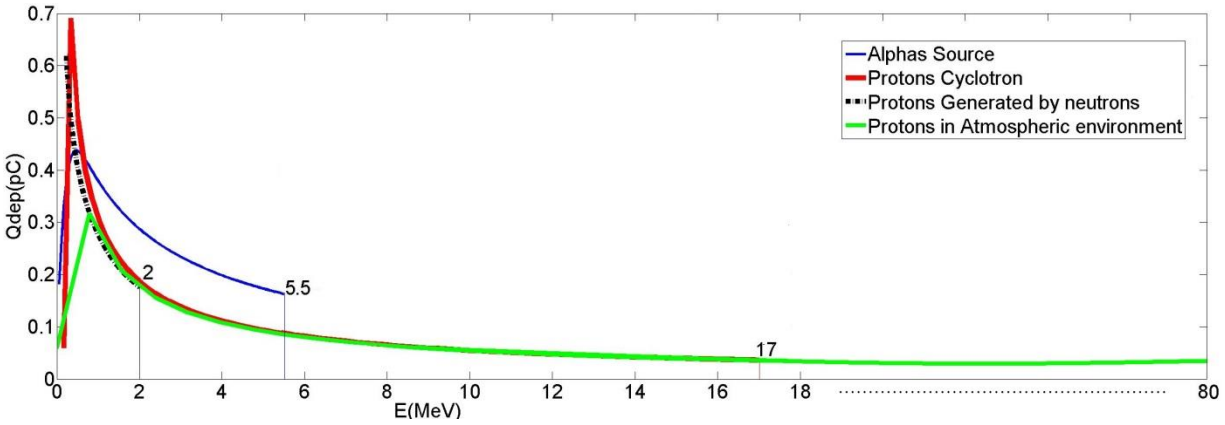


Figure 2. 26. Deposited charge for alpha particles and protons as function of Energy in Silicon.

Comparing the different simulations, a 5.5 MeV alpha particle deposits higher charge than 17 MeV mono-energetic contributions. Protons generated by 5.8-8.5 MeV non-monoenergetic neutrons, which have an energy about 2 MeV, would be able to deposit higher charge than 17 MeV protons. It is therefore expected that neutron particles would be capable of causing a greater amount of SEU than proton with 17 MeV, as these particles could collect more charge in devices.

CHAPTER 3

ACCELERATED TEST TECHNIQUES

The knowledge about the radiation environment is essential to evaluate the expected SEE impact on a specific component. A test is generally defined as a *procedure that taking measures intended to establish the quality, performance, or reliability of something, especially before it is taken into widespread use*. This means that the test reproduces the practical application before the device under test is used. Therefore, test conditions need to be similar to those of the intended application, or at least be able to extrapolate its results to real environment. One of the main characteristics in radiation tests is that these are usually accelerated, that means that they are design to mimic the operational conditions in a much shorter time. Furthermore, the source that produces a certain radiation field in principle does not have to be the same as the one in the operational case. Usually, radiation tests are performed with less particle species and energy range than the ones present during operation. Accordingly, it is important to correlate the different radiation effects expected in an operational environment to those measured under experimental conditions to predict realistic failure rates for the critical electronic devices.

This chapter describes the different accelerated test facilities used in this thesis, from a simple facility used in alpha test to the modern high-energy particle accelerators located at National center of accelerators facility, CNA (Seville) or at the European Organization for Nuclear Research CERN (Genève), which are extremely elaborate machines.

Experimental data are obtained from an experimental setup modified in each situation for:

- an alpha particle test at University of Balearic Islands
- a monoenergetic proton beam at CNA
- a non-monoenergetic neutron beam at CNA and
- a mixed–field hadron beam at CERN

The component needed to evaluate the SEE error rate for a specific device or electronic system is its sensitivity to SEEs, represented through the respective cross sections.

3.1 Mono particles facilities

Monoenergetic tests aimed at extracting the SRAM error rate are focused on (i) alpha particles, (ii) thermal neutrons and (iii) 18 MeV proton measurements, although, in practice, test beams are not totally monoenergetic due to their degradation or energy dispersion. In particular, for thermal neutrons, a peak around 30 keV is used.

A non-monoenergetic test with neutrons (1–10 MeV range) is presented to test the device in a neutron environment as close as possible to 10 MeV, following the hypothesis that affirms that, with the suppression of BPSG layers in modern technologies, Single Event Upsets (SEU) encountered in SRAM are now mostly attributed to high energy neutrons above 10 MeV [BAG07].

In the following subsections, test facilities used in this thesis work are presented.

3.1.1 Alpha particle accelerated test

Irradiation with monoenergetic alpha particles was conducted at the laboratory of the University of the Balearic Islands. The alpha source is an Am-241 (Figure 3. 1). Americium is a metal of atomic number 95, which does not exist naturally. It is artificially produced by successive neutron capture from isotopes of plutonium. The Am-241 is an alpha emitter but also emits low-energy gamma radiation as a by-product through the reaction:

$$^{241}_{95}Am \rightarrow {}^{237}_{96}Np + \alpha + \gamma \qquad \textbf{3. 1}$$

The resulting neptunium nucleus undergoes a long chain of disintegrations and, at the end of his radioactive life, becomes Thallium-205, which is stable. It is possible to model the source as a constant flux emitter, as the half-life of Am-241 is 433 years.

The active zone of the source is circular-shaped, and it is located at the center of the opposite face of Figure 3. 1. The packaging that covers the source is stainless steel, and it is used as support for the active zone and to allow a safe handling of the source.

According to the Nuclear Safety Council Instruction of 26 February 2003, which defines the exemption values for nuclides, facilities that involve substances with activities below the exemption values for the specific substance will be not considered the radioactive facilities. The Am-241 has an exemption value of 10 kBq, which is less than the activity at the source (5 kBq) [CSN12]. For this reason, it is not necessary for the Nuclear Safety Council to carry out

any monitoring or control over the installation in which the source is used, in this case, the laboratory of the University.

Figure 3. 1. Source of alpha particles close to one euro coin to appreciate its size.

The main characteristics of the alpha source are a diameter of the die of 25mm with a diameter of the active zone of 7 mm and a matrix thickness of 0.5 mm. The alpha source active area is about 38.5 mm^2 and the source activity is 5 kBq±30% with an emission energy of 5.5 MeV. The distance between the source and the DUT surface was 3 mm approximately. So, if we consider an alpha beam flux of $5 \cdot 10^3$ alphas/s and the setup present in this thesis, the alpha particle beam obtained exposes the sample to a flux of 3250 alphas/s·cm^2.

3.1.2 Cyclotron CNA

In 2004, an 18/9 compact cyclotron was installed at the CNA (National Centre for Accelerators) in Seville, and it is nowadays the highest proton energy source in Spain. It is capable of generating proton beams (18 MeV, 80 μA) or deuteron beams (9 MeV, 35 μA) from two sources of internal ions (Penning type) manufactured by the medical technology company based in Belgium IBA (Ion Beam Applications) [GAR00].The machine has eight target ports, seven of them are dedicated to short half-life radioisotopes production for Positron Emission Tomography studies. The eighth port is connected to a beam line which is dedicated to the radiation in materials and electronic components, this includes a series of remote control permanent elements to monitor and to define the beam current and size. The proton irradiation techniques of technological samples for radiation damage studies are one of the objectives of this facility [RES08, 38]. The last section is in a separated vault with two meters thick wall and there is a neutron shutter which is automatically retracted once the beamline is selected. A very

simple and versatile external beam has been developed to perform experiments in air, see Figure 3. 2. Several nozzles with different sizes are available, where diverse material windows can be adapted, and where it is possible to accommodate graphite collimators with various hole diameters.

The magnetic sweeping system consists of two magnets for horizontal and vertical sweeping and the maximum magnetic field is 0.25 T. It is possible to select the frequency of the power supplies of the magnets from 20 to 30 Hz in steps of 0.05 Hz. Thus, by choosing values out of phase it is possible to achieve that the beam covers the same route every 20 seconds, guaranteeing the uniformity of the fluence in a maximum area of 16 × 20 cm^2.

Figure 3. 2. SRAM SEU test during the June 2014 irradiation test at CNA. External beam to perform experiments in air.

The target to be irradiated is placed on a robotized table in the air. Although the maximum particle current density for protons in electronics experiments is of 1 μA/cm^2 (~$6 \cdot 10^{12}$ particles/$cm^2 \cdot s$), it can be reduced with diaphragms to 10^2-10^8 particles/$cm^2 \cdot s$.

For fluences greater than 1pA/cm^2, the current is measured directly on a graphite tray using a Brookhaven 1000c current integrator, Figure 3. 3.

The cyclotron and the beam line are located in adjacent rooms, equipped with shielding and instrumentation for radiological safety.

Figure 3. 3. Brookhaven 1000c current integrator and graphite tray monitored view behind.

3.1.2.1 Monoenergetic proton Facility Setup

It is possible to mount the test board on a robotized arm which can be moved to focus the proton beam on the target (Figure 3. 2). A specific test board, compatible with the CNA setup, was designed to bias the device and set up the adequate configuration to write and read-out the memories during the proton beam irradiation. This control is achieved using an Altera FPGA that communicates with a host PC through a USB port which configures the FPGA through a Blaster cable and sends read-out the chip data through an RS-232 connection, (Figure 3. 4).

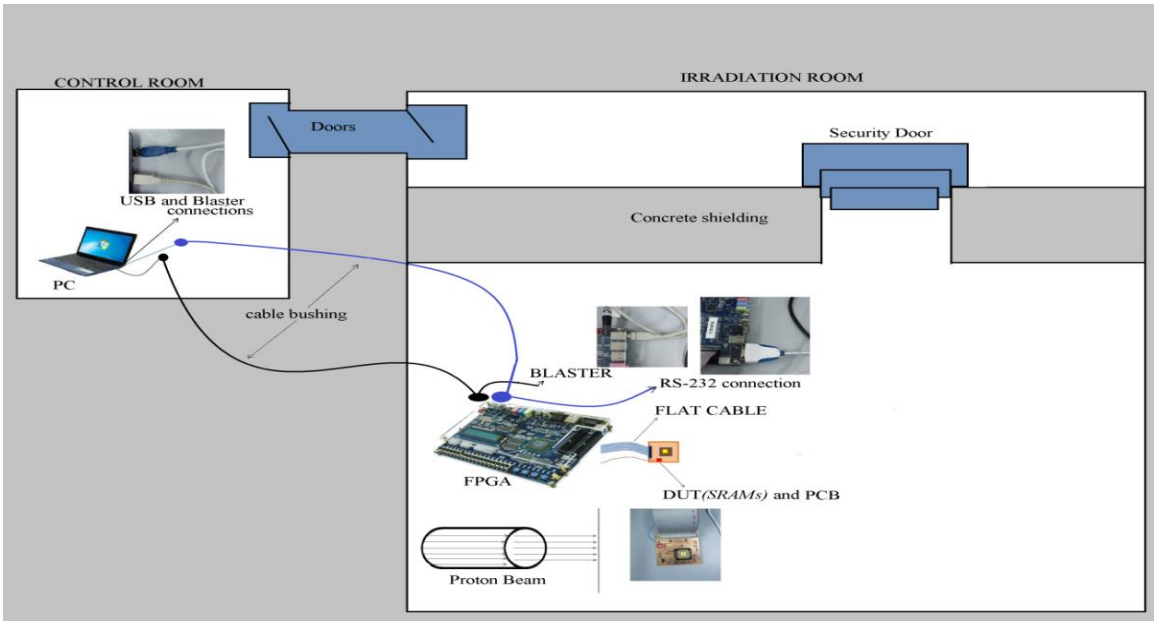


Figure 3. 4. CNA Setup in Proton Irradiation.

The DUT was set about 10cm away from the proton beam output, see Figure 3. 5. As stated above, the CNA's cyclotron is capable of producing proton beams of 18MeV. Although due to the air environment, the proton energy that reached the chip surface was about 17 MeV. This value has been obtained using the energy loss data calculated by the SRIM2008 code [ZIE08].

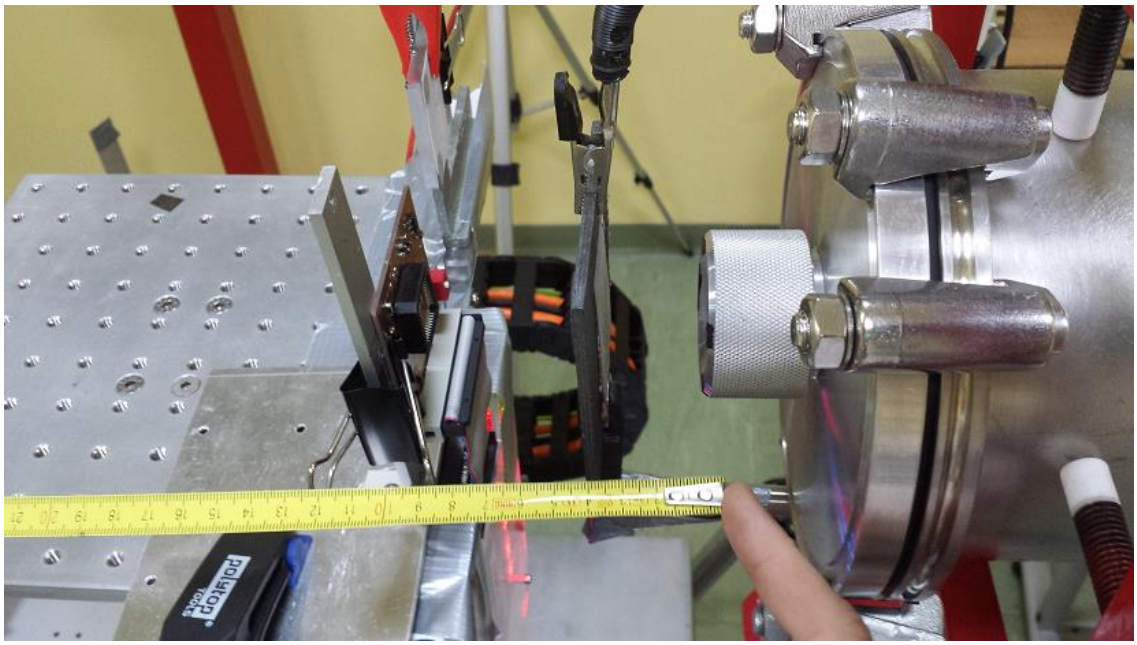


Figure 3. 5. SRAM SEU test during the June 2014 irradiation at Cyclotron (CNA). From left to right, the DUTs can be observed on the table to 6 cm from the graphite tray, which it is to 4 cm from the proton beam output.

The beam can be considered to be almost completely focused on the DUT, so the FPGA remains out of the beam line to avoid its direct irradiation (see Figure 3. 4). As stated in section 3.1.2, the ion flux is obtained from the beam current with a Brookhaven 1000c current integrator, however, as the circuit is connected to the control system, direct current reading of the target is not available and the proton flux monitoring has been performed in an indirect way. During the tests, the beam current is measured into the electrically isolated graphite collimator behind the exit window. To calculate the corresponding proton flux at the DUT, a correlation factor is obtained performing a calibration process, by simultaneous measurements into the graphite collimator and another graphite plate placed at the DUT position. The secondary electron losses in graphite are taken into account. It was found that beam flux was difficult to maintain under control for values lower 400pA/cm^2, equivalent to $1.6 \cdot 10^9$p/cm^2·s, where the flux values fluctuated within 6% during each run. Finally, the fluence (p/cm^2) at the DUT was calculated with accuracy better than 10%. It is important to notice that the collimator is covered with a thin ZnS(Ag) scintillator film to observe the light produced by the protons to be sure that the ion beam always hits the same position.

3.1.3 Tandem CNA

The Tandem accelerator in the National Center of Accelerators in Seville was the first accelerator installed in the CNA and it is fundamentally an analytical and matter modification tool. It is a Pelletron tandem accelerator of 3 MV, model NEC-9SDH-2 [GAR08]. It accelerates protons, alpha particles and a wide variety of other ions by generating a high voltage of up to 3 Million Volts (MV).

Those ions are obtained from three sources. One of them is based upon the use of radio frequencies (Alphatross) and generates negative ions from gases (H, He, N ...). Another is a caesium bombardment source (SNICS), which generates negative ions from a solid sample. And the last one, and the latest installed, it is a Duoplasmatron type source, which is very stable and provides a high brightness beam. The sources are connected by different ports to a magnetic deflector which selects the desired masses.

An injection system is capable of taking the ions to the accelerator´s tank, where very high-voltages have been generated by mechanical charge transport, such it is produced an acceleration of the ions.

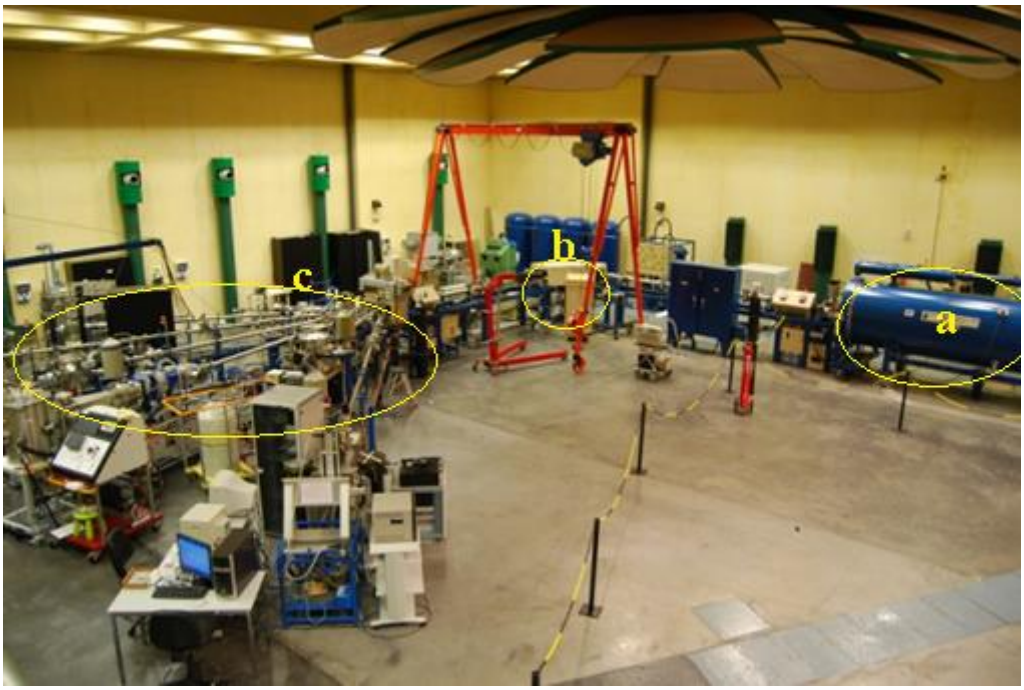


Figure 3. 6. From left to right, the elements that can be seen are the research lines (c), selector magnet (b) and accelerator´s tank (a), source [CNA].

After the ions are extracted from the accelerator, a 90° analytical magnet allows separating the ionic species and the desired charge from the rest of the beam. After passing the magnet at 90°, the beam can pass directly through line 0° or it can be deflected by a selector magnet to another of the six possible lines.

The Accelerator is monitored from the control room outside the Tandem room (where the accelerator is located). From this room, it is possible to control the parameters and equipment to achieve a beam of particles with the required characteristics for the experiment. The rate of gamma-ray and neutron radiation is measured continuously by two dosimeters above the selector magnet.

3.1.3.1 Monoenergetic thermal-neutrons

As it is seen at Table I, in terrestrial environments, neutrons are the dominant cosmic-ray by-products that cause soft errors. High-energy neutrons can lose energy by scattering with materials in the environment and ultimately reaching the thermal equilibrium energy and becoming thermal neutrons (~25 meV) [GOR04]. The typical shape of the energy differential spectrum in isolethargic (logarithmic) units at the ground level is shown in Figure 3. 7.

Neutron scattering or absorption events depend on the cross-section, which is proportional to the neutron energy, and the atomic density at the target. Semiconductor materials have a low probability of interacting with free neutrons. Thermal neutron cross-section for naturally occurring silicon is about 2.24 barns($1 \cdot 10^{-28}$ m^2) and it means that a thermal neutron would have to travel across a mean free path of about 8.6 cm before it is scattered or it is captured [RIN91]. For this reason, although it is not practical to detect neutrons using only modern Si devices, solid state semiconductor thermal neutron detectors are interesting, and nowadays they are being developed because it is possible to make them more compact, operate at lower voltages, and be more robust against vibration induced noise.

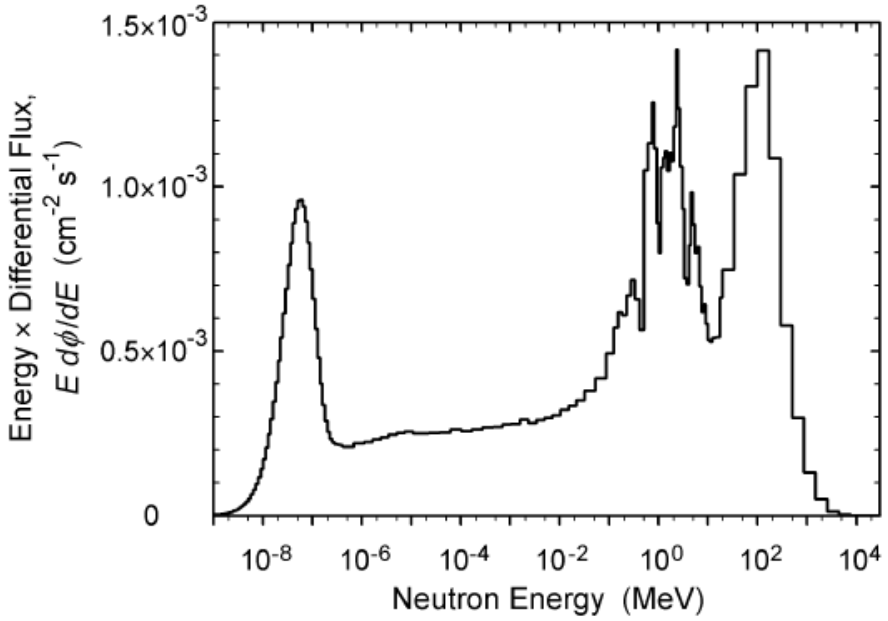


Figure 3. 7. The neutron spectrum measured outdoors on the of the IBM T. J. Watson Research Center in Yorktown Heights, NY (source [GOR04]]

The thermal part of the spectrum is capable of inducing soft errors in ICs because of the very large reaction cross section of thermal neutrons with ^{10}B, an isotope that was commonly found in many IC processes as a substrate dopant and in the glass passivation layers.

The most probable result of the interaction of a thermal neutron with ^{10}B is a 1.87 MeV alpha particle and 0.84 MeV ^{7}Li particles along with a 0.48 MeV photon [BAU01]. Both α-particle and lithium nucleus releases enough energy to cause SEEs.

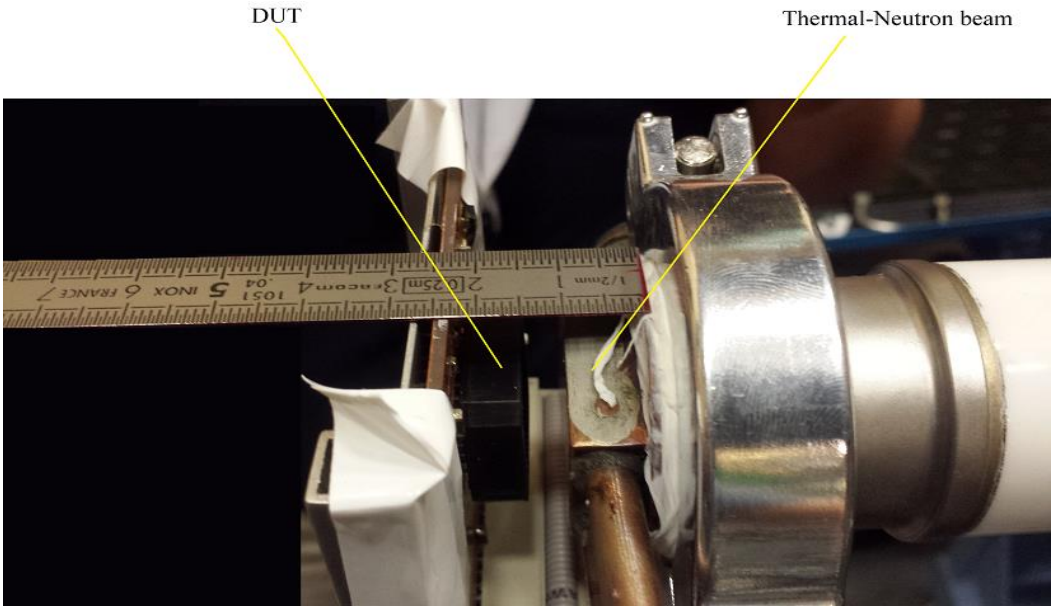


Figure 3. 8. From left to right the DUT and the thermal neutron beam output.

To test the performance against the effects of thermal neutrons, an experiment was developed at the CNA with neutrons of 30 keV. This beam consisted in a quasi Maxwellian at kT=30 keV produced by the ^{7}Li(p,n) reaction at 1.912 keV proton energy. It is based on the energy degradation of the incident proton beam at energies close to the ^{7}Li(p,n)^{7}Be reaction threshold [PRA14, IRA16].

The neutron productions have been measured using EnergySet [LOV02] based on [LIS73] to produce reliable data of total neutron yield within a 10-20% uncertainty. The neutron production can be calculated if the number of protons on the target is measured (measuring the charge accumulation of protons in lithium). At the same time, the neutron dose was measured with a dosimeter to verify that the neutron production remained constant. The production was estimated about $2 \cdot 10^{9}$ neutrons/cm^{2}·s and, assuming that the neutron source-device distance was 7mm, see Figure 3. 8, the flux in the device was $1 \cdot 10^{7}$ neutrons/cm^{2}·s.

3.1.3.2 Non-monoenergetic fast-neutrons

With the suppression of BPSG layers in recent fabrication technologies, neutron induced SEUs in SRAM based systems are now mostly attributed to high-energy neutrons [BAU02]. Although it was seen in chapter 2 that neutrons are not directly ionizing particles, it is known that above an energy threshold, they can interact with the ^{28}Si atoms creating secondary ions and, for silicon target, the created ion species range from hydrogen to phosphorus [WRO00]. These

secondary particles can be generated anywhere in the semiconductor material and emitted in any direction. Some of these reactions occur above energy thresholds of few MeVs, such as $^{28}Si(n,p)^{28}Al$ with a 4 MeV threshold and $^{28}Si(n,\alpha)\ ^{25}Mg$ with 2.7 MeV.

It has been reported that below the 0.25 μm CMOS IC technology node, bulk technologies exhibit a relatively high sensitivity to neutrons between 4 and 6 MeV [BAG07], which is explained by the contribution of alpha particles coming from (n,α) reactions. SRAM technologies (below 0.18μm) exhibit a significant SEU sensitivity to neutron energies as low as 4 MeV [BAG07], while the 65 and 90 nm nodes have shown SETs at 1 MeV [LAM09].
Although previous works have demonstrated that above 50 MeV, the effects on microelectronic circuits of protons instead of neutron seem comparable [BAG04], which agrees with the well-known behavior in nuclear physics that the two cross-sections tend to the same values at high energies, it is known that protons and neutrons interact differently with matter and, at lower energies, between 5 and 14 MeV, there is a mean shift of 2-4 MeV to have the equivalent SEU cross-section, i.e. $\sigma_{proton}(E + 2\text{-}4\ MeV) = \sigma_{neutron}(E)$ [LAM09].

To obtain neutron energy as close as possible to 10 MeV, a deuteron beam of 5.3 MeV was produced working at the maximum available terminal voltage of the 3 MV Tandem accelerator at CNA. This beam consisted in a fast neutron field produced by the $^{2}H(d,n)^{3}He$ reaction.

The neutron production target consisted of a deuterated target with Titanium deposit with the following characteristics: 500 μg/cm^2 thickness, 3 mm aluminium backing and D/Ti ratio equal to 1.5. The deuterium beam was collimated to 1 cm in diameter (Figure 3. 9) and the current was recorded.

Figure 3. 9. Deuterium-implanted titanium (TiD_2), thickness = 500 μg/cm^2, Ratio D/T > 1.5 and backing of aluminium of 3 mm.

Except in the initial preparation and calibration of the beam, where an unusual peak was observed, and a few pauses during the irradiation due to the warming in the magnets of the accelerator, the beam average current was 300 nA, see Figure 3. 10.

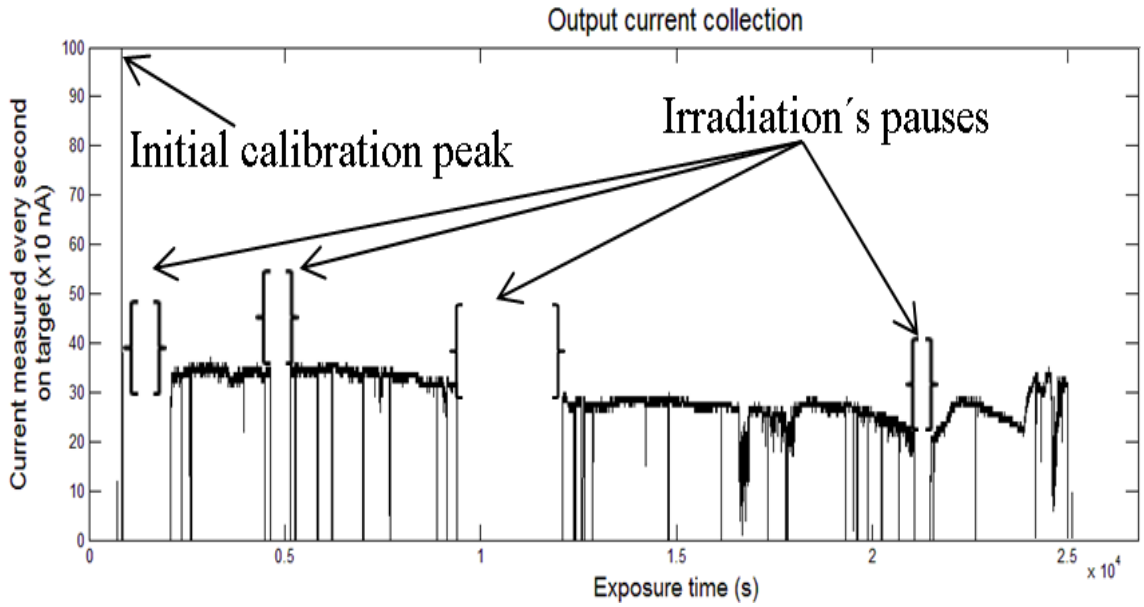


Figure 3. 10. Deuterium current measured on the TiD_2 target.

Considering a quasi-constant deuterium current of 300 nA on the target, the most important parameters of the ^{2}H(d,n)3He reaction can be estimated [LIS73], Figure 3. 11.

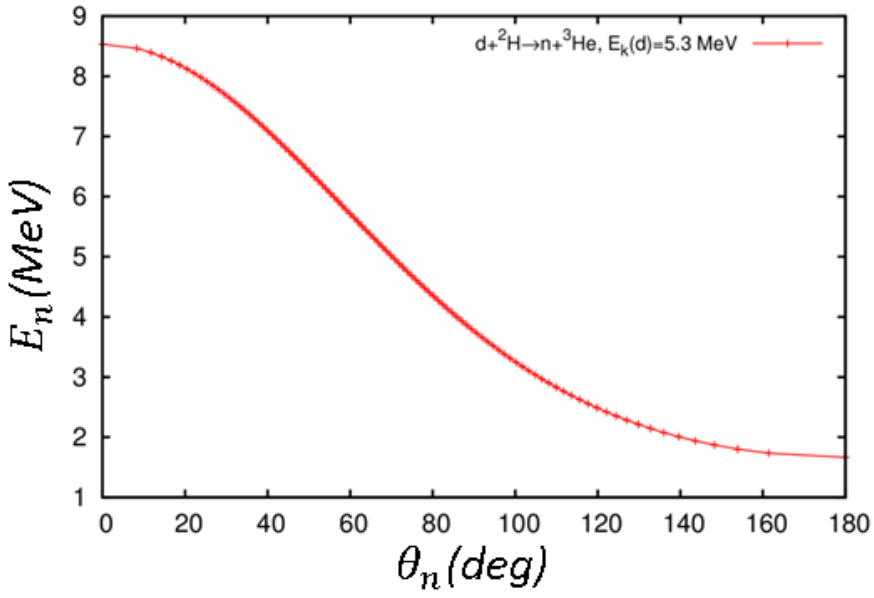


Figure 3. 11. Neutron energy in the ^{2}H(d,n)^{3}He reaction

As in thermal-neutrons, EnergySet [LOV02] based on [LIS73] was used to produce reliable data of total neutron yield and angular-energy distributions. As in the previous section, neutron production can be calculated if a number of deuterons on the target is measured, that is measuring the charge accumulation of deuterons in Deuterium. Table III shows the expected fluxes for each predicted energy, which can produce a reaction on the device. Assuming ~5 mm distance target-device, a target diameter of 1cm and a chip surface of 1.1x1.1 mm^2, the angular aperture of the neutron which can produce a reaction in the device can calculated, obtaining an angular aperture from 0° to 58°, (Figure 3. 13). So, the device was irradiated with neutrons from 5.8 to 8.5 MeV, and the expected fluxes calculated by integrating the values of the figure 3.10 are shown in Fig 3.12.

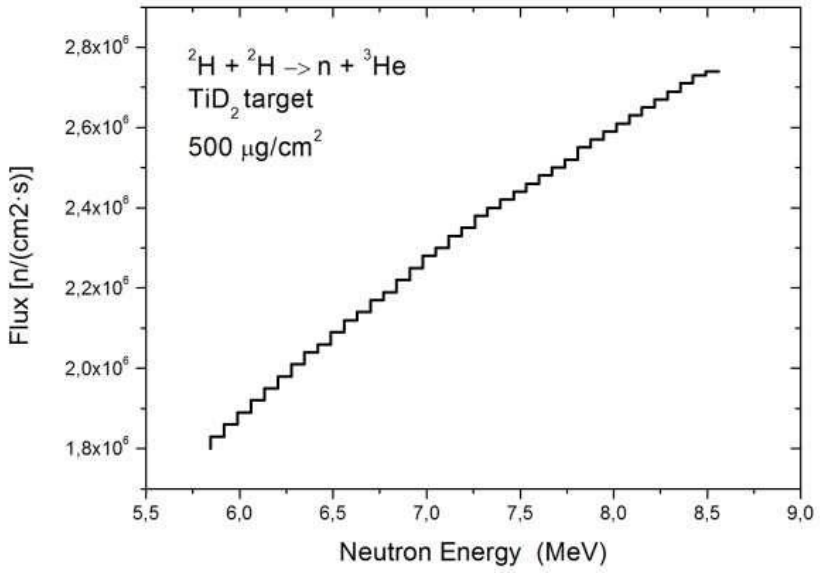


Figure 3. 12. Expected neutron flux (n/cm^{2}s) as a function of the energy onto the chip during our irradiation.

Table III shows the energies and the expected fluxes, which can produce a reaction in the device that will be analysed in chapter 5.

Table III. Energies and the mean fluxes expected to reach on the device.

	0° (3mm)	**20° (5mm)**	**40° (1cm)**	**58° (1cm)**
Mean flux (10^6 n/cm^2·s)	2.7	2.6	2.5	1.8
Mean neutron Energy (MeV)	8.5	8.4	8.1	5.8

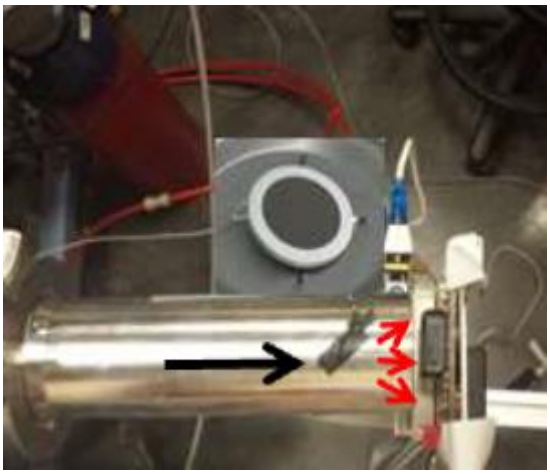


Figure 3. 13. Setup for fast neutrons during the positioning of the chip. Deuterated target (inset). Black arrow represents deuterium beam and red arrows represent neutrons in the forward direction.

3.2 Mixed-field hadron facilities

As it was seen in chapter 2, in the upper atmosphere, the incidence of the radiation sources not only comes from monoenergetic protons or neutrons but from high-energy cosmic rays, which can generate other particles when they interact with the atomic nuclei of the atmosphere elements, mainly with those of oxygen and nitrogen. This situation is similar to a high-energy accelerator radiation field.

Many radiation environments can be described as mixed-field, such as the atmospheric and stratospheric spectra, where protons, neutrons, pions or muons are found, hence this type of radiation is called 'mixed'. The main characteristic of the atmosphere radiation environment or the high-energy accelerator radiation field is that those are of mixed nature, both in terms of hadron types and energy interval.

To test the device in similar conditions to an atmospheric environment or, in a high-energy accelerator context, a High-Energy Hadron test at CHARM was planned.

3.2.1 CHARM facility at CERN

Testing at CHARM has been driven by the need of characterizing the radiation response of electronic components in an environment resembling that of the LHC and other CERN locations of interest. The aim of the CHARM facility is to have a dedicated place for the testing of electronics and systems in characterized mixed-radiation fields. These mixed-fields can

replicate a wide number of real radiation environments such as atmosphere, space or accelerator complexes, for example [THO16].

CHARM facility is situated in the Proton Synchrotron (PS) East Area hall at the Meyrin Site of CERN in Switzerland.

PS was built as a 24GeV proton accelerator and begun operating in 1959. It is the oldest major particle accelerator at CERN. The accelerator is part of the LHC injector chain, accelerating protons and heavy ions. Figure 3. 14 shows a diagram of the CERN accelerator complex in which it is possible to appreciate the position and dimensions of PS versus other lines at CERN and the different particles generated in them.

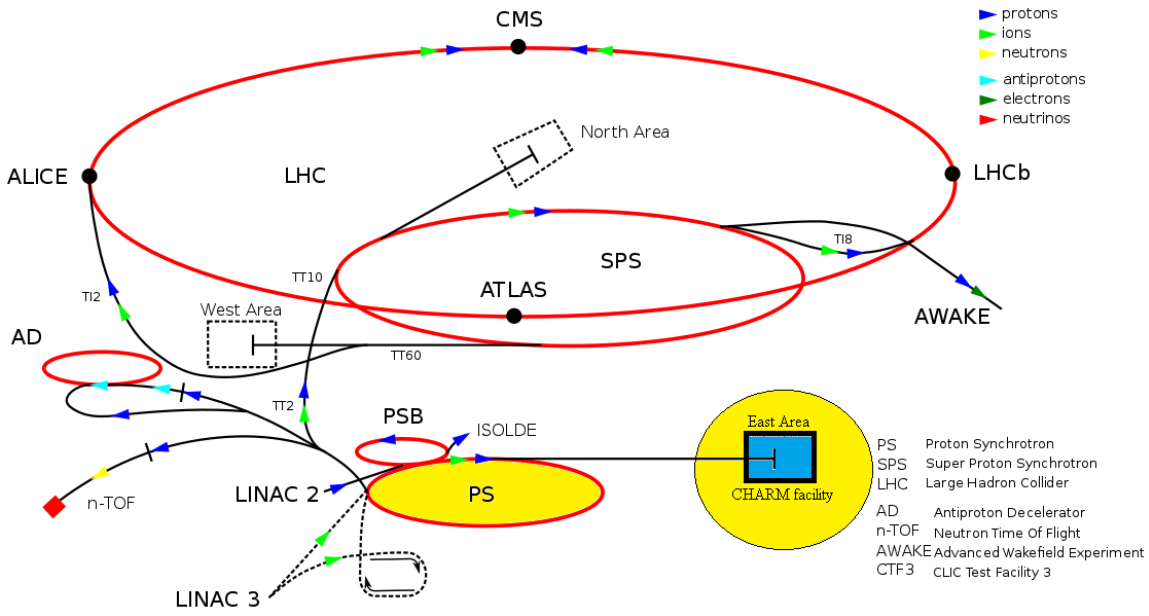


Figure 3. 14. The CERN accelerator complex. CHARM location, source [THO16].

At CHARM, input arrives at a 24 GeV proton beam from the PS, which can be directed to a number of beam lines to various physics experiments. The CHARM facility is located at the end of the T8 beam-line in the PS East Area Hall. Figure 3. 15 shows a screenshot from the 3D drawing of the PS East Area Hall in which CHARM facility is located in the southern part of the hall.

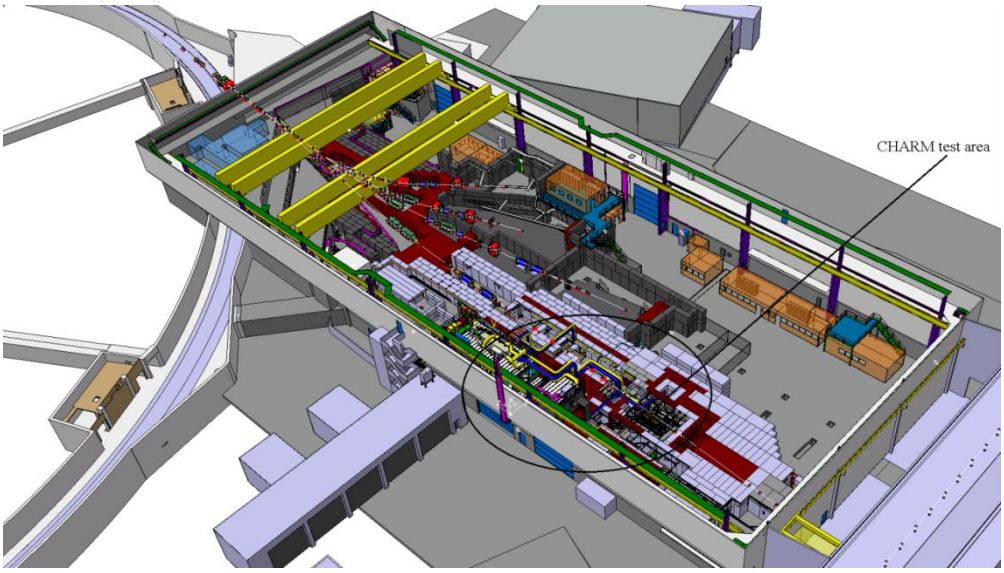


Figure 3. 15. The PS East Area Hall. CHARM facility. (source [THO16])

The CHARM facility has two main rooms, a preparation room, and a control room, in addition to a buffer-area for storage post-test irradiation. Figure 3. 16 shows a draw of the beamline and surrounding areas. The preparation room has space for users to make dry-runs of their test setup, whereas the control room is where the control and monitoring equipment for users is installed during their tests. The preparation room has the same components and racks which are in both control room and the irradiation room, (also called CHARM test area). Therefore, that allows simulating the real situation of communication between the control room and the radiation area. The CHARM test area has been built with the sole purpose of performing electronics testing.

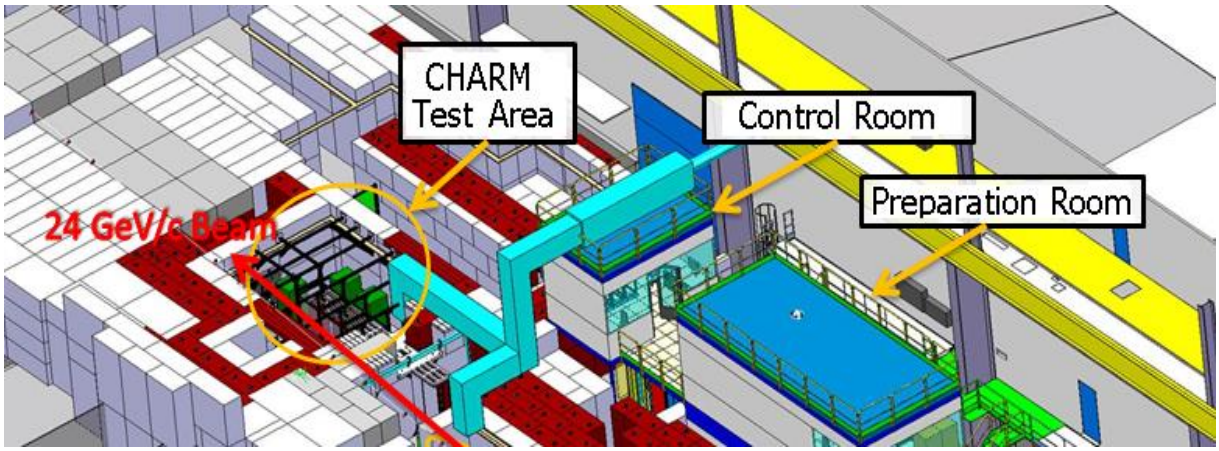


Figure 3. 16. A 3D Catia drawing of the CHARM facility, showing the different areas. (source [THO16])

The intensity within the radiation field can be varied by choosing different *targets* where the beam can be directed during the operation. Those can be copper, aluminium or aluminium with holes. The copper target generally gives the highest dose and particle fluences; the aluminium with holes target gives the least dose compared to the other targets. It is possible to run the beam measurements without the target, getting a test in a 24 GeV proton field [THO16]. So, the radiation environment inside the CHARM area comes to originate from the beam line interacting in the target. Furthermore, there are 4 layers of *shielding* installed in the middle of the test area which can be moved in or out of place to adjust the radiation field.

At test area one typically sees hadrons (protons, neutrons, pions and kaons), leptons (electrons, positrons and muons) and photons (x-ray and gamma). They range in energy from near primary beam neutrons and protons at 24 GeV, to thermal neutrons from the test area wall scattering at <1 eV [THO16].

Figure 3. 17 shows a simulated spectrum for the SEE-relevant hadrons at an LHC-like test location at the CHARM test facility. It was simulated with an integrated particle physics Monte Carlo simulation package used in high-energy experimental physics applications called FLUKA.

Depending on what particle types, energies, and fluences we interested in, it is possible to set the test setup in different test positions within CHARM test area, so that it can either be directly in the proton beam, behind shielding or at various angles and distances from the target . There are a total of 13 possible rack positions, which will be referred to as ’r1’ to ’r13’. Therefore, by varying the *target*, *shielding* and *position* of the test device, a large number of radiation fields can be achieved.

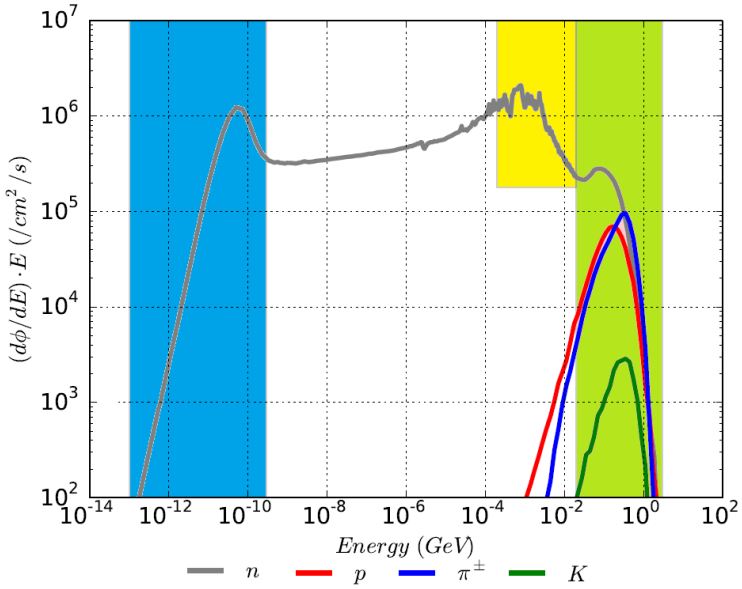


Figure 3. 17. FLUKA simulated lethargy spectra for the SEE-relevant hadrons at CHARM test facility (source [GAR14]). The different shaded regions represent approximately the thermal neutron (blue), intermediate neutron (yellow) and HEH fluxes (green),

3.2.2 High Energy Hadron (HEH)

As it has been seen in section 3.1, in addition to neutrons or protons, other hadrons as Kaons (K±), pions (π±) or even muons(μ), with energy higher than a few MeV can deposit a sufficient amount of energy in the silicon through indirect ionization and cause SEEs.

The radiation damages on electronics, in the context of a high-energy radiation field, such as the atmospheric environment or high-energy accelerator radiation fields described above are caused in greater proportion by high-energy hadrons (HEH, defined as hadrons above 20MeV).

An HEH test was set in CHARM to characterize the DUT in a mixed field and higher than 20 MeV energies. The SEE rate in an HEH mixed-field is dominated by indirect energy deposition events produced by nuclear interactions between the hadrons and the sensitive volume and its surroundings [GAR14].

To calculate the effects of the mixed-radiation field at CHARM in a similar way as it was done for other fields, it is necessary to define an equivalent particle. This is because it is not possible to discriminate between the effects of the fluences of different particles, which are in a variety of types and have different energies and varying impacts on the electronic components.

The 20 MeV threshold to consider hadrons as HEH is chosen since this value corresponds to an energy for which SEEs generation can be assured. A similar value called the high-energy hadron equivalent (HEHeq) is chosen to calculate the hadrons cross section equivalent. The difference between HEH and HEHeq depends on the way the fluence of hadrons below 20 MeV is calculated. For HEHeq, a Weibull function [DAN14] is used to model the response of a typical SRAM used for SEU detection. It is assumed to be more accurate than defining a minimum threshold (as in HEH definition, for defining the total HEH fluence).

The data from HEHeq and fluxes are proportionated by CERN Engineering Department and the Radiation to Electronics (R2E) group, using the intensity at the proton beam before interacting in the copper target and multiplying it by a conversion factor calculated with FLUKA simulations. To validate the accuracy from the fluence data, there are detectors in the vicinity of the samples being tested, which confirm the existence of massive samples produced by another experiment or if the beam, for any reason, did not completely interact with the target.

The period used in the CHARM campaign with the SRAMs under test was from 15/06/2016 to 12/07/2016 (22 days). To obtain neutron energies and fluxes as close as possible to an atmospheric environment, the DUT was located in the corresponding rack which was characterized by the spectrum shown in Figure 3. 18. During that period, the fluence registered was less than $9 \cdot 10^{10}$ HEHeq/cm^2 per week.

The DUT was restarted to have different tests to different TIDs and three tests were stored. These tests range from 3 hours, 90 hours and after these 90 hours another one of 12 hours, which correspond to a total fluence of ~$2 \cdot 10^9$ HEHeq/cm^2, ~$5 \cdot 10^{10}$ HEHeq/cm^2 and ~$6.5 \cdot 10^9$ HEHeq/cm^2 respectively. The Figure 3. 19 shows the HEHeq fluence estimated every 15 minutes inside the CHARM radiation room during the irradiation period which reached 11.5 days.

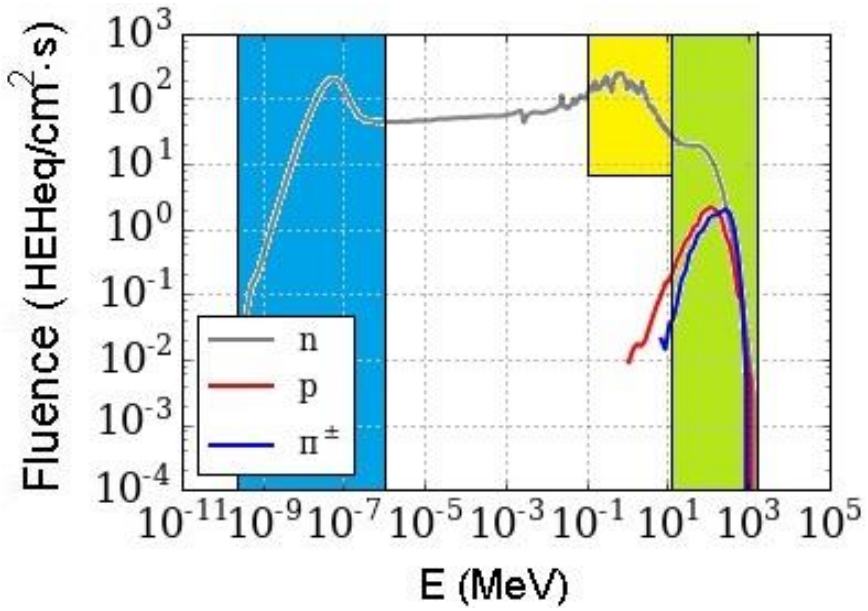


Figure 3. 18. Spectra for the SEE-relevant hadrons at CHARM test facility in the rack correspondent to the irradiation for the DUT. The different shaded regions represent approximately the thermal neutron (blue), intermediate neutron (yellow) and HEH fluxes (green).

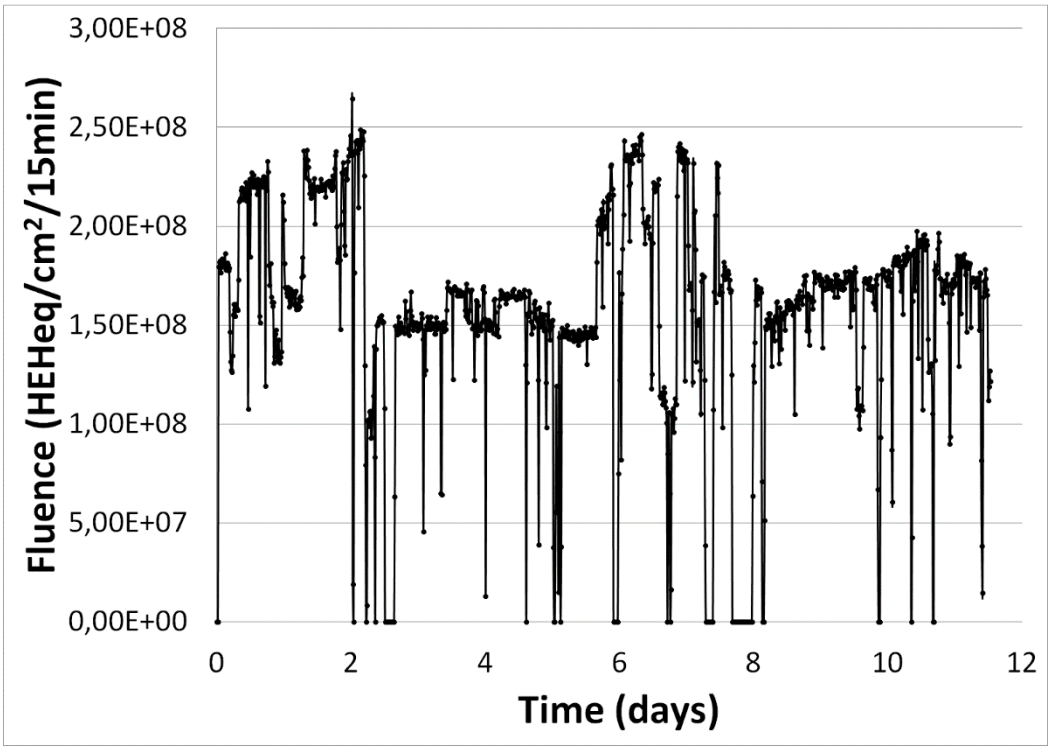


Figure 3. 19. HEHeq fluence estimated inside the CHARM radiation room.

Inside the radiation room, the DUT was situated in air as shown the Figure 3. 20.

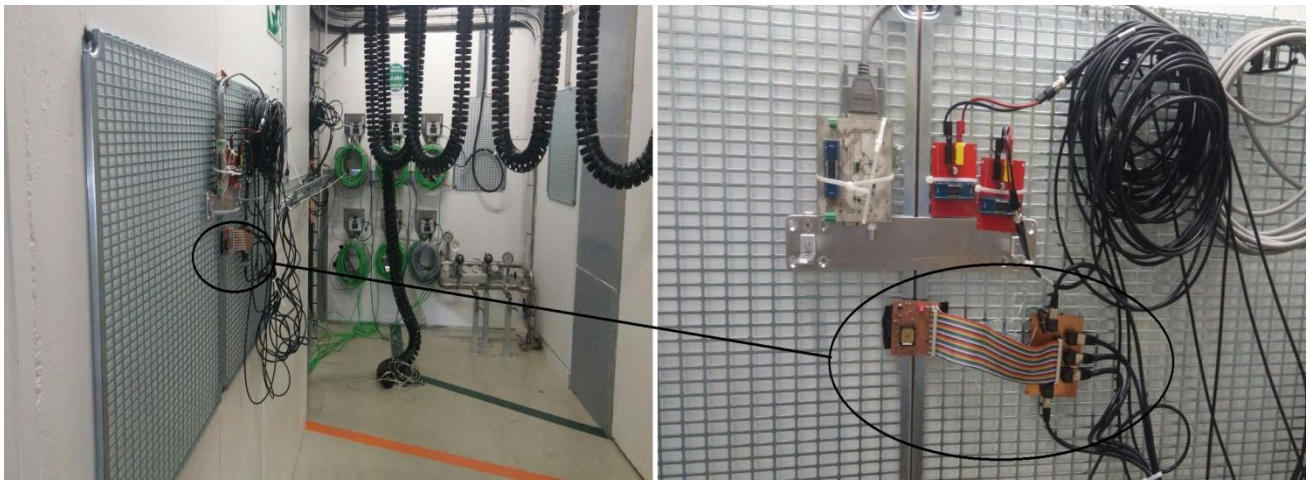


Figure 3. 20. DUT and Ethernet cables in CHARM radiation room.

The DUT is mounted on a test board, which is connected to an FPGA board but, in this case, Ethernet cables and PCBs are used as connectors between chip and FPGA. The laptop and FPGA are located in the CHARM facility control room via Ethernet-USB connection (Figure 3. 21).

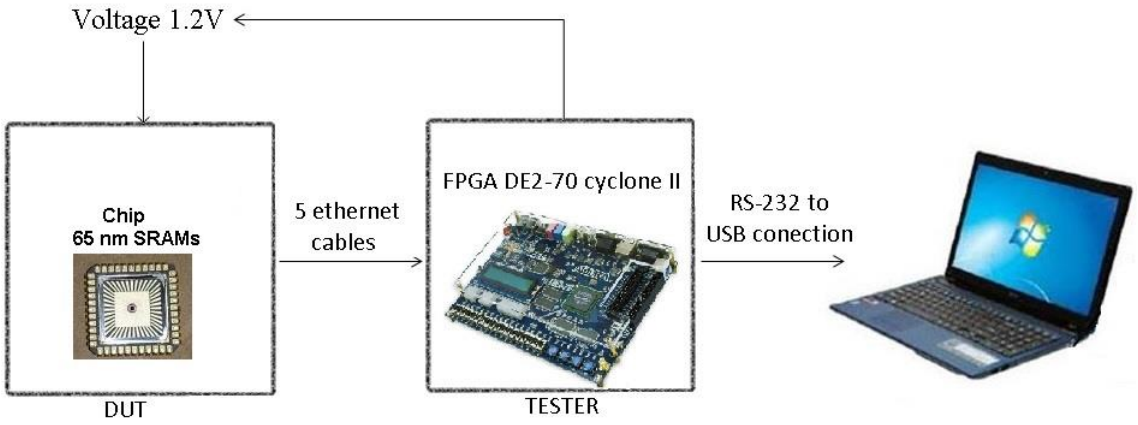


Figure 3. 21. Test Setup for the SRAM at CHARM.

The chip voltage supply and the test board are fed by the FPGA. The test board is read by a laptop from which it is possible restart and control the measurements.

CHAPTER 4

ANALOG-TO-DIGITAL CONVERTERS

Analog integrated circuits are also susceptible to SEEs, although little information about its effects has been reported. Analog-to-Digital (A/D) Converters are almost ubiquitous in modern SoCs, since they are required to transform signals from the analog world to the digital processing domain. This is true for consumer electronics but also for space applications. Any sensor acquisition chain, any scientific instrument requires at some point an A/D converter. Similarly, wireless transceivers also contain A/D converters to safely send data.

This chapter treats about the radiation effects in Sigma delta modulators, we will analyse the effects caused by SETs in the modulator long-term stability, and, identify its sensitive nodes.

4.1 Sigma delta modulators

There are many different A/D topologies with their particular strengths and drawbacks, as consequence of complex trade-offs between conversion speed, resolution, power consumption and silicon area. The effect of single events on A/D converters is obviously a concern for space applications, but the studies that can be found in the literature are usually not architecture specific [TUR96, SCH01]. Most of the research effort seems to be steered at the definition of validation protocols [BER10].

In the field of instrumentation, one of the most relevant architecture is probably the A/D converter based on the Sigma-Delta modulator (ΣΔM). The ΣΔM is the analog part of the Sigma-Delta A/D converter. It relies on relatively low complexity analog hardware, which brings good technological scaling capabilities. Power consumption can be much reduced since a large part of the processing is done by a digital filter. But most of all, ΣΔM converters usually exhibit very high linearity, ensure monotonicity and achieve low noise performances. All of these characteristics are of interest in high-precision instrumentation solutions. However, ΣΔ modulators have memory. As a matter of fact, they can be seen as an analog Finite-State Machine with feedback. And this combination of memory and feedback naturally leads to stability concerns.

The impact of SEE on continuous-time ΣΔ modulators has been reported in [LEU04]. The authors end up comparing the outcome high-level simulations of a database of modulators considered as black-boxes. Their approach was very generic, and the objective was to draw universal conclusions. However, they fail to point out the critical phenomena that can lead to serious performance degradation: instability.

What it is shown in this chapter is that, for high-order modulators, a Single-Event Transient may trigger instability and lead to long-lasting catastrophic conversion errors, even for switched-capacitor implementations. The validation is carried out by simulation of an existing prototype implemented in a 90 nm CMOS technology [ASG12]

The chapter is organized as follows: Section 4.2 gives a brief overview of the principles of operation of ΣΔ Modulators and stability concerns. Section 4.3 shows how a SET can modify the internal state of the modulator and drive it into instability depending on the ΣΔM internal state. Finally, Section 4.4 and 4.5 draw the results and conclusions of the study.

4.2 Principle of operation of the ΣΔM

Figure 4. 1 presents a simplified diagram of a ΣΔ A/D converter. On the left hand, it is found the modulator, which samples the input signal at a high frequency and converts it into a low-resolution (possibly only one bit) digital bit-stream. On the right hand, a digital filter removes the quantization noise located out of the band of interest, leaving the signal of interest almost unaltered.

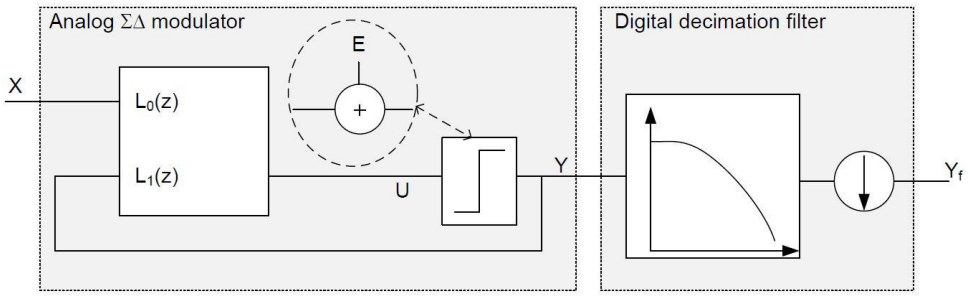


Figure 4. 1. A generic diagram of a ΣΔ converter.

The modulator is schematically represented by a loop filter and a coarse quantizer. The quantizer takes the output of the loop filter (*U*) and convert to an n-bit digital signal (*Y*). The feed-back in analog ΣΔ modulator performs the inverse function of the analog to digital

converter (quantizer) and converts the n-bit digital code to an analog voltage or current, closing the Sigma-Delta loop (see Figure 4. 1). In practice, this memoryless single quantizer would be implemented with a coarse ADC and DAC combination.

So, based on a linear model, $L_0(z)$ and $L_1(z)$ represent the the Z-transform in the loop filters (into a complex frequency domain representation) for the discrete time input signal (X) and for the output signal (Y) respectively. A common practice to study the frequency behavior of the modulator is to linearize the coarse quantizer. In a first order approximation, it can be modelled by an additive white noise (E), whose power is equal to the quantization noise ($\delta^2/12$, where delta is the quantization step). If the quantizer has a single bit resolution, it may be necessary to consider that it has an equivalent k, but it is still memoryless. The loop filter, however, does introduce memory. Its output depends on both the converter input signal X and the quantizer output Y, forming a feedback path.

The performance of the ΣΔM is affected by the quantization noise introduced by the quantizer as a summing perturbation. The output of the modulator depends on the input X and the quantizer noise E as seen in equations 4.1 and 4.2. The signal transfer function, STF, and the noise transfer function NTF, can easily be developed as shown in equations 4.3 and 4.4.

$$\boldsymbol{Y = L_0(z) \cdot X + L_1(z) \cdot Y + E} \qquad \textbf{4. 1}$$

$$\boldsymbol{Y = STF(z) \cdot X + NTF(z) \cdot E} \qquad \textbf{4. 2}$$

$$\boldsymbol{STF(z) = \frac{L_0(z)}{1 - L_1(z)}} \qquad \textbf{4. 3}$$

$$\boldsymbol{NTF(z) = \frac{1}{1 - L_1(z)}} \qquad \textbf{4. 4}$$

Ideally, the STF should be close to one in the signal bandwidth, while the NTF should be as low as possible. In that way, the quantization noise produced by the coarse quantizer is pushed out of the signal bandwidth (typically to high frequency for a low-pass modulator) and can be efficiently filtered out by the subsequent digital filter.

This expression is generic and operates for any implementation of loop filters (feedback). Considering the quantization noise as an independent white noise (which in fact is a strong approximation), it is possible to linearize the design and place the poles and zeros of the STF and NTF to optimize the filters [SCH05].

The simple linear approximation implies that the STF(z) and NTF(z) should have their poles located within the unit circle to ensure stability. This could easily be solved by proper filter design. Unfortunately, the linear approximation of the quantizer does not hold since the quantization error is highly correlated to its input. This correlation is particularly relevant if the quantizer is overloaded (i.e. if its input is out of the quantization range).

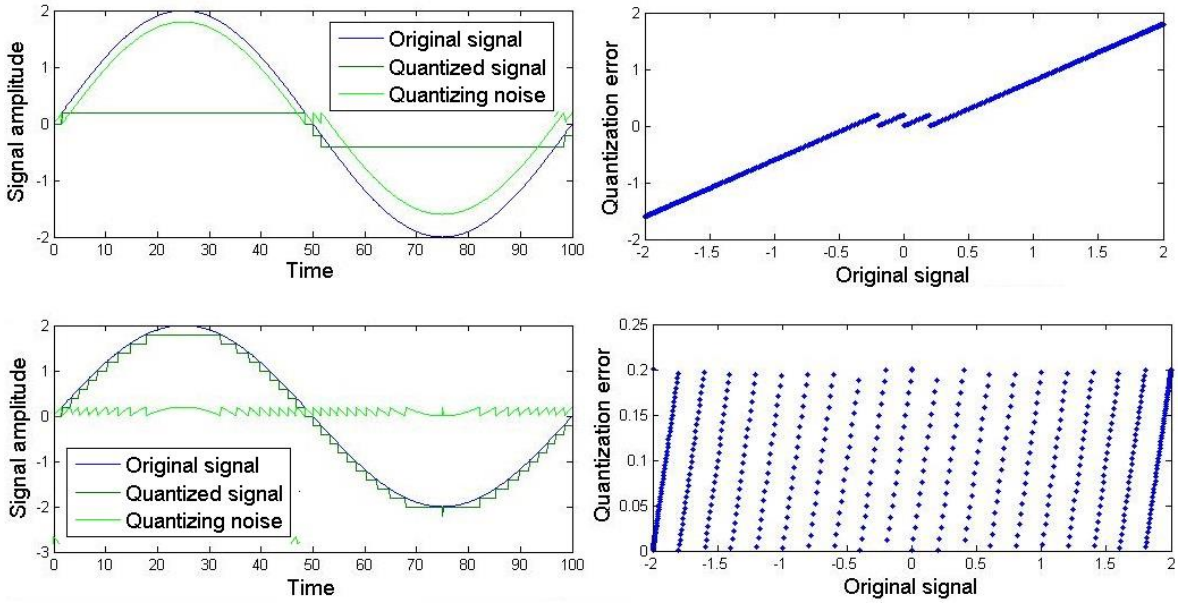


Figure 4. 2. On the left) Original signal, quantizing signal and quantizing noise for two different quantization steps (a sinus outside of the quantization range, overload, and another sinus within the range). On the right) Quantized signal at function of original signal for both situations.

For single-bit quantizer, it is a common practice to consider a variable effective gain k before the quantizer linearization. As a result, it is possible to study the locus of the STF and NTF poles with k to infer stability regions. The effective value of k can be estimated as show the equation 4.5.

$$\boldsymbol{k \approx \frac{E[|U|]}{E[U^2]}} \qquad \textbf{4. 5}$$

A more accurate approximation is proposed in [ARD87]. However, in both cases, it remains signal dependent.

For multi-bit quantizers, there is no effective gain unless the quantizer overloads. In [KEN93], a general rule is derived that states that stability is ensured for modulators with M quantization steps (i.e. M+1 quantization levels) for any input signal such that,

$$ax|u(n)| \leq M + 2 + \|ntf\|_1 \quad \textbf{4. 6}$$

$$\|ntf\|_1 = \sum_{n=0}^{\infty} |ntf(n)| \quad \textbf{4. 7}$$

where *ntf* is the inverse z-transform of the Noise Transfer Function NTF. Notice that the input *u* is normalized to one Least Significant Bit (LSB) and the full-scale is thus equal to M. For an Nth order differentiating NTF, it is found that

$$\left\|\left(1 - z^{-1}\right)\right\|_1 = 2^N \quad \textbf{4. 8}$$

A 4th modulator with 5 quantization levels would, in this case, have a stable input range of at least 50% of full scale.

4.3 Architecture of the 4th order ΣΔM

In this chapter, we used a switched-capacitor Tunable Center Frequency 4th order Cascade of Resonators with Feed forward (CRFF) based Sigma delta modulator shown in Figure 4. 3, and reported in [ASG12]. The modulator, designed at the National Center of Microelectronics in Seville (IMSE-CNM), was implemented in UMC 90 nm CMOS process, and it was capable of handling signals of up to 1 MHz bandwidth with tunability range of 0 to 22 MHz for a sampling rate of 100MHz. Increasing the sampling frequency to 200 or 300 MHz the tunability was increased to 44 MHz and 66 MHz respectively.

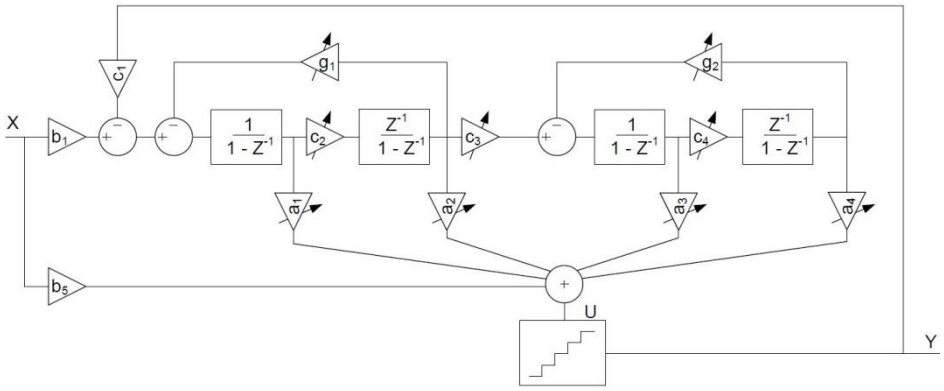


Figure 4. 3. 4th Order CRFF Based Sigma Delta Modulator.

It implements a single loop architecture that consists of two resonators and feed forward paths. Each resonator was made up of one Forward Euler (FE) and one Backward Euler (BE) integrator. The number of quantizer's levels was 5.

The variable notch in noise shaping is obtained by optimizing the zero placement of the Noise Transfer Function, employing a different set of coefficients for each center frequency. The two feedback coefficients (g_1 and g_2) across the resonators can be tuned to a get a desired notch in the NTF.

A direct feed forward path from the input X to the quantizer input guarantees unity STF. This way, only error signal is processed by the internal integrators. This strategy relaxes the swing requirements of integrators. To further scale the input of the integrators, coefficients c1 to c4 can be employed. In order to keep NTF and STF constant, feed forward coefficients a1 to a4 also need to be adjusted according to the values of the input coefficients of the integrators.

All the variable coefficients are implemented using digitally programmable capacitors. As a result, the modulator can be reconfigured either as a low-pass or as a bandpass analog to digital converter with a tunable notch frequency and an optimized loop-filter zero placement. The circuit, incorporates diverse architecture and circuit level strategies to adapt its performance to different sets of specifications with a variable sampling frequency of 100 and 200 MHz and scalable power consumption.

4.4 Sensitivity to radiation

The idea is that a SET can disturb the state of the ΣΔ modulator. The hypothesis is that any charge injected into the virtual ground of an Operational Transconductance Amplifier (OTA) is integrated by the feedback capacitor. In an implementation based on a switched capacitor, electrical charge could be injected into the virtual ground through any switch connected to that node. It is important to emphasize that the effect of a single event would be "permanent" since the charge would be stored in the feedback capacitor. If the charge injected by radioactive particles from the environment is small enough, it would only contribute to the noise at the output, but higher values can drive the ΣΔ device into an unstable output state.

It is usual to find capacitance values below 1pF. In our particular prototype, the feedback capacitance value was actually 800 fF for the first three integrators and 400 fF for the last one.

In this way, an injected charge of 400 fC would lead to a step of 500 mV in the first integrator output.

In this particular case, since the important quantity is the total injected charge and not the instantaneous current value, it is possible to assume that the exact pulse shape is not relevant whenever it occurs within the sensitive half clock period (in the order of 5ns for our case of study).

Figure 4. 4 shows electrical simulation results of the first integrator output for four different current pulses injected into the virtual ground: long and short square and double exponential pulses. However, the total injected charge was the same for the four pulses (Q_{pulse} = 300 fC). For the double exponential pulses, a 1-to-10 ratio between the rise and the fall time constants (10ps and 100ps respectively) was considered, as usual in the literature [MAV07]. On the top of the graph, it is shown the clock signal that drives the integrator and the shape of the pulses is displayed on the right-hand side. It can be observed that the evolution of the integrator is similar in all the cases, validating our assumption that the exact pulse shape is irrelevant for the charge injection in the virtual ground. In addition, it can be verified that the charge is effectively integrated, and the output is thus changed permanently and experiments a change of about 350 mV, very close to the expected one (300fC/800pF=375mV). The difference is apparently due to the finite settling capabilities of the OTA. The actual value of the long-term perturbation thus depends on the exact instant at which the SE pulse occurs. However, this result brings the possibility to use event-driven high-level simulations to study the possible long-term effects at least from a phenomenological viewpoint. Obviously, an evaluation of the probability of occurrence of such SEE would require an experimental study.

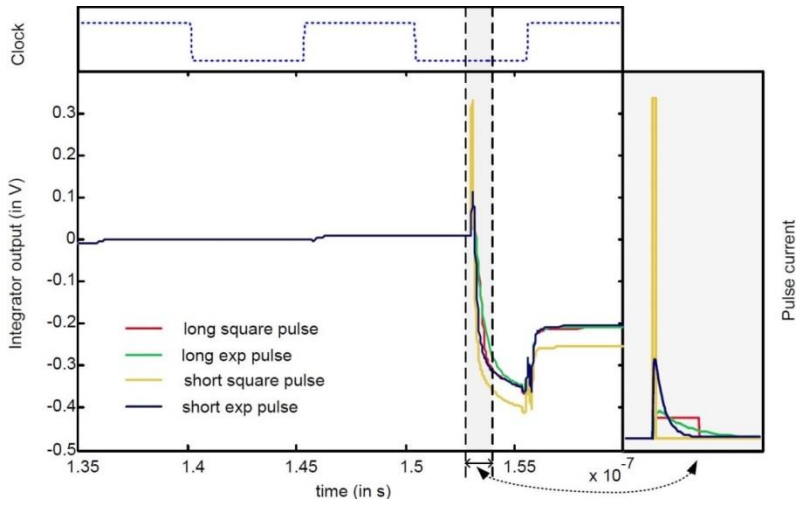


Figure 4. 4. Integrator response to 4 different current pulses injected into the virtual ground. The injected charge is 300fC.

4.5 Impact of sets on ΣΔM stability

In a first attempt to show the potential impact of SEE, a Matlab Simulink model of the ΣΔ modulator has been used to perform high-level simulations. In order to emulate the injected charge, single pulses have been injected at the input of any of the three integrators. The height of the pulse in volts is defined in equation 4.9, where Q is the injected charge (proportional to the LET), C is the feedback capacitance and FS is the modulator full-scale defined by the voltage references, introduced for normalization purpose.

$$h = \frac{Q}{C \times FS} \qquad \textbf{4. 9}$$

Visual inspection of the output of an integrator is a straightforward way to detect a possible instability in the modulator. However, a more systematic criterion should only rely on the modulator output. It is proposed to compare the output power spectrum before and after pulse injection. More concretely we simulated 3000-time instants. The pulse was injected at t =1000, a Fast Fourier Transform was computed on the first 1000 samples (normal behaviour before pulse), a second one was computed on the last 1000 samples (to check a possible faulty behaviour after the pulse). The 1000 samples in the middle of the acquisition registers were discarded as data can be affected by transient behaviour induced by the SEE perturbation. By doing so, it was given some time to the modulator to recover its regular operation mode after the current pulse. Otherwise, some stable modulators with a significant recovery transient could be tagged as unstable. The maximum of the power spectra difference is our instability signature: above a certain threshold (defined by the spectrum repeatability with no injection), the modulator is considered unstable.

Figure 4. 5 shows two examples in which the modulator is in low-pass configuration (with the notch configured at DC). The simulated output of the Fast Fourier Transform (FFT) at the output before and after pulse injection are compared. In Figure 4. 5.a, a pulse of 10% of the full-scale is injected and the modulator recovers its normal behavior after the perturbation, while in Figure 4. 5.b the amplitude of the injected pulse is set to 50% of the full-scale and the system becomes unstable.

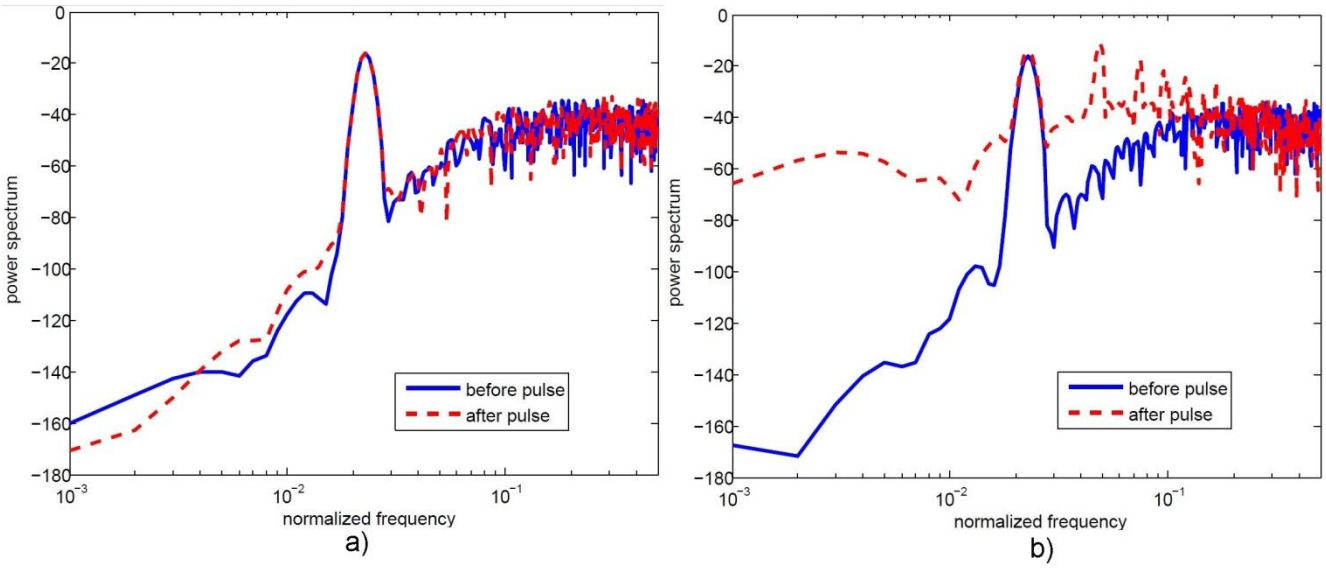


Figure 4. 5. FFT Examples: a)DC Stable and b)DC unstable

Figure 4. 6-a shows the instability probability for the modulator in low-pass configuration (with the notch configured at DC), as a function of the pulse height for three different integrator saturation levels (normalized to the full-scale). The probability was estimated simulating 100 modulator instances with a sine wave input of random amplitude (up to 50% of full-scale), frequency and phase. This is done because pulse-induced instability may be dependent on the actual modulator state at the injection instant.

It can be seen that for the threshold for instability triggering is around 40% of full-scale. However, when the integrators are set to saturate at full-scale, it appears that in some cases the modulator is able to recover from instability. This effect is more pronounced in modulators in bandpass configuration. Figure 4. 6.b shows the same plot obtained for a notch at 10% of the sampling frequency. For a saturation set at full-scale, the occurrence of instability is very low, for a saturation level set to two times the full-scale, loss of stability is much more probable though not systematic. Notice that the trigger for instability is also higher (roughly at 80% of the full-scale).

The effects of a single event transient in the modulator can also by analysed by transient analysis performed by electrical simulations at transistor level. These simulations are much more time-consuming than high-level simulations, and it is thus impossible to explore a large number of operating conditions.

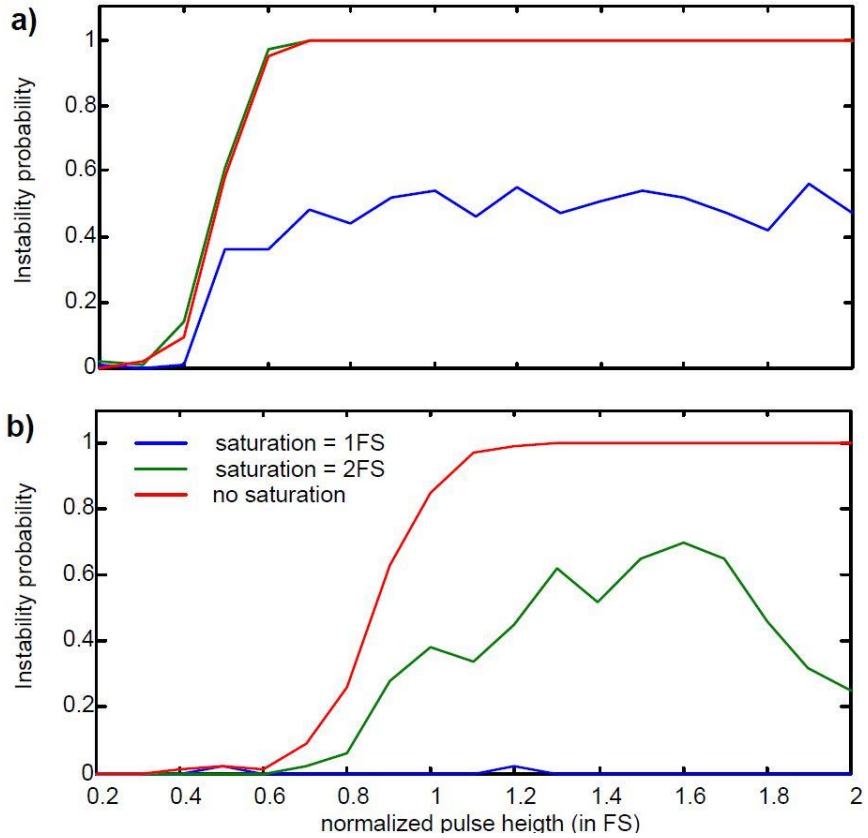


Figure 4. 6. Probability of instability as a function of the injected charge, for three different values of integrator saturation for a) a low-pass modulator notch at DC and b) a band-pass modulator with a notch at 10% of the sampling frequency.

Transient simulations have been performed at transistor level using Spectre as electrical simulator, and the transistor models provided in the UMC 90 nm physical design kit. Two ΣΔ modulator configurations have been analysed: one with a notch configured at DC, and a second one with a notch configured at 13MHz. The sampling frequency is set to 100 MHz so the semi-period is 5 ns, much larger than the duration of the injected current pulse. As before, the current pulse has been modelled as a double exponential with rising and falling time constants of 10 ps and 100 ps respectively. A charge of 500 fC was injected at the simulation time of 2 μs. The total simulation time is 4 μs.

As it can be seen from the integrator outputs displayed in Figure 4. 7, the first configuration (notch located at DC) becomes unstable after the perturbation produced by the SET. Indeed, the variation range of the integrator is clearly altered (the stable scale can be appreciated in the zoom inset). However, for a notch configured at 13MHz, the injected pulse leads to a noticeable abnormal transient, but the modulator recovers its normal output range after roughly 500ns (i.e. 50 clock periods).

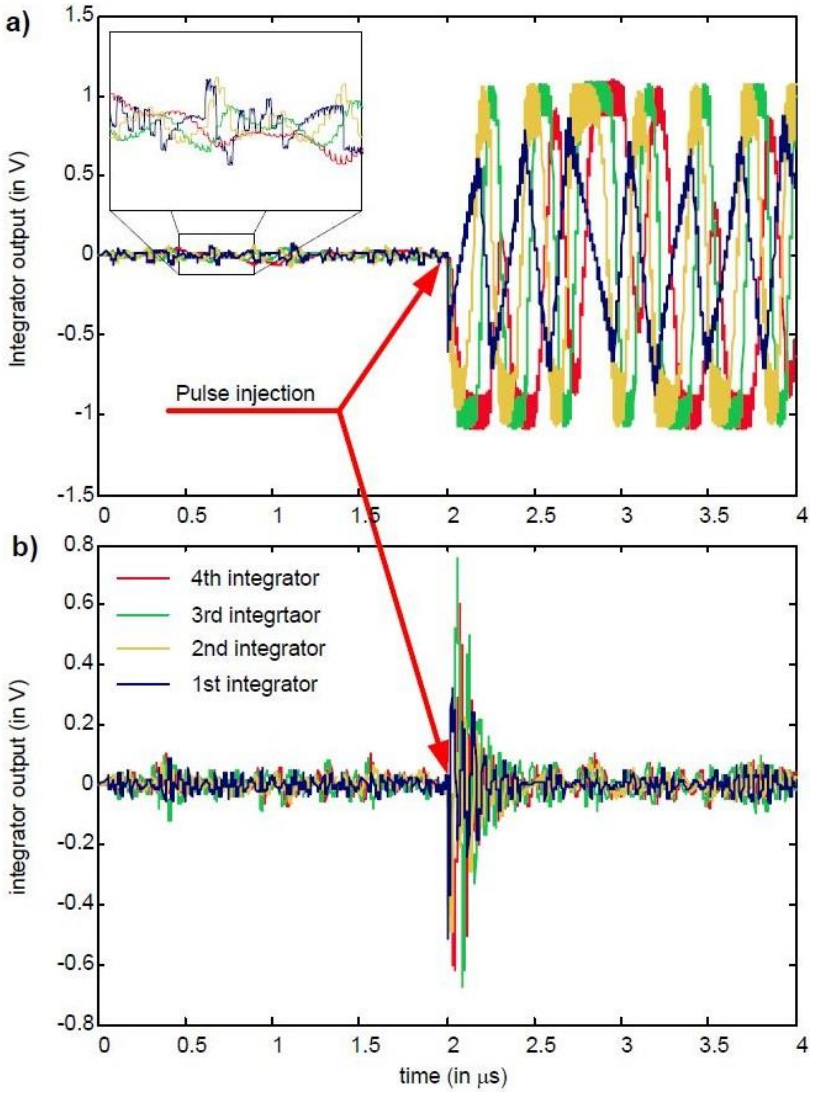


Figure 4. 7. Integrators output for transistor-level transient simulation of the ΣΔ modulator presented in [ASG12]. A current pulse is injected at 2μs and deposit 500fC. a) for notch configured at DC, b) for a notch configured at 13MHz.

It can thus be concluded that high-order single-loop modulators are only conditionally stable to SET events. Hence, this effect shall be taken into account for space applications. Several corrective actions can be envisioned:

- At system-level: rule-out the use of ΣΔ modulators. This is a quite drastic option, but other ADC architecture with no feedback shall only produce transient errors and then recover.
- At sub-system level: high order modulators can be achieved using a cascade topology of low-order sections (MASH architecture [SCH05]) which are inherently stable.
- At circuit-level: it is possible to add some kind of auxiliary circuitry that detects unstability (like a window comparator at the output of the integrators to detect overranges) and reset the integrators if necessary.

CHAPTER 5

STATIC RAM AND 6T-8T CELLS

Static Random Access Memories (SRAMs) are found in many digital systems, playing a crucial role in a wide variety of applications. This is because SRAMs are compatible with the standard CMOS technology used for the implementation of integrated circuits [ZHA09]. SRAMs are typically used when short access times as well as low power consumptions are required. One of the most widespread traditional applications is the cache memory and currently, with the emergence of multicore processors and systems on chip; the demand for integrated SRAM has increased [PAV08].

SRAMs also have drawbacks: they are volatile and they have a higher cost per bit than DRAMs; that is, its content is lost when its biasing voltage is switched-off, unlike to other types of memory such as flash memory.

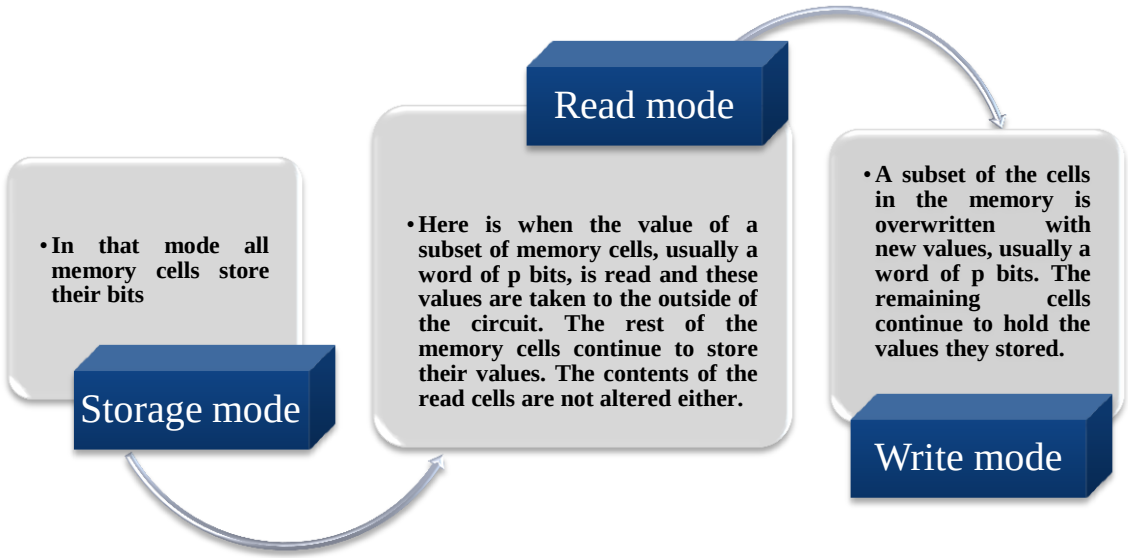


Figure 5. 1. Modes of operation of a SRAM

An SRAM memory is an element that is able to store N_b bits of information. These bits are usually structured in N_p words of p bits each ($N_b = N_p \cdot p$). The main element in an SRAM

memory is the SRAM cell (or bit-cell), which is capable of storing a bit of information in a latched structure. In addition, its content can be read or overwritten by a new one.

It is possible to understand the operation of a bit-cell by describing its three operation modes, Figure 5. 1.

The main goal of this thesis intends to study the effects induced by radiation in nanometer SRAM memories, especially to characterize an SRAM model designed at the University of Balearic Islands [TOR12].

Although the sensitivity of a cell to radiation can by described through their critical charge, a convenient parameter that can be computed by electrical simulation, the parameter that actually reflects the robustness of a memory against single event effects induced by radiation is the SER. There are some ways to correlate SER and critical charge, but the only way to get a measure of SER without depending on approximated models is exposing a memory to radiation fields.

5.1 SRAM bit-cell

Two topologies have been used for this work: the 6 transistors (6T) and the 8 transistors (8T) cell. The reason to choose the cell 6T is that it is currently the most used and can be considered as the standard topology. The 8T cell, although not so habitual, is increasingly used. For example, Intel® uses in some of its processors 8T cells at the level 1 and 2 cache (L1 and L2).

5.1.1 6T cell

A 6T SRAM cell consists of two nMOS pull-down devices (nMOS-I and nMOS-D in Figure 5. 2) and two pMOS pull-up transistors (pMOS-I and pMOS-D in Figure 5. 2) forming two feedback inverters and two nMOS transistors called pass transistors (TP-I and TP-D) which isolate the cell from the rest of the circuit during storage periods and allow access to the cell during reading and write operations. The pass transistors are controlled by the WL signal that is normally transmitted to the cells of the same row through the word-line (WL) line.

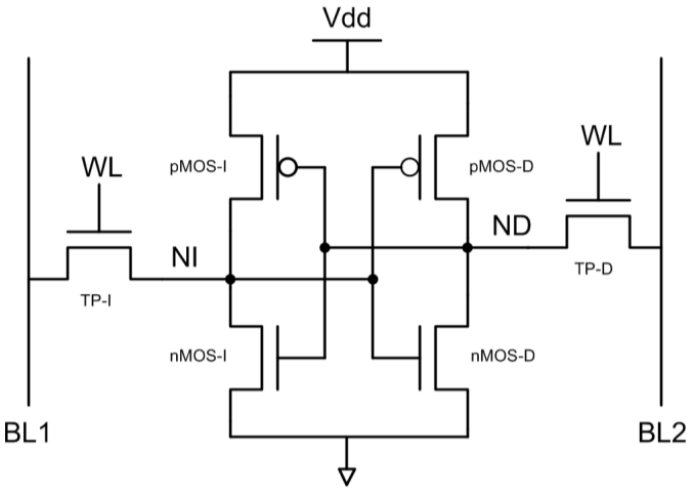


Figure 5. 2. 6T SRAM cell structure.

The two feedback inverters set the voltage values of the two internal nodes of the cell (ND and NI), so that, in a stationary state, one of these nodes is at a low level and the other at a high level, existing two possible states of the cell:

- ND at high level and NI at a low level

- ND at low level and NI at high level

One of these states will represent the logical value 1 of the cell while the other will represent the logical value 0.

Each of the internal nodes of the cell is connected through a transistor to a different bit-line (BL1 and BL2). These lines are common to a single column of cells and are connected through transmission ports to the reading and writing circuit. That is, the bit-lines are the intermediate nodes that are used to read and write the data into the cells.

The electrical characteristics of the 6T cell depend on transistor sizes. We will consider the following parameters:

- The ratio between the width of the pass transistors (nMOS), W_{step} and the minimum width that the technology allows (W_{min}).

$$\gamma = \frac{W_{step}}{W_{min}} \qquad \textbf{5. 1}$$

- The ratio between the width of nMOS transistors of the two feedback inverters (W_n) and W_{step}

$$\alpha = \frac{W_n}{W_{step}} \qquad \textbf{5. 2}$$

- The ratio between width of the pMOS transistors of the two feedback inverters (W_p) and W_{step}

$$\boldsymbol{\beta = \frac{W_p}{W_{step}}} \qquad \textbf{5. 3}$$

5.1.1.1 Write process in a 6T SRAM cell

The process of writing a new value in a 6T SRAM cell begins by taking the bit-lines to the voltage levels to which it is desired to force the internal nodes in the cell (each bit-line is connected at a node through its pass transistor). We will assume that the node ND is at a high level and NI at a low level, and that it is desired to write the inverse value (see Figure 5. 3). Subsequently, the WL signal is activated and the ND node voltage begins to decrease at a rate that depends on the relative strengths of its pass transistor and the pull-up transistor (β parameter). Meanwhile, the voltage at the NI node begins to increase due to the influence of the bit-line to which it is connected (high level), in this case, the transistors involved are the step and the pull-down (α parameter). At first, the feedback from the cell inverters opposes this change, as the cell is intrinsically stable.

However, if the relative strengths of step transients (which change of state) and the pull-up and pull-down of the cell (which oppose the change) are appropriate, the voltage levels of the internal nodes of the cell will reach a level in which the feedback in the cell will start to change of state. From this moment on, the writing process of the cell is triggered irreversible. It may also happen that, if the relative strengths are not adequate, at the end of the write period and deactivate the pass transistors, it has not reached the point where the feedback of the cell supports the change of state. In this case, if this happens, the cell feedback will retrieve the original voltage values from the internal nodes of the cell, and the write will have failed.

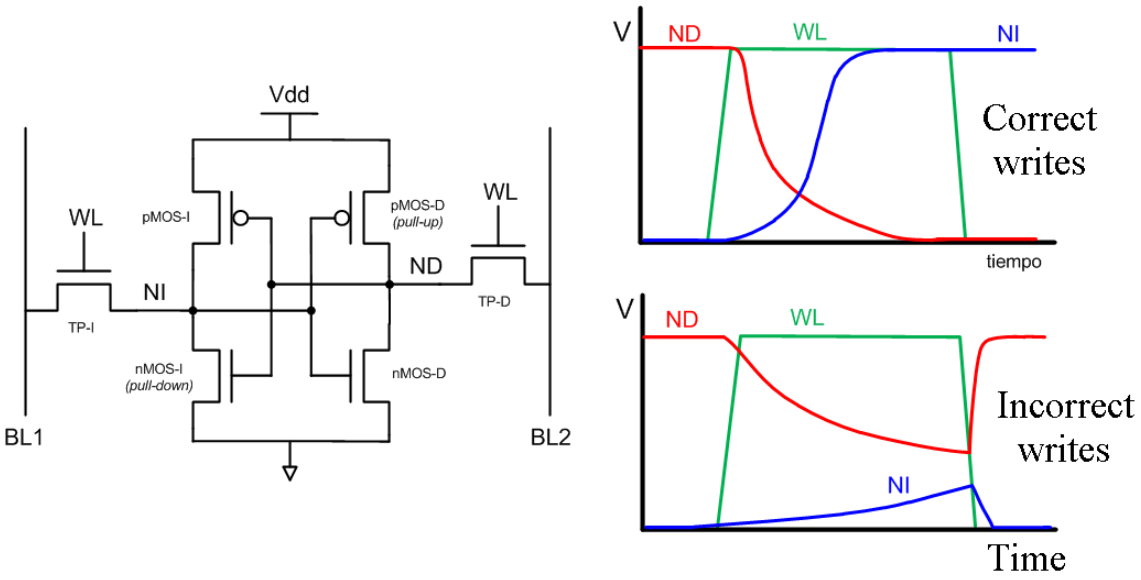


Figure 5. 3. Schematic representation of a correct write process and a failed write process in an SRAM 6T cell.

5.1.1.2 Read process in a 6T SRAM cell

Before starting a cell reading, both bit-lines are initially set to V_{DD}. It is assumed that the ND node is at a high level and NI at a low level (Figure 5. 4). When the WL signal is activated, the pass transistors connect the internal nodes of the cell to the bit-lines. Then the bit-line that connects to the NI node begins to discharge through the pass transistor and the pull-down transistor. However, the other bit-line will not be appreciably discharged since it is practically at the same voltage as the node ND. This difference of discharges between bit-lines is what allows that the contents of the cell can be read by the read circuit.

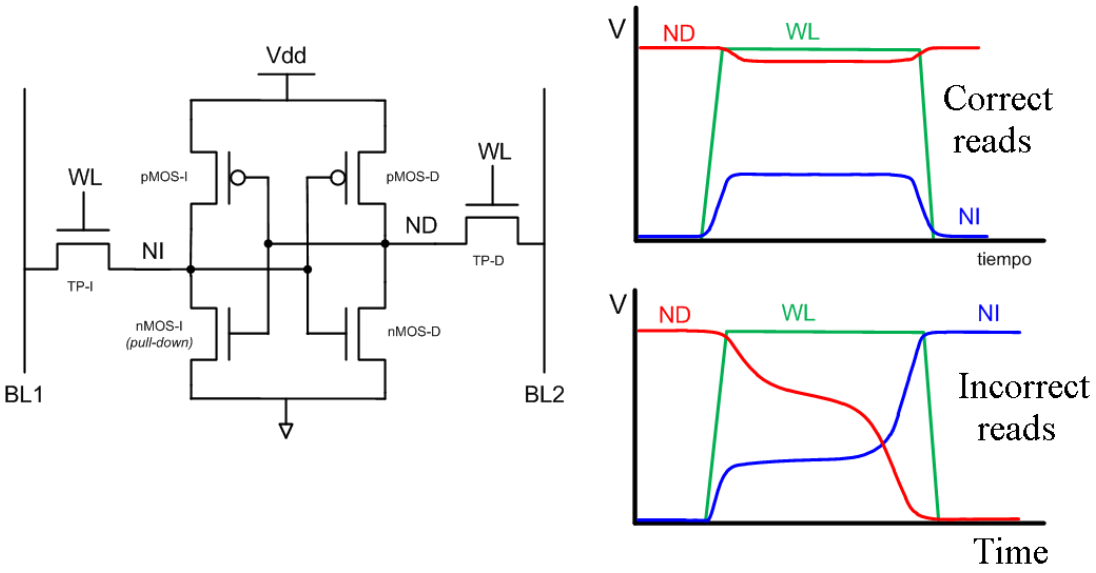


Figure 5. 4. Schematic representation of a correct read process and a failed read process in a SRAM 6T cell.

During the discharge of the bit-line, the low-level node (NI) sees its voltage increased, whereas the node ND is practically unchanged. The magnitude of the NI perturbation depends on the relative strength of the step and pull-down transistors (α parameter). If the disturbance is small, the actual feedback from the cell will be able to maintain its state. However, if the disturbance exceeds a certain critical value, the feedback from the cell will not be able to counteract it, and a change in stored value will occur. Transistor sizing must prevent this type of readings that corrupt the bit saved in the cell, to guarantee a non-destructive read, α is usually comprised between 1.5 and 2.5.

The read circuit has access to two bit-lines, one that is discharged and another one that it does not, therefore, can be differential.

5.1.1.3 Minimum size 6T SRAM cells

Bit-cell area is reduced using minimum size transistors (α=β=γ=1). Unfortunately, this can lead to read stability reduction as a side effect (note that bit-cells are sufficiently stable in hold mode even with α =1). Despite that, there are alternative ways to avoid read failures while keeping α=1. In multi-threshold-voltage technologies, it is possible to guarantee cell stability by selecting the threshold voltages for each transistor in the bit-cell [ZHU11]. A second alternative is the use of read assist circuits based on word-line voltage modulation. This second option does not involve a permanent design setting and can be applied and adjusted according to the needs of each operation scenario. The read assist circuit guarantees cell stability by slightly lowering

the word line voltage. In [ALO14] a 10% reduction in word-line voltage in a 6T minimum size cells (6T-MSC for short) during read operation lead to the same stability level than a conventional 6T cell at nominal voltage, with 20% area saving. According to this, we decided to study the viability of 6T minimum size cells in this work.

5.1.1.4 6T cell Layout

The layout of the 6T cell has been designed with a regular layout topology [OSA01]. This cell is also called wide cell, lithographically symmetric cell or, in the version to be used, a cell of rectangular diffusions. The reasons for its choice are basically that it reduces the variation of parameters and its use is recommended below 90 nm nodes [PAV08].

When considering design for manufacturability, bit-cell layouts having simple shapes are desirable. The basic features of this layout are that all polysilicon lines are aligned in the same direction, orthogonally to diffusions, that are also aligned in the same direction.

The layout of a 6T-MSC cell used for this thesis is shown in the Figure 5. 5 together with its transistor schematic to be able to identify the position of the transistor in the layout. Furthermore, it is included the cell with metal layers in order to identify the position of *bit-lines*, *word-lines*, power lines and ground lines. We also note that by setting α=1, bends are removed from the diffusion lines, thus eliminating a possible source of variability.

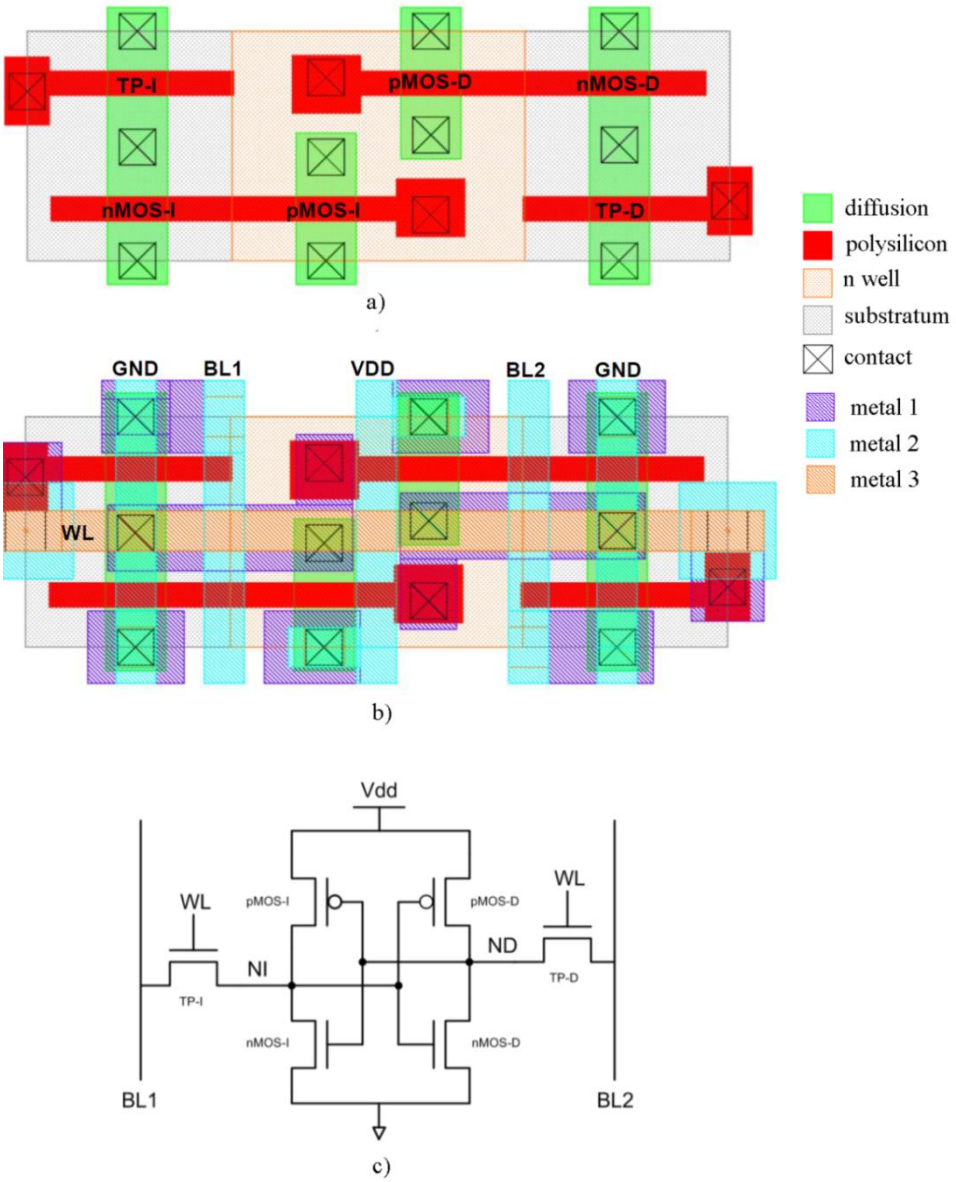


Figure 5. 5. 6T-MSC Cell a) Layout without metal layers. B) Layout with the layers of metal, c) Circuit of the cell.

It is appreciated that the layout meets the characteristics of regular layout, active areas of constant width and polysilicon lines in the same direction and aligned.

5.1.2 8T cells

Eight-transistor cells are constructed by adding two nMOS transistors (NR1 and NR2), along with an extra read-word-line (RWL) and a dedicated read-bit-line (RBL) to the 6T cell (Figure 5. 6). The write-word-line signal (WWL) is used exclusively for write operations: in an 8T cell, a read access does not disturb its contents, providing a cell with better noise margins [BOT15].

The dedicated read port consisting on two nMOS transistors (NR1 and NR2) allow cell reading by replicating the logic state of *Node2* to the *read-bit line* (RBL), when the read word line (RWL), control signal is asserted (see Figure 5. 6). A cell 8T is asymmetric because the read port is connected only to one of the two internal nodes of the latch. The RBL is common to all cells in the same column, and it is connected to the read circuit.

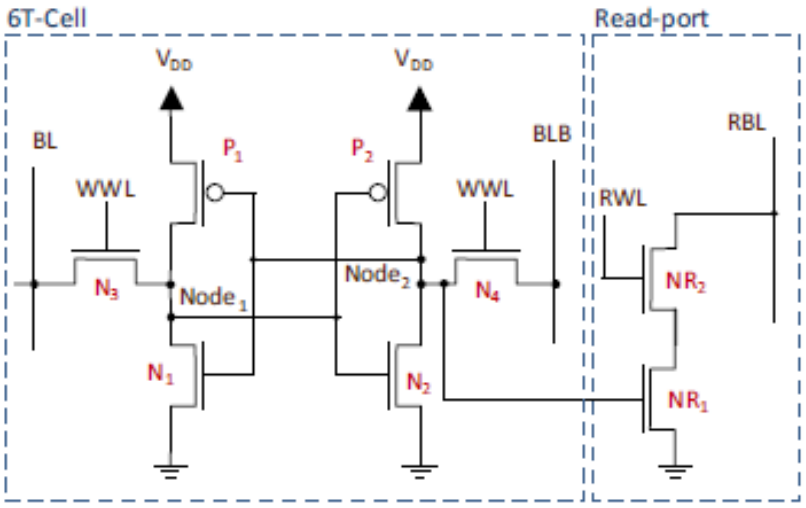


Figure 5. 6. Schematic of an 8T SRAM cell. It consists of a conventional 6T SRAM cell, formed by pull-down transistors N1 and N2, pull-up transistors P1 and P2, access transistors N3; N4 completed with an additional read port formed by transistors NR1 and NR2.

The writing process of a cell 8T is performed in the same mode as the writing process of a cell 6T as described in 5.1.1.1; however, the reading of a cell 8T is different. The voltage of node ND controls the gate of transistor NR1. The transistor NR2 (controlled by the RWL signal) connects the transistor NR1 to the read bit-line (RBL) during a read process and isolates it for the remainder time. If during a read process the ND node is at a high level, the read bit-line is discharged through the transistors NR2 and NR1. However, if during a read process the node ND is at low level the read bit-line is not discharged since the transistor NR1 is OFF. In this way, the reading circuit can know the state in one of the internal nodes of the cell and therefore,

the logical value that it is stored. Since the read process is performed through a single bit-line, the read circuit cannot be differential.

It is important to that, unlike a cell 6T, in a read process in an 8T cell does not disturb its contents, since it is performed through the gate of the transistor TL1. This is an advantage since it eliminates the compromise between the dimensional constraints which are imposed on a read and write process since the read process is done without disturbance. Therefore, the transistors could be optimized only for the writing process (minimum size transistors can be used without impact on read noise margins).

5.1.2.1 8T cell Layout

Figure 5. 7 shows a comparison between the layouts of a 6T and an 8T cell (without the metal layers). It is also included the layout of an 8T cell with the metal layers and the transistor level circuit of the 8T cell.

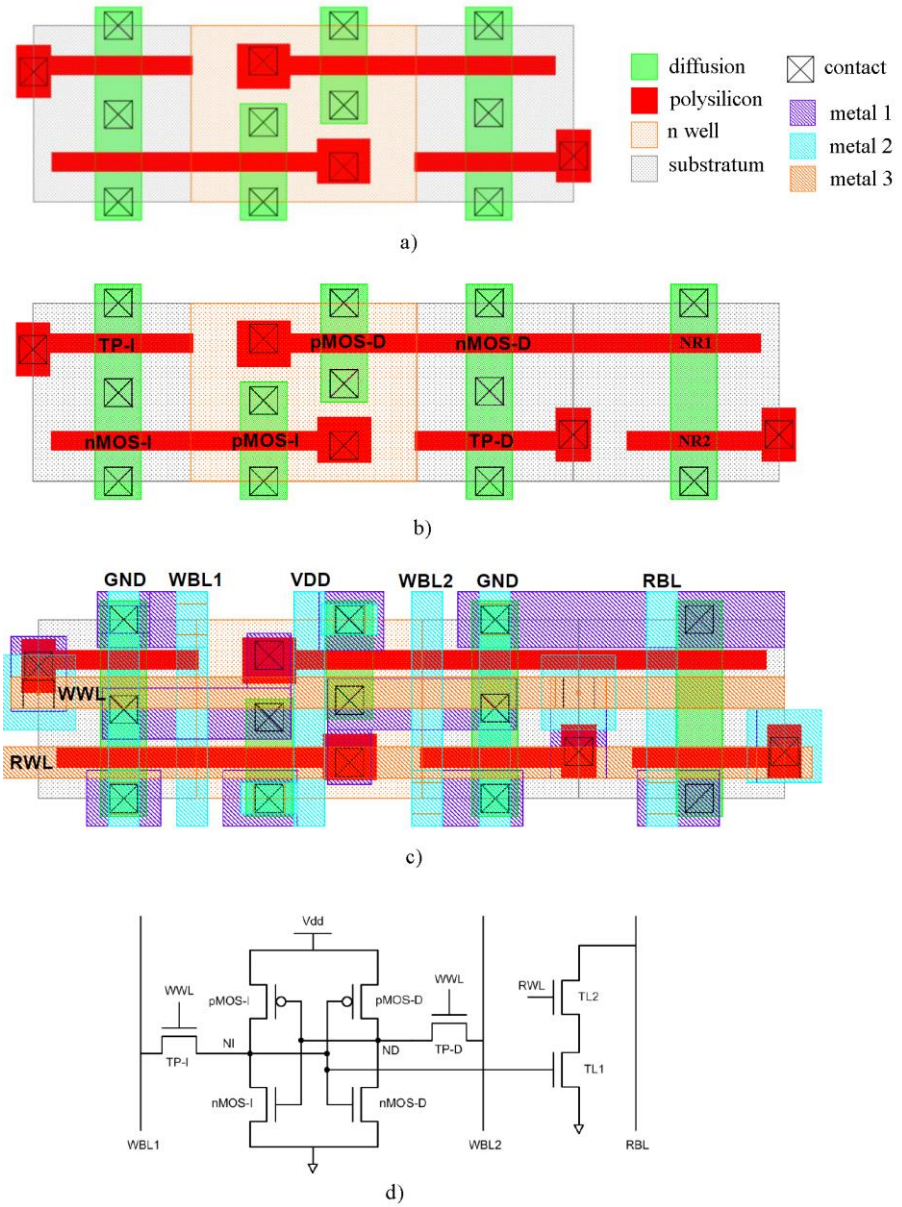


Figure 5. 7. Comparison between the layout of a 6T cell and an 8T cell. a) Layout 6T without the metal layers. b) Layout 8T without the metal layers.c) Layout 8T with metal layers. d) The circuit of a cell 8T.

In the Figure 5. 7, it is seen that the read stage has been added to the right of the layout of a cell 6T to form the cell 8T. The polysilicon lines in 8T cell follow the same orientation as the 6T, and these are aligned with the existing lines. No bends are introduced into the new active zones. The transistor of the read stage which shares a polysilicon line with the inverter is the one which is responsible for reading the state of the cell (NR1) and the other one is the transistor which is connected to the read *bit-line* (NR2).

The main features of the 8T cell and 6T cell are compared in Table IV.

Table IV. Comparison of the main characteristics of the 8T cell and 6T measures.

Cell	Width pMOS, Wp (µm)	Width nnMOS, Wn (µm)	Cell height (µm)	Cell width (µm)	Increased width with respect to 6T	Cell area (μm^2)	Increased area with respect to 6T
6T	**0,15**	**0,15**	**0,58**	**1,75**	**0%**	**1,01**	**0%**
8T	**0,15**	**0,15**	**0,58**	**2,41**	**38%**	**1,39**	**38%**

5.1.3 Cells radiation sensitivity

Both 6T and 8T cells have two internal nodes sensitive to radiation: Node1 and Node2, both belonging to the internal latch (see Figure 5. 8). In order to analyses the sensitivity, it is important to note that a logic upset can be due to electron collection at the drain of the nMOS pull-down transistor connected with the cell node being at logic "1," or to hole collection in the drain of the pMOS pull-up transistor connected with the node being at logic "0." Note that in both cases SEU is originated in a transistor in OFF state. Typically, the charge collection efficiency for holes in CMOS devices is smaller than for electrons; moreover, the magnitude of Q_{crit} required to flip the node being at "0" is higher than the corresponding Q_{crit} required to flip the node being at "1" [TOR14]. Figure 5. 8 shows the layouts of the 6T and 8T cells pointing out Node1 and Node2, the most sensitive regions to radiation.

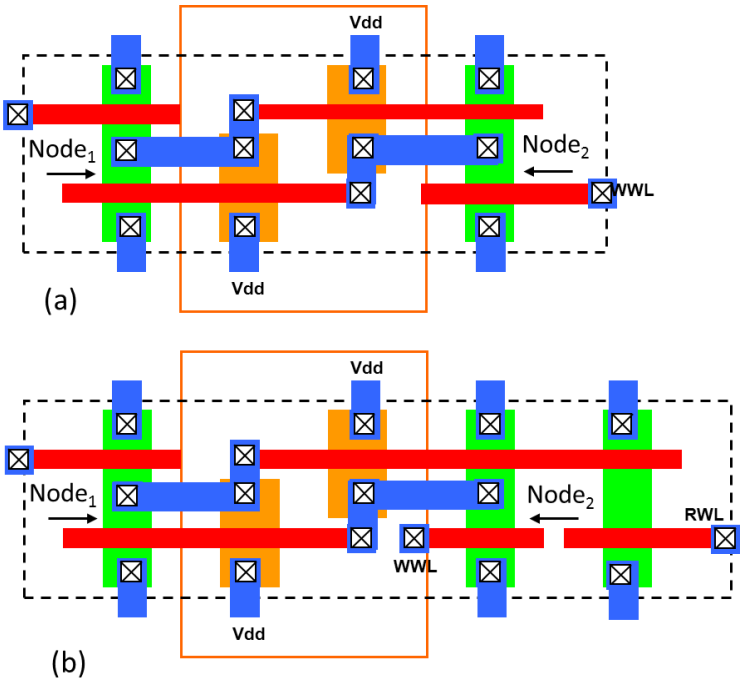


Figure 5. 8. ***(a) 6T-cell layout. (b) 8-T cell layout***

Figure 5. 9 illustrates the SRAM core floor plan for a 4x4 block. Note that the cell width is larger than its height. The sensitive pull-down devices are circled assuming that all cells are initialized to logic-1 (only transistors being in off state are sensitive to charge collection). MBUs are expected to be more common when the sensitive devices are closely placed [YIN15].

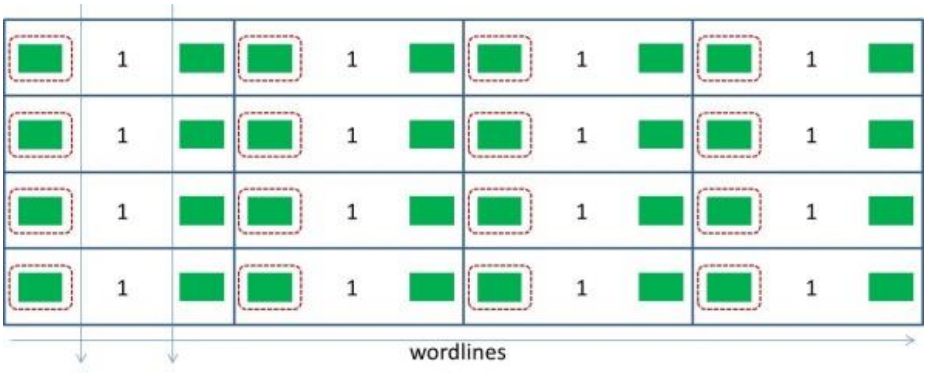


Figure 5. 9. Detail of a 4x4 block of the memory core, individual bit-cells are placed sharing their biasing contacts. The green rectangular shapes indicate transistor sensitive areas. The memory core is obtaining by repeating this block.

5.2 SRAM features

The memory used in this work has been implemented in a commercial 65 nm CMOS technology, biased at 1.2 V. The chip has two separate memory banks activated with different characteristics but both with the same number of cells, 16,384 cells distributed in 256 rows and 64 columns. Each cell stores one bit, so it is 16 kb memories. The data is read in 8-bit words, resulting in 2048 8-bit or 2 kB words.

It is considered that the number of cells in each memory is ample to collect enough data in case of the memory is subjected to an irradiation process in which it is impossible to control the location of the affected cells. According to [TOR12], each memory contains approximately 530.000 transistors in the modules.

Both SRAMs used for this thesis were implemented in the same chip. The main features of each block are reported in Figure 5. 10.

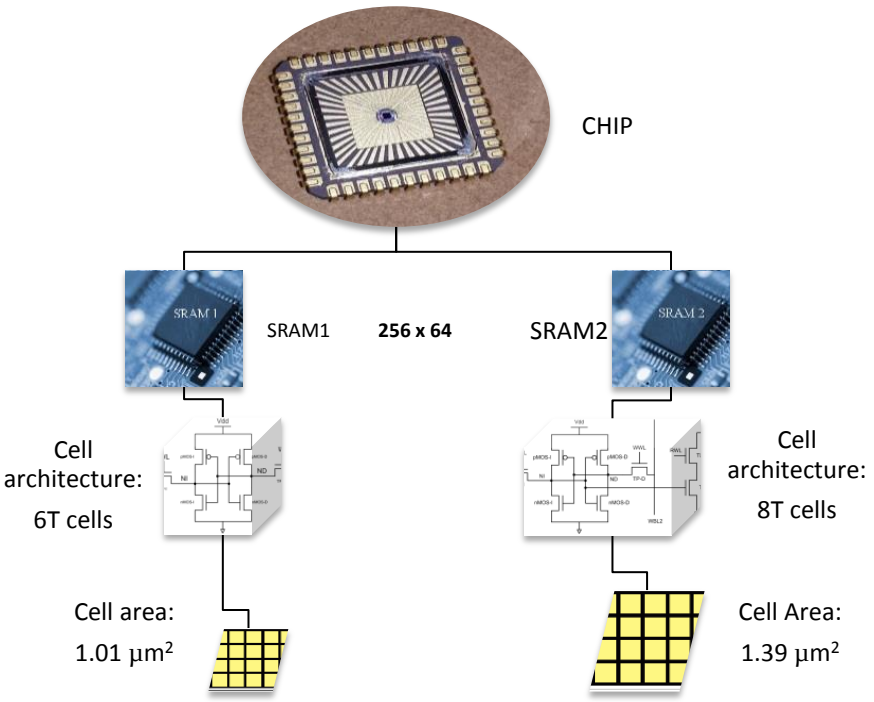


Figure 5. 10. SRAM features.

5.2.1 SRAM structure

The structure of each SRAM consists in:

An array of cells

- A bit is saved in each of these cells. These can be in storage mode, that means these maintain the value of the bit that contain or in access mode in order to read the saved data or write a new one.

A row decoder

- It is a circuit capable of activate the access to the cells which them are part of a row of the matrix. When it wants to access a particular cell, either to read it or write it, the decoder activates access to the entire row to which the cell belongs.

Write circuit

- It is a circuit capable of modifying the voltage levels of the bit-lines of a given column and, thus, write the desired value in one of the cells of that column. The cell to be written will belong to the row whose access has activated the row decoder. The process is the same for the 6T and 8T cases.

A column decoder

- It is used when the number of read or write circuits is lower than the number of cells in a row in the memory. In this case, only a subset of the cells in each row are read or written. The purpose of the column decoder is to activate the transmission doors necessary to ensure that the read or write circuits are connected to the bit-lines which give access to the cells to be read or written. The number of cells which are read or written at the same time is called the word length of the memory.

Read circuit

- It is a circuit that is used to read quickly the contents of a certain cell of memory. It is different for 6T and 8T.

A schematic representation of these elements can be seen in Figure 5. 11.

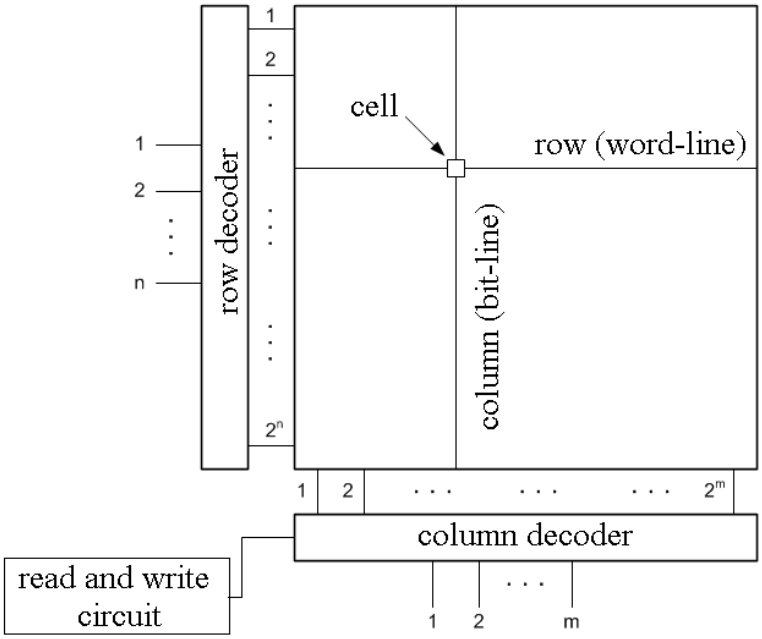


Figure 5. 11. Basic SRAM structure.

Figure 5. 12 shows how an accessed cell (B is the word length) is separated from the next one by a certain amount of cells in horizontal. Although the different blocks have been represented one in front of the other, their real position on the layout of a memory is obviously two-dimensional. The three-dimensional representation has been used in order to improve the visualization. The most common structure set each block horizontally in order to share the word-line by all the cells of the same row.

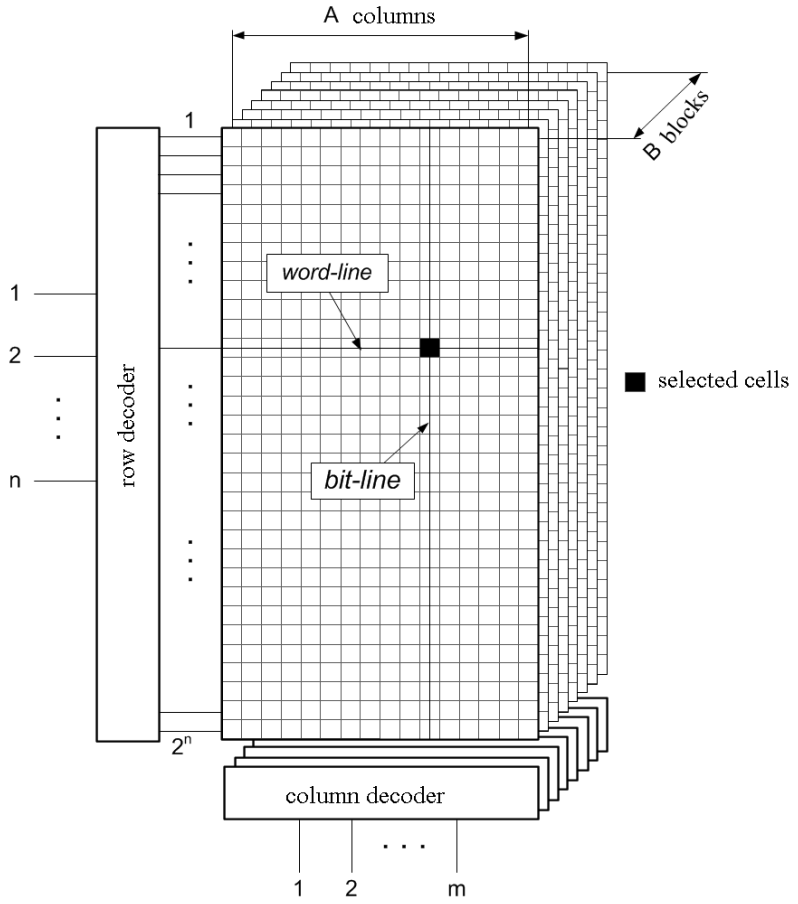


Figure 5. 12. Organization by blocks in an SRAM(source [TOR12]).

The row decoder is responsible for activating the corresponding word-line, depending on the chosen memory address. With this structure, all cells in the same row (B·A cells), independently of the block which those belong, share the same word-line and these are selected in each read and write operation.

However, in each block, only one cell is accessed. The chosen cell is determined by the column decoder. In this way, each read (or write) operation only access to B cells, one per block.. The column decoder is responsible for ensuring that of every cell selected by word-line, only one is connected to each read (or write) circuit.

5.2.2 Interleaving

To reduce the number of errors occurring simultaneously in the same word (MBUs), the bits of each word are located with a physical separation on the memory layout: interleaving distance. By using a large interleaving distance, the probability that a single transient event affects two bits in the same word is highly reduced. In this way, it is possible to use simpler detection and

correction codes since it is less likely that the same word has several bits simultaneously affected [GIL05].

In the designed memory, all bits of the same word are located in the same row but not in adjacent cells but with an interleaving distance of 8 cells. That is, two consecutive bits of the same word have between them 7 cells which these are part on the content of another 7 words.

5.2.3 SRAM voltage

The nominal supply voltage of the 65 nm technology is 1.2 V. However, the input/output cells (which these will be called convenience pads or I/O cells) that have been used for the prototype are configured to work at 3.3 V. That is, all input signals through the circuit must be 3.3 V, and these are internally converted by the pads to the memory supply voltage. Likewise, the signals generated by the circuit are converted by the output pads to a voltage of 3.3 V.

5.3 Distribution of SRAMs in the final layout

This section describes the distribution of the two memory banks in the chip used for this thesis. Figure 5. 13 shows the final layout with the distribution of all elements together with the pad ring:

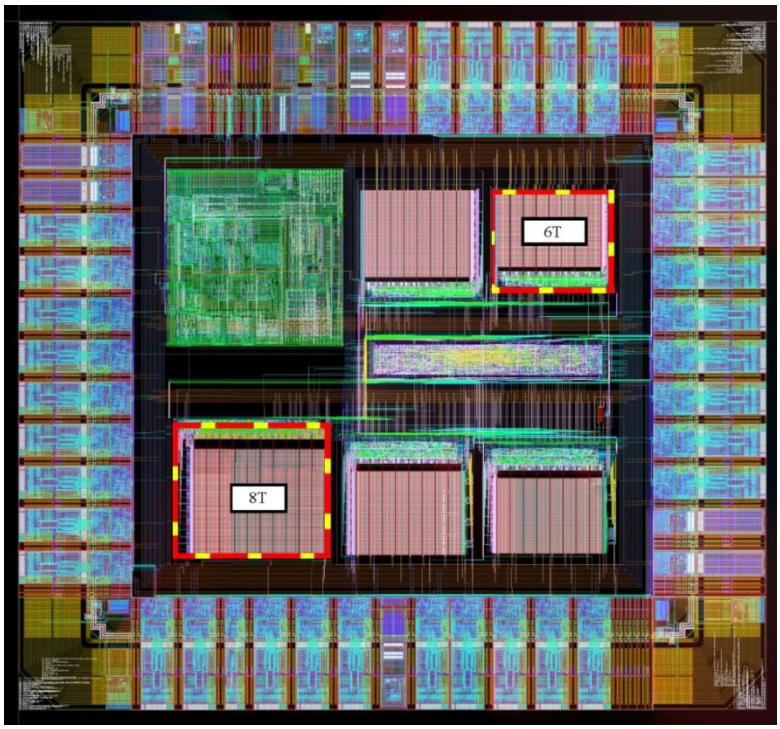


Figure 5. 13. Final layout of the integrated circuit with the highlighted layout of the two memory banks used.

The integrated measures, including the ring pads, are 1028µm x 1070µm and its area is 1.1 mm^2. The integrated circuit has a total of 44 pads.

Table V details the dimensions of each memory bank, including the control unit in each bank.

Table V. Dimensions of memory banks

SRAM	Width(µm)	Height(µm)	Area($µm^2$)	Area increased respect to 6T
6T	150	182	27.300	0%
8T	205	193	39.565	45%

5.4 Transient events effects by radiation in SRAMs

This section details the mechanism by which an energy particle can generate an SEU in an SRAM memory. It also describes the different magnitudes that are used to quantify the robustness of memories and SRAM cells.

5.4.1 Impact effect by particles in a SRAM memory cell: SEUs

It has been described in chapter 2 how the impact of an energetic particle in a circuit is capable of generating a charge collection. The mechanism consists of the cross of an energetic particle through the matter close to sensitive zones in the device which creates electron-hole pairs by some of the ionization mechanisms described in section 2.4.2. This effect could cause the occurrence of a transient current pulse, which in turn causes a change in the voltage in the affected node. In the case of SRAM cells, if the pulse is large enough it can cause a change in the cell logical value, which means, a SEU.

When the particle impact occurs near the n+/p junction polarized in inverse (drain-substrate union of an nMOS in short), the node n+ (drain), being at VDD, collects the generated electrons and, therefore, voltage decreases at the node. In contrast, if the impact occurs near a p+/n junction polarized in inverse (drain-substrate union of a pMOS in short), the node p+ (drain), being at 0 V, attracts part of the generated holes and, therefore, a voltage increase occurs at the node [DOD94].

Assuming a cell SRAM 6T with a node at a high level and another at a low level as in Figure 5. 14, it is possible to distinguish two mechanisms of generation of SEUs.

- If the charge collection produced by the ionizig particle affects the OFF-nMOS transistor drain of the latch (we assume that it corresponds to the ND node), the current generated by the collected charge decreases the node voltage, if the magnitude of the impact is high enough, it can cause that the node reaches temporarily a value low enough to activate cell feedback, the voltage at node ND will continue to decrease while the voltage at NI increases until there is a permanent inversion of the state for the cell.
- If the cross of the particle affects the OFF-pMOS transistor drain (we assume that the OFF-pMOS transistor is connected to the NI node), the current generated by the collected charge causes an increase in voltage node. In this situation, NI was at 0 V, so if the magnitude of the impact is high enough, it may cause that the node reaches temporarily a value high enough to decrease the voltage at the output of the other inverter (which has as input NI). This change could cause that the cell own feedback continues to increase the voltage in NI and decreasing the voltage of ND until there is a permanent inversion of the state in the cell.

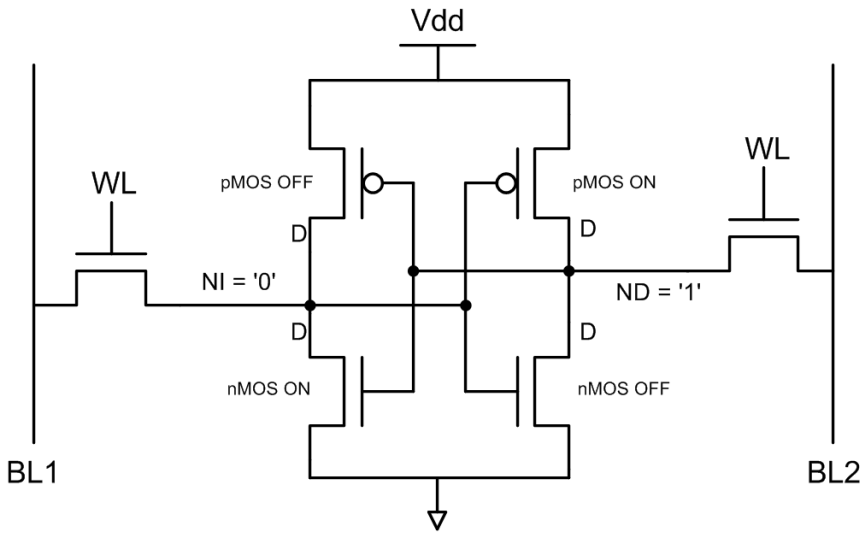


Figure 5. 14. 6T SRAM cell. The case with the ND node at a high level and the NI node at a low level.

It is important to know that because to the cell consists of two feedback inverters, the voltage levels in the nodes are mutually reinforced. When, due to the interaction with a particle, the voltage value in one of the nodes begins to degrade, initially, it must overcome the opposition of the feedback of the cell that it tends to prevent change. But if the perturbation is strong enough to pass a given threshold level, the own feedback of the cell helps to finalize the inversion in the

voltage value of the two nodes [TOR12]. Figure 5. 15 shows the simulation behavior of two nodes in a cell during a state change caused by a current injection which emulates the interaction effect of a particle. The nodes end up inverting their voltage levels, and a SEU is produced.

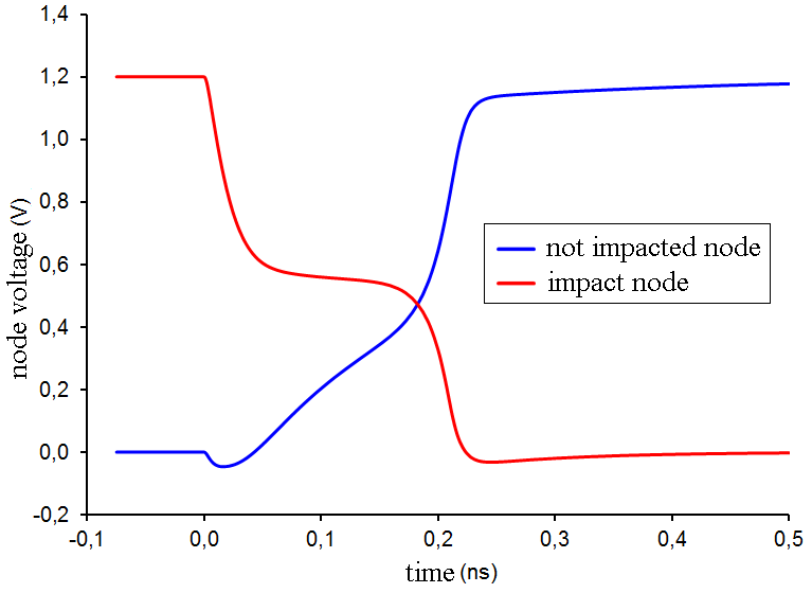
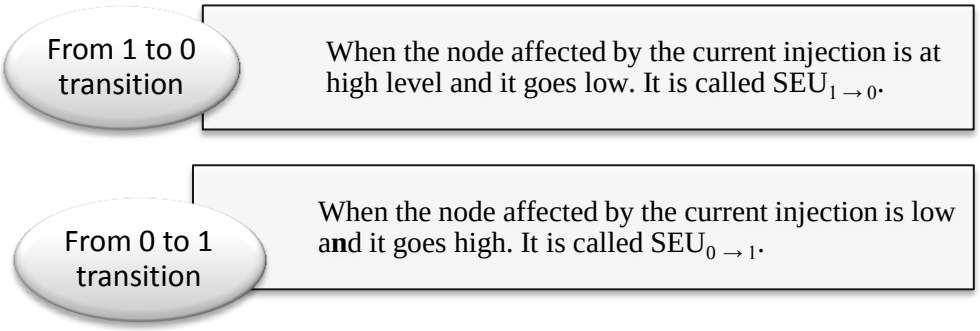


Figure 5. 15. Behavior simulated of two nodes in a SRAM cell during an SEU (source [TOR12]).

It is useful to differentiate between two types of change in a cell state:



$SEU_{1\rightarrow0}$ is caused by a collection of electrons at the drain of the pull-down transistor in OFF mode, while the $SEU_{0\rightarrow1}$, corresponds to hole collection at the drain of the pull-up transistor in OFF mode. It is assumed that $SEU_{1\rightarrow0}$ is much more probable than $SEU_{0\rightarrow1}$ [HEI05]. This is

because hole mobilityis smaller than the electron mobility and, in addition, the charge collection efficiency related to pMOS transistors is lower than the charge collection in nMOS devices [HAZ00].

Finally, it should be noted that "SEU" makes reference to the change stored in a cell. However, charge carriers generated by the cross of the particle can cause changes in more than one cell. This happens in cells which these are close to the ionization traces created by the particle. In this case, the effects produced are called Multiple Cell Upset (MCU) or Multiple Bit Upset (MBU),that have already been defined previously in section 2.4.2.1.2 [MAV08].

5.4.2 Critical charge and SER

The critical charge, (Q_{crit}) is a parameter used to characterize the robustness against events transient induced by radiation in SRAM cells. However, to study the robustness at a SRAM memory level it is used the Soft Error Rate (SER).

SER and critical charge are correlated since both of them measure the robustness of a memory or a cell to transient events. Usually, a high critical charge implies a low SER. However, that relationship is not so simple because it depends on other parameters, some of which are often difficult to know or estimate.

It is important to take into account that "SER" depends on the radiation flux received by the circuit while the critical charge does not depend on the flux. For this reason, the radiation flux has to be a known parameter. In addition, a certain particle flux is capable of deposit an amount of charge. However, the critical charge is not measured in terms of deposited charge, but taking into account only the effective charge that the node ends up collecting. For this reason, it is necessary to determine the collection efficiency of the charge and thus calculated the collected charge (Q_c). This parameter is not easy to calculate since it depends on multiple factors that can be difficult to quantify, as specific technological parameters, circuit geometry, angle and position of the ionization trace, etc. For example, Q_c depends on whether these are used, or not, guard rings and their specific design [NAR08]. For these reasons, to calculate Q_c, 3D simulators are usually used. These simulations are computationally expensive and, in addition, since the position and angle of the ionization trace cannot be known in advance, it is often necessary to carry out a lot of simulations to contemplate the different situations.

The semi-empirical model used in [HEI05] and [SEI06] to calculate the SER from the critical charge is:

$$\boldsymbol{SER_j = k\emptyset_{rad} \sum_n A_{dif}^n e^{-\frac{Q_{crit}^{n,j}}{Q_c}}} \qquad \textbf{5. 4}$$

where:

- SER_j is the soft error rate of the circuit in state j.
- k is a scaling parameter.
- $Ø_{rad}$ is the radiation flux.
- Q_c is a parameter that represents the charge collected and it depends on the radiation type, the technology, the geometric features in the circuit and in the trajectory of the particle.
- A_{dif}^n is the area of the node n which is sensitive to interaction with the particles.
- $Q_{crit}^{n,j}$ is the critical charge of node n in state j.

The model takes into account the particle flux, the effective charge collected and two additional parameters A_{dif}^n and k. "A_{dif}^n" is used to take into account the cross section of the affected node, the model assumes that the cross section depends linearly on the area of the node and exponentially on the critical charge (see equation 5.4) . The "k" parameter is a scaling parameter which takes into account all other factors that influence the SER.

According to equation 5.4, there is an exponential dependence of SER with the critical charge. However, the influence of the critical charge on the SER is also strongly influenced by the parameter Q_c. At an equal critical charge, a node with a low Q_c has a SER lower than a node with a higher Q_c. In [HAZ00] it is stated that the Q_c of a nMOS is about 100 times greater than in a pMOS. For this reason, the SER percentage related to events generated in the drain of nMOS transistors is greater than those related to pMOS drains.

The practical application of equation 5.4 usually requires adjusting parameters like Q_c and A_{dif} from experimental measures, since their theoretical determination is difficult.

CHAPTER 6

SEU MEASUREMENTS

This chapter presents the SRAM behaviour under different test beams, including 17 MeV protons and neutrons with energy range between 5.8 and 8.5 MeV. In addition, results from a mixed-field environment are also shown and correlated with the HEH approach prediction.

6.1 Introduction

Although it is appropriate to simulate how particles interact with electronic devices, SER is hard to predict as its value depends on the source and type of particle under consideration, device structure and material properties, so the experimental characterization is often necessary to determine the real behavior of a given component.

As it was introduced in chapter 2, although SEUs are non-destructive soft errors, they can lead to data corruption and faulty information. Moreover, in the case of those systems having SRAM bit-cells containing configuration information (ex., in an FPGA) SEUs can lead to malfunction.

The effects produced by a particle on an electronic component depend on its energy, as radiation environments are composed by particles having different energies, the concept of cross-section is introduced to compute the soft error rate of a component in the presence of a given radiation spectrum. The cross section for a memory is a measure of the SEU occurrence probability that depends on the type and energy of the incident radiation. It is obtained experimentally through n different measurements [x_1, ...,x_n] of individual components of the same distribution, so it can be calculated through equation 6.1 [GAR14].

$$\boldsymbol{\sigma_{SEU} = \frac{\sum_{i=1}^{i=n} x_i}{n}} \qquad \textbf{6. 1}$$

Each measurement x_i is referred to the same component, facility, radiation type or particle and energy. It is defined by dividing the number of SEU counts "*N*" by the respective particle fluence Ø [GAR14] as shown in equation 6.2.

$$\boldsymbol{x_i = \frac{N_i}{\emptyset_i}} \qquad \textbf{6. 2}$$

It is usual to find the cross section value in function of the size of the memory in bits, so assuming that Ø is the fluence of the incident radiation (particles), N is the number of produced

events in the overall memory, and M the size of the memory in bits. The cross-section of an SRAM bit cell can be computed as it is shown in the equation 6.3.

$$\sigma_{SEU} = \frac{N}{M\emptyset} \qquad \textbf{6. 3}$$

The cross section will depend on the memory fabrication technology and the supply voltage. The cross section values will be subject to a certain spread related to the natural deviation in the sensitivity of the devices. This value which is related to the standard deviation of the measurement distribution and is highly important, especially for components to be used as SEE-count based radiation monitors [GAR14]. Two different error types should be considered as a first approach, statistical and systematic. The statistical type is of a random nature, and these can be reduced by increasing the counts per measurement and the total number of measurements per cross section.

The corresponding statistical error in a set of "n" measurements, E_{stat} is considered in this work as two times the standard deviation of the mean (sd_μ) as shown in equation 6.4, where sd_n is the standard deviation of the measurement set x_1, ...,x_n, defined in the equation 6.5.

$$\boldsymbol{E_{stat} = 2 \cdot sd_\mu = 2\frac{sd_n}{\sqrt{n}}} \qquad \textbf{6. 4}$$

$$\boldsymbol{sd_n = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(x_i^2 - \mu^2)} \quad where \quad \mu = \frac{1}{n}\sum_{i=1}^{n} x_i} \qquad \textbf{6. 5}$$

In this thesis, for a finite number of measurements $\boldsymbol{x}_i$, it will be subject to the statistical spread of the standard deviation distribution [NOS51]. The statistical error is associated with the contribution to the uncertainty related to the count statistics, $\boldsymbol{sd_{count}}$, of the individual measurements, which for a cross section $\boldsymbol{\sigma_{SEU}}$ obtained from N> 50 counts can be calculated using equation 6.6.

$$\boldsymbol{sd_{count} = \frac{x_i}{\sqrt{N}}} \qquad \textbf{6. 6}$$

In this case, the Poisson distribution characteristic of the SEE events can be approximated by a Gaussian distribution. For count or N values below 50, the tabulated uncertainty ranges should be employed for the desired confidence level [WIL37]. For count or N values below 50, it should be employed tabulated uncertainty ranges in an acceptable level [WIL37].

About of systematic error E_{sys}, it will be affected to all results in the same manner, as these are referred on a given calibration the fluence measurements at each facility from which the cross

section values are derived. Unless stated otherwise, E_{sys} will be considered as 10% for a 2*sd* confidence level, following what is typically reported by the facilities.

In this thesis, cross section values will typically be expressed with their associated statistical relative errors in percentage. An example would be as $1.23 \cdot 10^{-14}$ cm^2/bit ± 10%.

The SER experimental determination means to measure the number of SEUs per unit of time that occurs in an SRAM under certain conditions.

In order to determine the SER in a memory bank, the following method has been used:

1. Write all the cells of the memory bank to a known initial value.
2. Read the contents of the memory bank, compare it with the value written initially and verify that they match.
3. Start irradiation.
4. Wait for a certain irradiation time step (T_S).
5. Read the contents of the memory bank and compare it with their initial values written in the first step, compute the number of cells that have experienced a logic state change (N_i)

Repeat steps 1 to 5 until the desired total irradiation time, T_{exp}, has been reached. The total number of SEUs can be calculated by summing all the SEUs that have occurred in the different irradiation periods as shown by the equation 6.7.

$$\boldsymbol{N_{TOT} = \sum_{i=1}^{n} N_i} \qquad \textbf{6. 7}$$

$$\boldsymbol{T_{exp} = n \cdot T_s} \qquad \textbf{6. 8}$$

It is important to choose an adequate irradiation time step, since if during this time interval, the same cell is affected two or more times by an SEU, the result for the number of SEUs will be erroneous (i.e. if the same cell suffers an even number of SEUs, at the end of the sampling period, it will be in the same state as at the beginning and therefore, no event will be counted). For this reason, it is not appropriate to use excessively long irradiation time steps, so that the chances of having multiple SEUs occurring in the same cell are low.

The total SER during the experiment can be obtained as:

$$\boldsymbol{SER_i = \frac{N_i}{T_s}} \qquad \textbf{6. 9}$$

$$\boldsymbol{SER = \frac{\sum_{i=1}^{n} SER_i}{n} = \frac{\sum_{i=1}^{n} N_i}{n\ T_s} = \frac{N_{TOT}}{T_{exp}}} \quad \textbf{6. 10}$$

Another alternative way to calculate the SER is the slope of the graphical representation of the total number of SEUs as a function of the elapsed time of the experiment.

The soft error rate per bit at a given particle flux is obtained as it is expressed in the equation 6.11.

$$\boldsymbol{SER_{bit-cell} = \frac{N}{MT_{exp}} = \sigma_{SEU} \emptyset_t} \quad \textbf{6. 11}$$

For non-monoenergetic sources, the soft error rate is related to $\sigma_{SEU}(E)$ by the integral equation 6.12 [GAR13,MAL17]

$$\boldsymbol{SER_{bit-cell} = \int_{Emin}^{Emax} \frac{d\emptyset_t}{dE} \sigma_{SEU}(E) dE} \quad \textbf{6. 12}$$

where $d\Phi(E)/dE$ is the differential flux of the particle spectrum (that also depends on the energy), E_{min} is the cut-off energy below which no upsets occur, and E_{max} is the maximum particle energy.

To determine the SEU rate produced as a response to a particular type of non-monoenergetic radiation environment (i.e. the natural radiation environment in a given terrestrial position produced by cosmic rays) the cross-section $\boldsymbol{\sigma_{SEU}}$ is usually fitted to a Weibull function obtained from experiments performed with a tunable monoenergetic source.

This work is not oriented to obtain the SER produced by a given environment subject to a certain energy spectrum. We will analyze the results produced by a quasi-monoenergetic radiation source and, therefore, compute the related SER from (6.11), assuming that the cross-section obtained from (6.3) can be regarded as a cross-section mean-value of the monoenergetic source. In each case, the behavior of 6T and 8T bit-cells will be presented.

6.2 Experimental set-up

A portable set-up, that allows its transport to the different facilities in which the circuit will be irradiated, was developed to perform the experimental measurements. It was implemented using a CycloneII® FPGA[ALT06].

The DUT, consisting on two different and standalone SRAM memory blocks was mounted in a printed circuit board (PCB), DUT-board, which is connected to the FPGA control board by a flat cable as shown in the figure 6.1. The voltage supply on the DUT-board was fed by the control board. SRAM accesses (read and write) were managed through the FPGA. Data acquired by the control-board were sent to a laptop connected via Ethernet-USB connection to the control board. Finally, MATLAB code was developed to detect the presence of events in the measured raw data.

Previous experiments performed with alpha particles showed that the cross section of the SRAMs does not depend on the initial pattern stored in the memory (‘All Zeros’, ‘All ones’ or ‘alternative bits’) [TOR12], the bit pattern 0x00 or ‘All Zeros’ was used during the tests to write all the cells of the memory banks to a known initial value.

The working frequency used in the experiments was 2MHz, and the strategy used in the data collection was to configure the system to send the data from the chip to the laptop through the control board each time that a change was detected in the values acquired from the memory.

The experimental setup used has as purpose to write and read both 6T and 8T SRAM memories during irradiation.

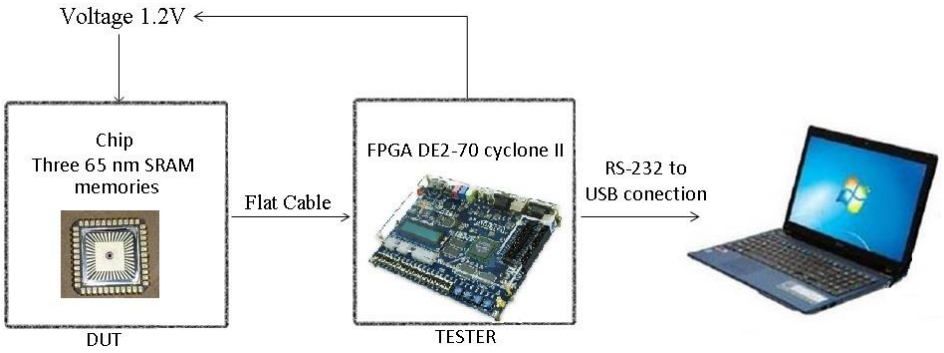


Figure 6. 1. Test Setup for the SRAM tests.

6.3 Alpha particle accelerated test: SEU results

This section describes the experimental measurements that have been made with an alpha particle source described in the chapter 3. The distance between the source and the DUT surface was 3 mm approximately, see Figure 6.2, which is quite important, since the alpha particles of this energy have a length path about 4 cm in the air [POC96]. The flux alpha particle in the accelerated test corresponds to a flux of 3250 alphas/s·cm^2.

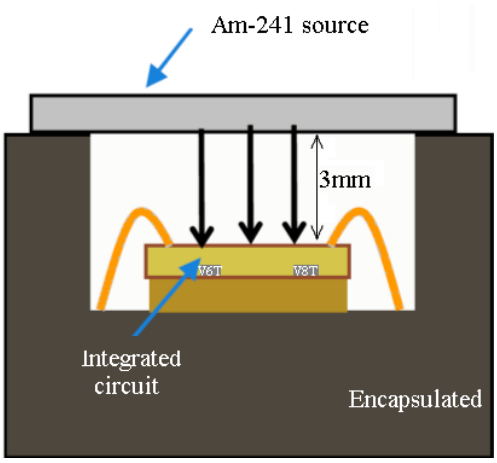


Figure 6. 2. Diagram of the radioactive source on the socket of the integrated circuit.

Although an experiment with alpha particle and these SRAMs is discussed in more detail in [TOR12], in order to compare the results obtained in different experiments in this thesis, it was decided to realize a similar experiment before moving the device and the setup to external irradiation facilities.

The first experiment to determine the accelerated SER has been performed during a time of 6.5 hours with a sampling period of 10 ms. As it was said above, to reduce the amount of data generated without losing information, the system was configured to save a file with the memory content every time that a change in the state of at least one bit-cell is detected. In average, soft error rates about 1.6 SEU/min for the 6T memory bank and 1.13 SEUs/min for the 8T memory bank have been observed.

Figure 6.3 shows the results of the number of accumulated SEUs during the irradiation time for the two cell types.

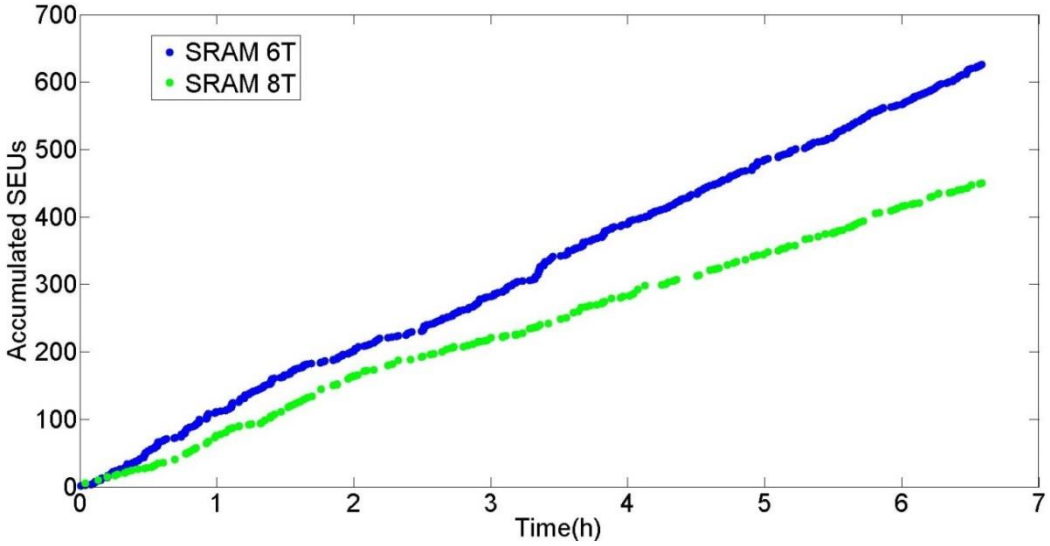


Figure 6. 3. Number of accumulated SEUs over an irradiation period of 6.5 hours in the cells considered.

It is possible to observe in figure 6.3 that the evolution of the number of accumulated SEUs follows a linear trend vs. time that is; its slope (the SER) is constant. This result was expected since the SER does not depend on time.

Table VI shows the differences between the SER of the different memory blocks.

Table VI. Comparison of SER and the area for the different cell types

Cell Type	*Cell Area (μm^2)*	*Increased area respect to 6T*	*SER (SEU/h·mem)*	*SER decrease respect to 6T*
6T	*1.01*	*0%*	*95.15*	*0%*
8T	*1.39*	*37.7%*	*68.34*	*28.18%*

As it was described above, cells in SRAM 8T have an additional parasitic capacitance due to the presence of the read port. So, although this SRAM has two additional transistors and higher area, 8T cell is slightly more robust than the 6T cell to alpha particles, both in terms of SER and critical charge [TOR12]. Observing these results in the figure 6.3, it is concluded that with an additional area of 37.7% and adding 2 additional transistors in the reading stage, the SER can be reduced by 33%.

Although it is not discussed here in detail, it should be noted that not any increase in the transistor width, will affect SER, on the one hand, drain area, and thus the cross-section, increases with transistor width increasing SER, but on the other hand, node capacitance also increases, increasing Q_{crit} and decreasing SER [TOR12].

This experiment corresponds to a total fluence of ~$7.61 \cdot 10^7$ α/cm^2, so in order to evaluate the cross section and SER to alpha exposure, equation 6.3 and equation 6.11 have been used. The resulting cross section and SER values are shown in table VII.

Table VII. Measured SER and cross-sections in alpha test.

	σ_{SEU} *(cm^2/bit)*	***SER*** **(SEUs/bit·s)**
6T	$5.15 \cdot 10^{-10} \pm 9.4\%$	$1.68 \cdot 10^{-6} \pm 9.4\%$
8T	$3.78 \cdot 10^{-10} \pm 8.7\%$	$1.23 \cdot 10^{-6} \pm 8.7\%$

Note that both the cross section and SER have been evaluated having into account the evolution in the total experiment. The cross section evolution during the irradiation is shown in Figure 6. 4.

The Total Ionization Dose, TID, can be obtained from:

$$\boldsymbol{DOSE(rads) = K \cdot LET \cdot \emptyset} \qquad \textbf{6. 13}$$

where K is a conversion factor[1] equal to $1.602 \cdot 10^{-5}$ rad·mg/MeV and Ø is the alpha beam fluence in α/cm^2. Taking into account that the LET for alpha particles with 5.5 MeV is ~0.6 MeV-cm^2/mg [ZAI04], the resulting TID is ~731.5 rads.

Additional irradiation esperiments were performed in order to verify the results presented in table VIII witth similar results.. The total irradiation time with the alpha source was 238 hours, which corresponds to a fluence of $27 \cdot 10^8$ α/cm^2 and a dose of ~26 krads.

Similar results were obtained in [TOR12], the same devices were exposed to irradiation times of 800 hours, equivalent to a dose of 80 krads, using a different experimental set-up (a Logic analyser was used instead the FPGA).

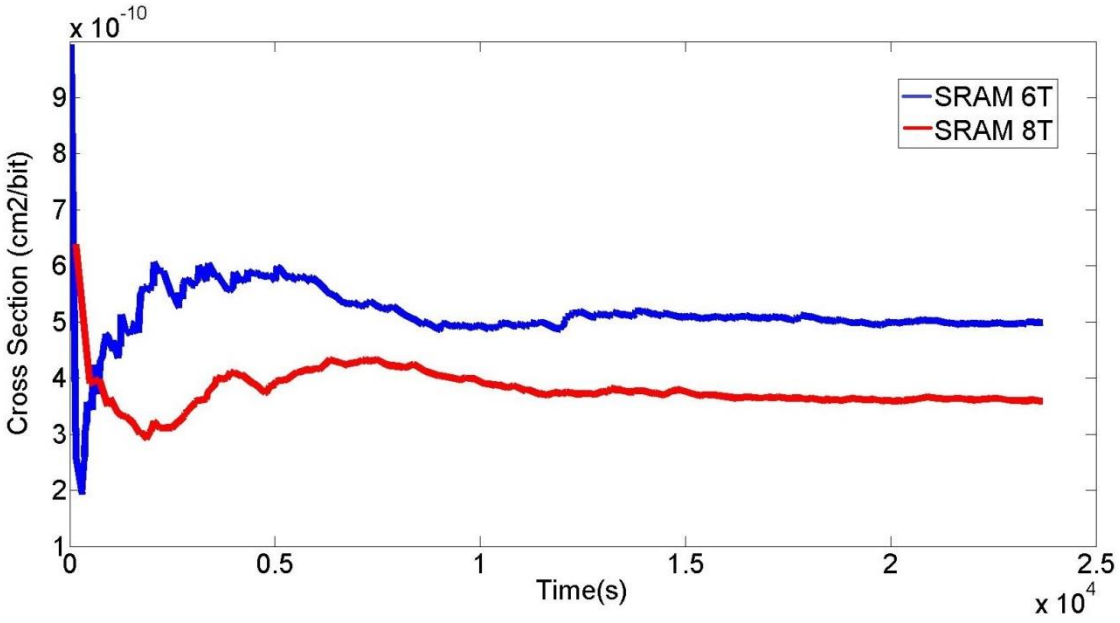


Figure 6. 4. Cross Section per bit for alpha data set.

6.4 Proton irradiation

SRAM memories were also irradiated with an 18 MeV proton beam in order to calculate their cross section to protons with energy closer to 20 MeV.

The proton energy that reaches the DUTs surface after traversing the exit window placed between the proton accelerator beam and the exterior, and the air was ~17 MeV; a value obtained using the energy loss data computed using the SRIM2008 code [ZIE08].

The irradiation flux was $1.6 \cdot 10^{9}$ p/cm^2·s, it was used to irradiate the 6T and 8T devices to a fluence of $8.5 \cdot 10^{10}$ p/cm^2, equivalent to 30 krad (Si). This procedure has been repeated four times, at the end of the irradiation process, each chip was exposed to a fluence of $3.4 \cdot 10^{11}$ p/cm^2, equivalent to an ionization dose of 120 krad (Si).

Two different samples were irradiated, the first sample (DUT_1) was the same which was exposed to the alpha source as presented in section 3.1.1, the second one (DUT_2) was a new one not previously exposed to any radiation source.

No events were observed during the first irradiation step of 30 krad. Events were detected in the three following irradiation steps; the resulting SER (corresponding to DUT_1) was 0.29 SEUs/s

in the 6T SRAM and 0.11 SEUs/s. in the 8T. Both, SER and related cross-sections are shown in Table VIII.

Table VIII Measured SER and cross-sections in proton test on DUT_1.

	σ_{SEUm} (cm^2/bit)	σ_{SEUf} (cm^2/bit)	*SER* (SEUs/bit·s)
6T	$0.64 \cdot 10^{-14} \pm 28\%$	$0.80 \cdot 10^{-14} \pm 28\%$	$1.03 \cdot 10^{-5} \pm 28\%$
8T	$0.82 \cdot 10^{-14} \pm 32\%$	$1.08 \cdot 10^{-14} \pm 32\%$	$1.32 \cdot 10^{-5} \pm 32\%$

Note that Table VIII shows the mean cross section and the cross section corresponding to the fourth irradiation step. In order to observe if it exist a dependency of the cross section on the accumulated TID, we show in Figure 6.5 the evolution of the cross-section in each consecutive irradiation interval.

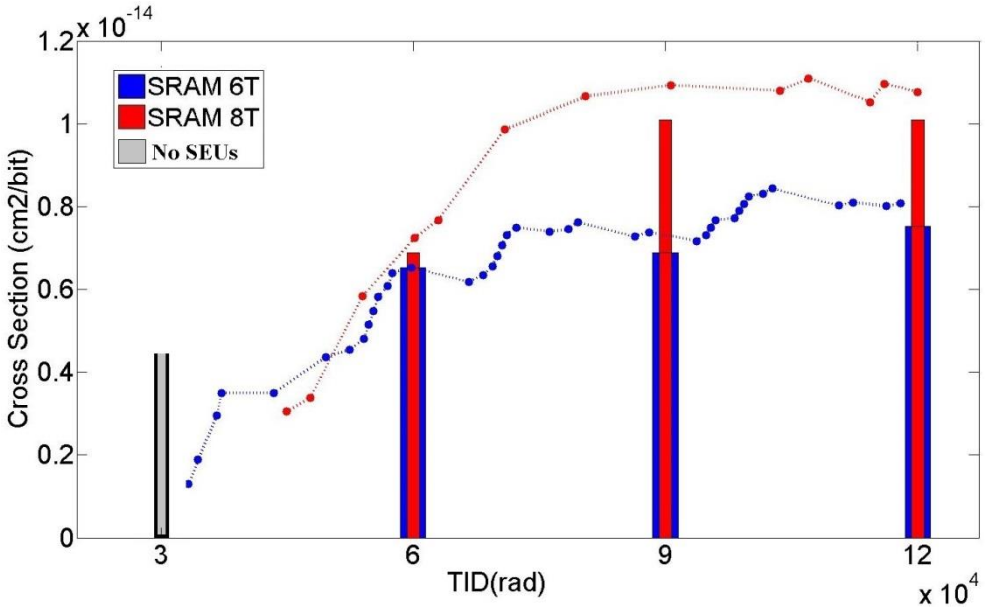


Figure 6. 5. Cross sections as function of TID for four intervals (bars) and per each measurement (lines) in DUT_1 whit SRAM 6T (blue) and SRAM 8T (red).

It is possible to observe that SEUs starts over 30 krad(Si) in SRAMs 6T and a bit later in SRAM 8T. To confirm that result we tested a second sample, DUT_2, the obtained results follow the tendency shown in the Figure 6. 6.

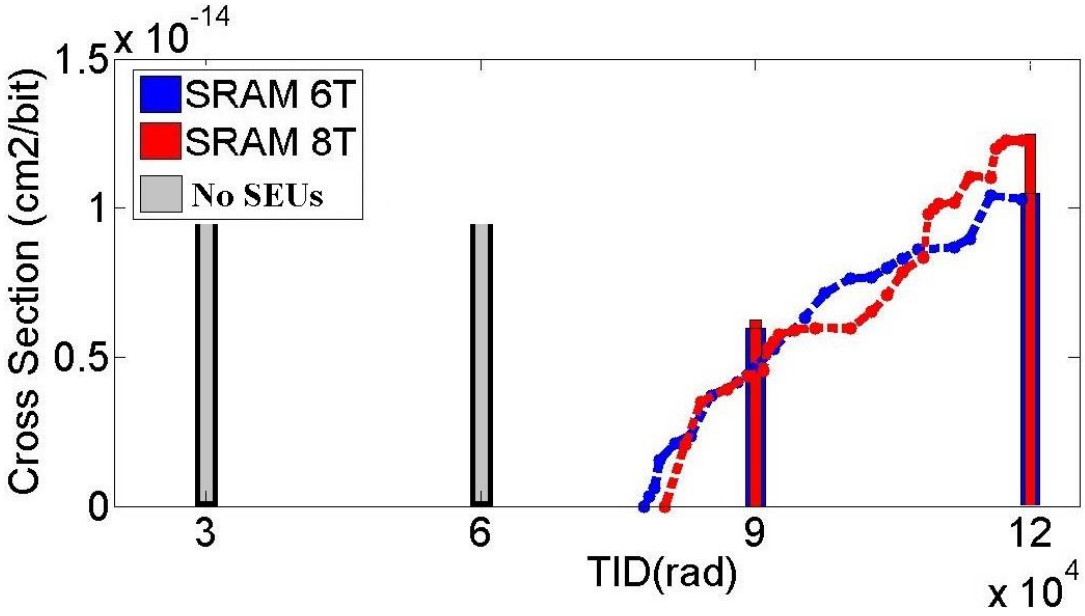


Figure 6. 6. Cross sections as function of TID for four intervals (bars) and per each measurement (lines) in DUT_2 whit SRAM 6T (blue) and SRAM 8T (red).

In this case, DUT_2 starts to present SEUs over 60 krads but the cross section and SER are quite similar to the DUT_1; see Table IX . DUT_2 presents a SER in SRAM 6T and 8T of 0.32 SEUs/s and 0.39 SEUs/s respectively.

Table IX Measured SER and cross-sections in proton test on DUT_2.

	σ_{SEUm} (cm^2/bit)	σ_{SEUf} (cm^2/bit)	*SER* (SEUs/bit·s)
6T	$0.55 \cdot 10^{-14} \pm 60\%$	$1.02 \cdot 10^{-14} \pm 60\%$	$0.87 \cdot 10^{-5} \pm 60\%$
8T	$0.74 \cdot 10^{-14} \pm 46\%$	$1.22 \cdot 10^{-14} \pm 46\%$	$1.19 \cdot 10^{-5} \pm 46\%$

If we compare the number of accumulated events vs. the total ionization dose in both samples, it is possible to observe that both devices reach quite similar values at the end of the radiation campaign. We notice that DUT_1, which had been exposed to ~30 krad in the alpha source in previous tests, start before to show sensitivity to the radiation. The DUT_1 increase quickly from 30 krad to 90 krad and tends to saturate around 120 krad. DUT_2 seems to increase from 90 krad to 120 krad reaching a similar SEU count than for DUT_1. Unfortunately, we do not have enough experimental data to confirm that soft errors only appear after the samples have been irradiated over a given TID threshold value.

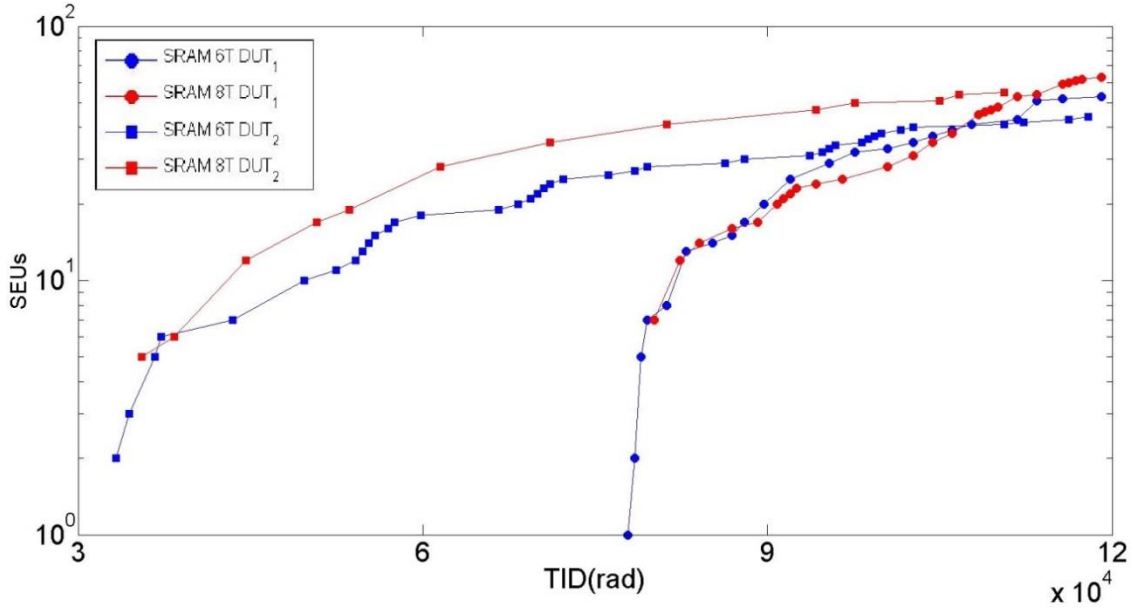


Figure 6. 7. SEUs as function of TID in two DUTs exposed to proton irradiation.

Irradiation started after the memory was initialized to a known state (The memory was initialized to all-0, logic 0 was written in all memory cells). Then, the memory content was periodically read during irradiation, obtaining a readback bitstream at each sampling time T_s. The bitstream was compared to the previously obtained one, and its content was recorded only when one or more changes were detected (together with their timestamp).

Once a readback bitstream is obtained, it is possible to assign each upset to a given bit of the SRAM core. When more than one upset appears in the same bitstream, the event is defined as an MBU while the other classes are classified as SEUs. Note that we have not considered if the affected bits are or not in the same word, so with this method it is not possible to distinguish between truly MBUs and two or more single bit upset generated from independent events. The later can be estimated from the probability of having coincident single bit upsets (SBUs), as a function of the percentage of the array that has experience a single event upset, as shown in Figure 6. 8 [WIR14].

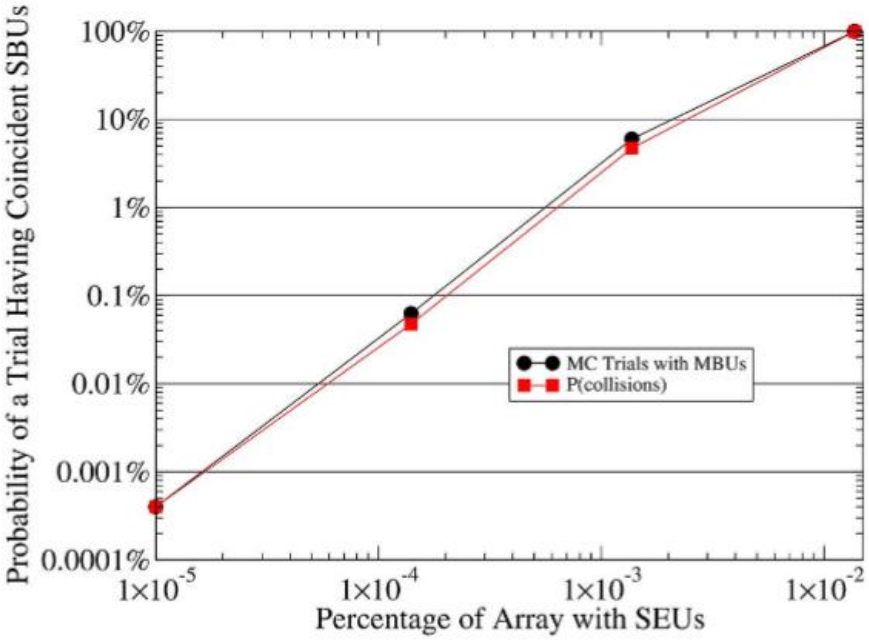


Figure 6. 8. Probability of an MBU or MCU as a function of the percentage of the Array that has SBUs (source [WIR14]).

Table X shows the multiple bits upsets found in each memory per reading stored.

Table X. Multiple bit upsets

		SEUs	MBU or MCU (2)	MBU or MCU (3)	MBU or MCU (≥4)	Total Events	Affected bits
DUT_1	**6T**	36	3	1	0	40	44
	8T	55	0	0	0	55	55
DUT_2	**6T**	34	9	0	0	43	52
	8T	56	4	0	0	60	64

Taking into account that the occurrence of radiation induced SEUs follow a Poisson distribution [SCH13], the relative uncertainty on the obtained SER is given by $\frac{1}{\sqrt{N}}$, where N is the number of detected events. In this experiment, this corresponds to statistical uncertainties close to 20%. Considering this imprecision, it is clear that both cell topologies present similar soft error rate levels despite the larger area occupied by the 8T cells.

The analysis of the readback bitstream allows the assignment of each upset to a given bit address in the SRAM core. Although with this method, it is not possible to distinguish between

a truly MBUs or two or more SBUs generated from independent events; it is possible to determine the probability of a trial having coincident SBUs by looking to the number of bit-cells with SEUs (p) within a collision range (k) in a given bitstream, and the total number of bit-cells (n) [TAU09].

$$prob_k(n, p) \approx 1 - e^{\left(\frac{-p(p-1)(2k-1)}{2n}\right)} \qquad \textbf{6. 14}$$

In our case, the readback period was selected according to the particle flux to reduce the number of upsets per readback. Therefore, in our experiments, as the size of our memory was 64x256 and the maximum number of SEUs detected in a readback was 9, it was obtained a 0.05% worst-case probability of incorrectly identifying a multiple SBUs as an MBU, see Figure 6. 8, while it was usually below 0.012 %.

Figure 6. 9 and Figure 6. 10 show the evolution of the number of events produced in each SRAM during irradiation together with the number of affected bits (the difference between both values is due to MBU occurrence) in the DUT_1 and DUT_2 respectively.

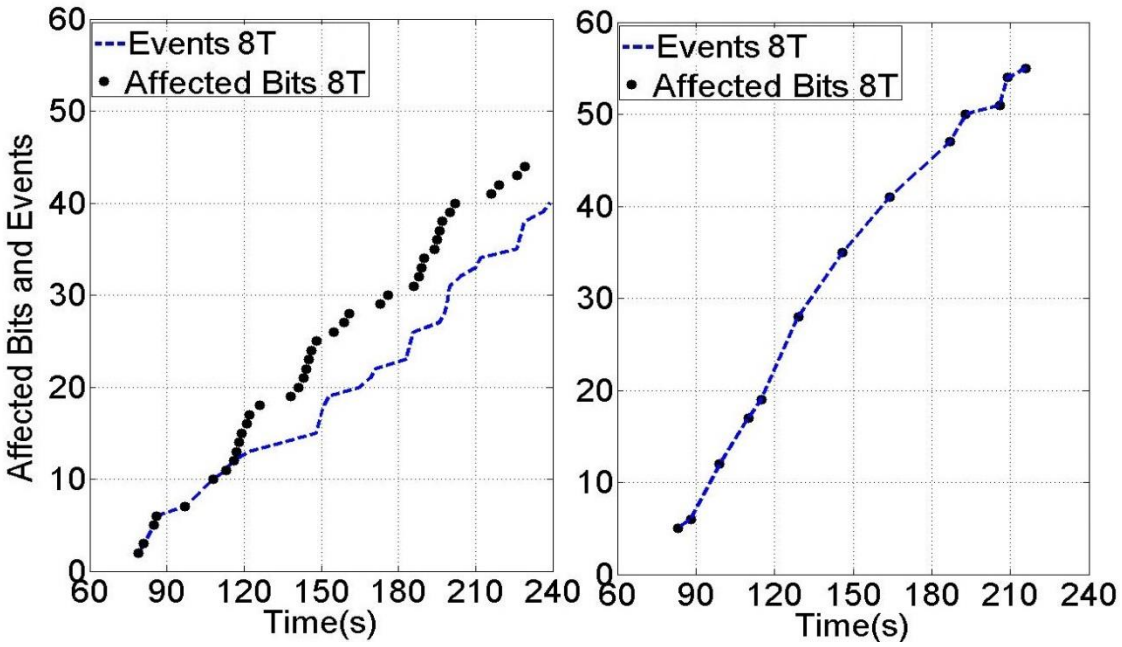


Figure 6. 9. Number of SEUs and MBUs, and the number of affected bits by proton irradiation vs time in DUT_1.

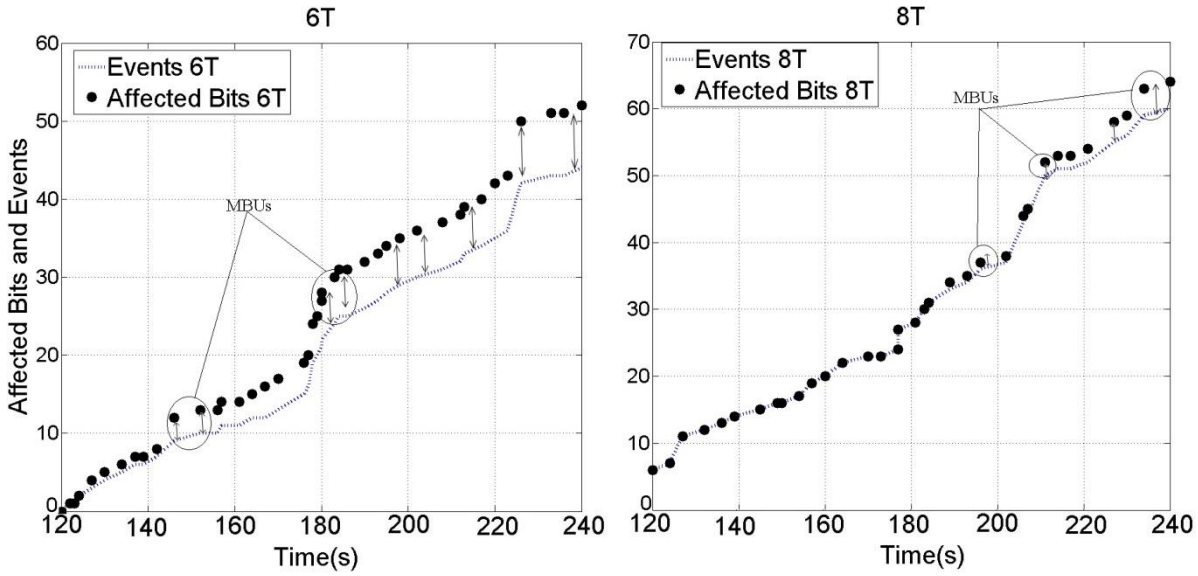


Figure 6. 10. Number of SEUs and MBUs, and a number of affected bits by proton irradiation vs time in DUT_2.

The number of events is similar in both devices; however, it is interesting to note that the percentage of MBUs is larger in 6T memories than in 8T. Such behaviour may be related to the effect of the added read port in the 8T cells, (see Figure 5. 8) as it does not contribute to generating new events, but prevents the occurrence of multiple ones.

Figure 6.11 shows the placement of all the measured events for each SRAM in each experiment together with the presence of MBUs (circles). Experimental data analysis reveals that the major number of events produced were SBUs, although the presence of MBUs was noticeable in 6T SRAMs (Table X). Most of 2-bit MBUs detected involved two adjacent cells of the same column, followed by the occurrence of two adjacent cells in diagonal, and two cells in a row (note in Figure 5. 9 that the distance between the sensitive active areas of two adjacent cells of the same column is lower than the distance between two adjacent cells of the same row).

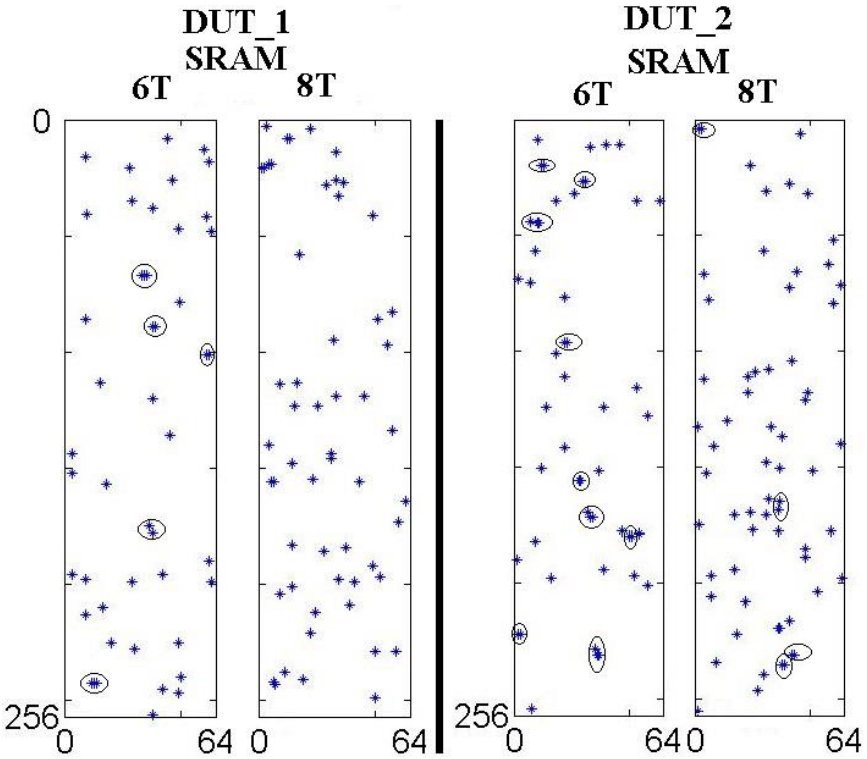


Figure 6. 11. Bitmap of detected SEUs produced by proton irradiation. Circles denote the presence of MBUs.

6.5 Neutron irradiation tests: SEU/MBU results

Measurements were performed at Tandem CNA facility with the objective of characterizing the SRAM response to epithermal neutrons (~30keV) and intermediate energy neutrons (below and close to 10MeV).

6.5.1 Epithermal neutrons

The first neutron irradiation was performed with epithermal neutrons with energies distributed according to a maxwellian spectrum of 30 keV average energy. The production was estimated about 2.0×10^{9} neutrons/cm^2·s and, assuming that the neutron source-device distance was 7 mm, the flux in the device was 1.0×10^{7} neutrons/cm^2·s. The total fluence in 6 hours was approximately $2.2\cdot10^{11}$ neutrons/cm^2, bigger than fluence corresponding to the fast neutrons case, which will be present below.

No SEUs were detected in the SRAM after a 6 hours exposition, indicating that the energy delivered by epithermal neutrons due to elastic collisions with the crystal lattice was unable to induce side reactions capable of producing ionizing particles after interacting with the chip

material. This result cannot be extrapolated to neutrons of lower energy, since the cross-section of a 1 eV neutron, is more than 100 times greater to that of a neutron of 30 keV [MUG12].

6.5.2 Fast neutrons

In a second neutron irradiation experiment, the samples were irradiated during ~6 hours with a neutron beam flux with energy range comprised between 5.3 to 8.5 MeV as it is shown in Figure 3.12. The total flux equivalent for the non-monochromatic beam is calculated using the equation 6.15,

$$\emptyset_{Nmix} = \int_{E=5.8}^{E=8.5} \emptyset(E)dE \qquad \textbf{6. 15}$$

where $\emptyset_{Nmix}$ is the total neutron flux $(n_{5.8}^{8.5} cm^2 \cdot s)$ for the non-monochromatic beam of energies from 5.8 to 8.5 MeV. The non-monochromatic beam flux was $6.04 \cdot 10^6$ n/cm^2·s,

In that case, due to time availability to the neutron facility, only a sample was characterised. The total ionization dose, in rads, caused by neutrons is given by [KTH09]:

$$D_{Nmed}(rads) = 1.603 \cdot 10^{-5} \cdot \emptyset \cdot E(MeV) \cdot \sum_i N_i \varepsilon_i \sigma_i \qquad \textbf{6. 16}$$

being Φ the neutron fluence in n/cm^2, N_i the number of atoms/g of ith species in the material, ε_i is the fractional neutron energy transfer to the nucleus and σ_i the elastic scattering cross section in barns (10^{-24} cm^2) [KTH09]. It is important to highlight that this equation takes into account only the first collision interaction between the neutrons and the target material and does not include secondary or other higher-order collisions. As discussed in the section 2.6.6, the proton TID obtained by secondary particles in a neutron irradiation fluence of ~10^{11} was ~$3 \cdot 10^5$ p/cm^2, not higher of 25 krad.

The number of atoms/g of the ith specie in the target can be estimated from the technological parameters of the CMOS technology (thickness and density of the silicon bulk, SiO_2 layers, copper and aluminium layer). The fractional neutron energy transferred to the nucleus ε_i after a collision is given by:

$$\varepsilon_i = \frac{2 \cdot M_t \cdot M_n}{(M_t + M_n)^2} \cdot (\cos^2 \theta) \cdot E_{in} \qquad \textbf{6. 17}$$

where the angle θ is the angle between the recoil and a target nucleus, E_n is the energy of the incoming neutron before it interacts with the nucleus target, and M_t is the mass of the target nucleus (atomic mass).

In the worst case, the maximal energy transferred to the target nucleus in the circuit layers is,

$$\boldsymbol{\varepsilon_{imax} = \frac{2 \cdot M_t \cdot M_n}{(M_t + M_n)^2} E_{in}} \qquad \textbf{6. 18}$$

According to this, the following expression has been used to compute the TID related to the neutron irradiation:

$$\boldsymbol{D_{Nmed}(rads) = 1.603 \cdot 10^{-5} \cdot \left[\sum_j \emptyset_j \cdot E_j\right] \cdot \left[\sum_i N_i \varepsilon_i \sigma_i\right]} \qquad \textbf{6. 19}$$

Neutron elastic scattering cross sections for the elements present in the target circuit are obtained from [MUN13]. Taking into account that the total neutron beam fluence was ~$1.33 \cdot 10^{11}$ n/cm^2, beam energy was in the range between 5.8 and 8.5 MeV, and index i refers to the predominant elements presents in the target, such as Aluminium, Silicon, Copper or Oxygen, the total dose in rads obtained with equation 6.19, was below 8 krad. So adding this value to the 25 krad produced by secondary protons, the limit of 120 krad was not exceeded.

Setup and experimental method were the same used than for the proton irradiation experiment. Considering that SEUs were related to those bit-cell that changed its logic state, the evolution on the number of cells that change its state during the irradiation is shown in the Figure 6.12

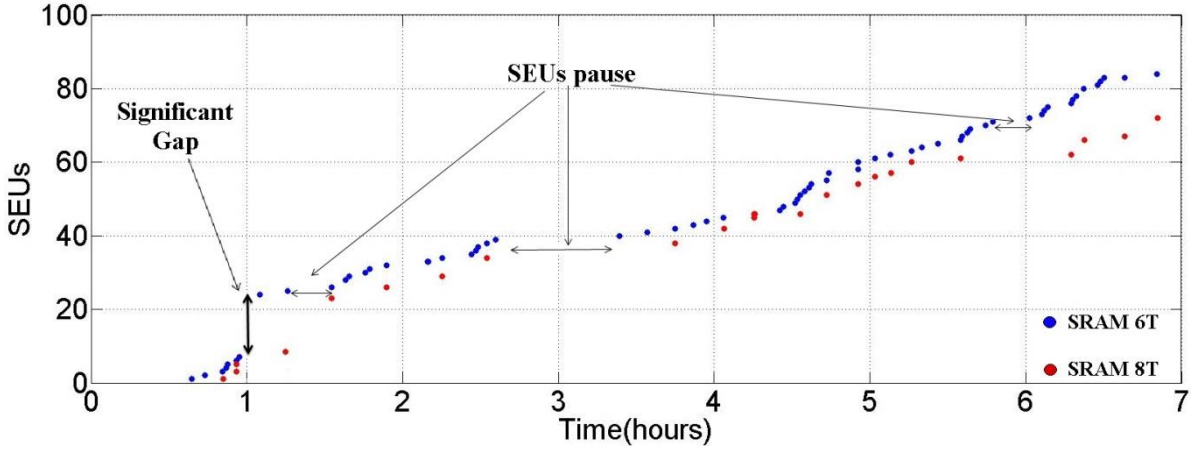


Figure 6. 12. Number of SEUs by neutron irradiation vs time in both SRAMs 6T and 8T.

At t=1 hour, we note the presence of a significant gap in the 6T SRAM memory, after that, the number of SEUs differ in small quantities compared with that gap. We also note the presence of dead-time intervals in which no SEUs are collected in any of the SRAM. Both, deuterium beam and SEU collection are shown in the Figure 6. 13 as a function of time, where we observe that dead-time intervals are related with neutron beam interruptions.

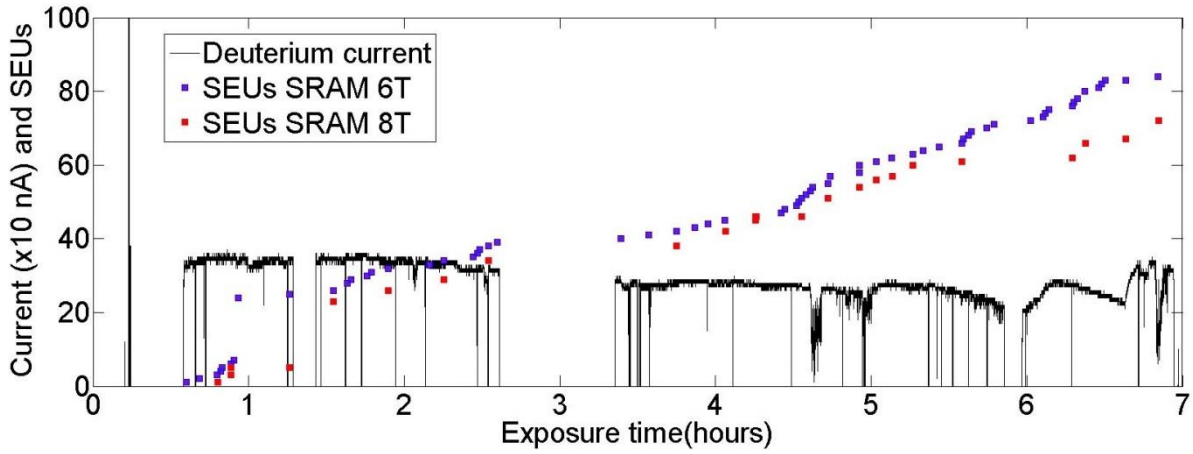


Figure 6. 13. Deuterium current measured from the TiD_2 target and SEUs detected in both SRAM.

Figure 6. 14 presents the estimated cross section as function of the fluence (after processing raw data to correct the effects of dead-time intervals).

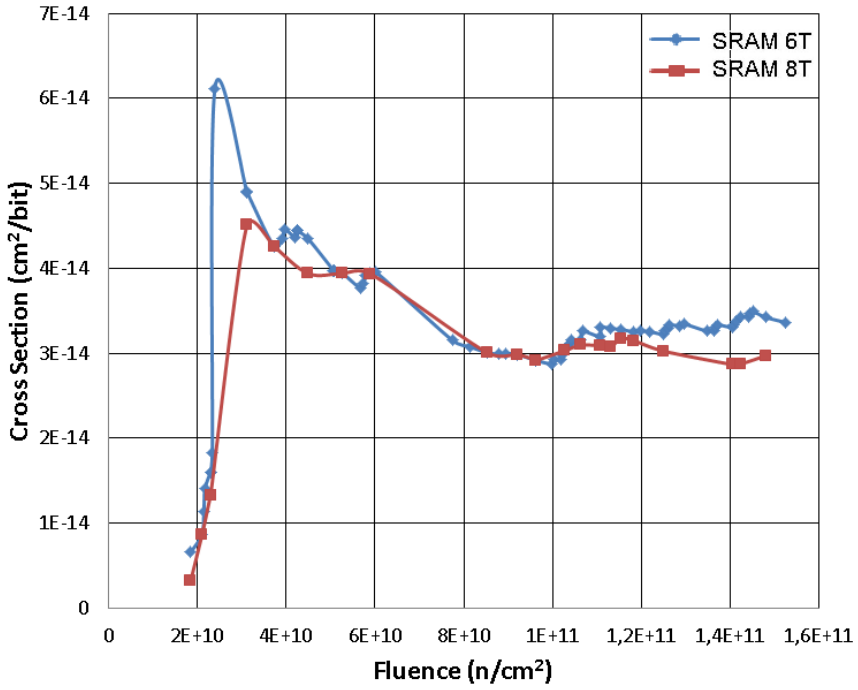


Figure 6. 14. Cross Section as a function of the fluence in fast neutron irradiation.

The cross section values (medium cross section and final cross section) and SER values are presented in Table XI.

Table XI. Measured SER and cross-sections in neutron test.

	σ_{SEUm} (cm^2/bit)	σ_{SEUf} (cm^2/bit)	*SER* (SEUs/bit·s)
6T	$3.37 \cdot 10^{-14} \pm 30\%$	$3.36 \cdot 10^{-14} \pm 30\%$	$2.24 \cdot 10^{-7} \pm 30\%$
8T	$2.78 \cdot 10^{-14} \pm 37\%$	$2.97 \cdot 10^{-14} \pm 37\%$	$1.7 \cdot 10^{-7} \pm 37\%$

We found that in the energy range between few MeV and 10 MeV, the neutron cross-sections are in the same order of magnitude as in previous studies below 20 MeV, see Table XII.

Table XII. Reported neutron cross-sections cm^2·bit

	Feature size	Device Size	Neutron energy	Cross-section (cm^2/bit)
J. Baggio et al. [BAG04]	**0.5 µm**	**1 Mbit**	**14 MeV**	$\mathbf{3.77 \cdot 10^{-14}}$
	0.25 µm	**1 Mbit**	**14 MeV**	$\mathbf{(2.95–5.51) \cdot 10^{-14}}$
	0.18 µm	**4 Mbit**	**14 MeV**	$\mathbf{3.99 \cdot 10^{-14}}$
F. Irom et al. [IRO07]	**90 nm**	**NA**	**14MeV**	$\mathbf{1.3 \cdot 10^{-14}}$
	90 nm	**16 Mbit**	**14 MeV**	$\mathbf{3.9 \cdot 10^{-16}}$
S. Danzeca et al. [DAN14]	**90 nm**	**8 Mbit**	**5 MeV**	$\mathbf{0.93 \cdot 10^{-14}}$
	90 nm	**8 Mbit**	**8 MeV**	$\mathbf{2.16 \cdot 10^{-14}}$
	90 nm	**8 Mbit**	**14 MeV**	$\mathbf{1.09 \cdot 10^{-13}}$
D. Lambert et al. [LAM09]	**65 nm**	**NA**	**1-20 MeV**	$\mathbf{2 \cdot 10^{-16}–3 \cdot 10^{-14}}$

In order to identify the sensitivity to MBUs in both architectures, we analysed the number of upsets after each memory read-out (Table XIII). The method used to detect MBUs is the same one described in the Proton irradiation case.

Table XIII. Multiple bit upsets.

		SEUs	MBU or MCU (2)	MBU or MCU (3)	MBU or MCU (≥4)	Total Events	Affected bits
SRAM	**6T**	**60**	**4**	**0**	**3**	**67**	**84**
	8T	**56**	**0**	**0**	**1**	**57**	**67**

An MBU was found in the SRAM 8T which was detected coinciding with the current peak shown in Figure 6. 13. Seven MBUs were found in the SRAM 6T, one of them was collected close to the peak current. Both MBUs have the identical magnitude and were read in the same instant of time. In order to avoid corrupt data from fluences not included in the experiment, this contribution was neglected in both SRAMs due to that this peak of current was not characterized in energy terms.

Figure 6. 15 shows the evolution of the number of events produced in each SRAM during irradiation together with the number of affected bits (the difference between both values is due to MBU occurrence).

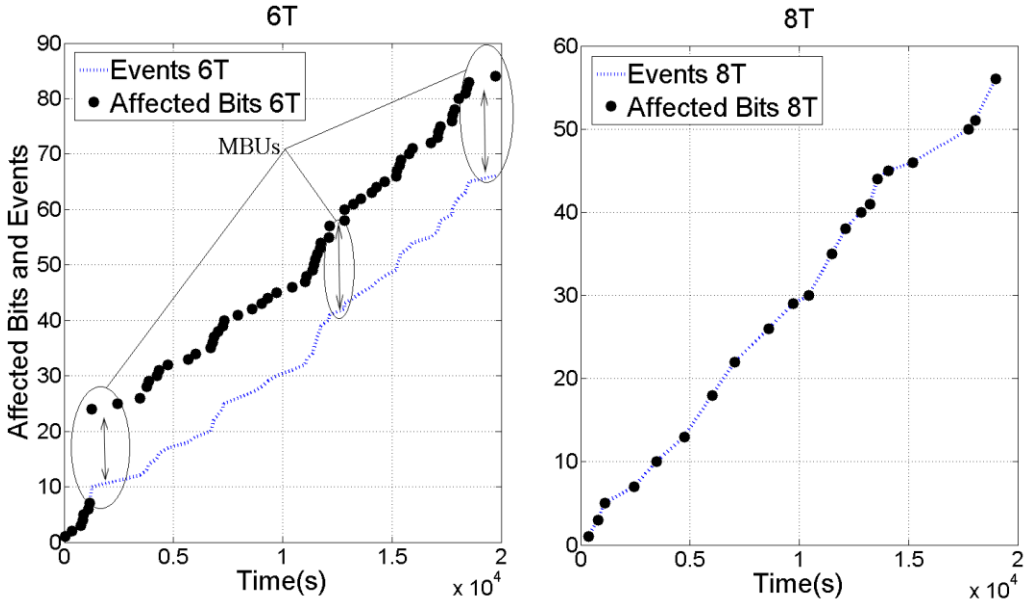


Figure 6. 15. Number of SEUs and MBUs, and number of affected bits as a consequence of neutron irradiation

Although most events were SBUs, the percentage of MBUs is larger in 6T memories than in 8T (Table XIII). As in the proton irradiation, most of 2-bit MBUs detected involved two adjacent cells of the same column, followed by the occurrence of two adjacent cells in diagonal, and two cells in a row.

Figure 6. 16 shows the placement of all the measured events for each SRAM in each experiment together with the presence of MBUs (circles).

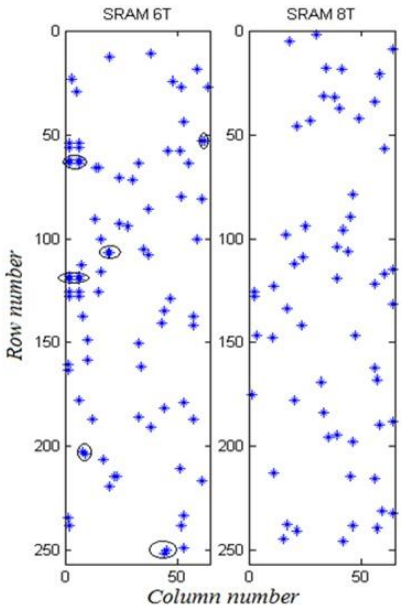


Figure 6. 16. Placement of detected SEUs produced by neutron irradiation. Circles denote the presence of MBUs.

6.6 CHARM: mixed-field test

A new sample with the described SRAM 6T and SRAM 8T devices was tested in the CHARM radiation facility at CERN (see section 3.2 for details about this facility).

Table XIV compares the approximate annual HEH flux values in different level altitudes and in the LHC tunnel at CERN; it is concluded that the mixed hadron field tests at CHARM correspond to fluence magnitudes similar to those obtained during a year in a low-Earth orbit (LEO).

Table XIV. HEH annual fluxes for different radiation environments (source [GAR14]).

Spectrum	$\emptyset_{HEH}(/cm^2/yr)$
Ground level	$1\text{-}2 \cdot 10^5$
Avionics	$\sim 2 \cdot 10^7$
ISS Orbit	$\sim 7 \cdot 10^8$
Polar LEO orbit (800 km)	$\sim 3 \cdot 10^9$
LHC	$\sim 10^6\text{-}10^{12}$

As it was discussed in 3.2,2, the data in the CHARM environment comes from four different test, which reached fluences from $\sim 2 \cdot 10^9$ HEHeq/cm^2 to $\sim 5 \cdot 10^{10}$ HEHeq/cm^2.

Due to an issue in the setup connection, the data corresponding to one of the bits of the SRAM output word was lose. The issue affected all tests performed at CHARM as it was not possible to access the irradiation room during the whole irradiation period. Therefore, only 7×8×256 bit-cells were used when calculating the cross sections and SERs.

Any SEU was observed during the first test (about~3 hours long).

In the second test the sample was exposed to radiation during ~90 hours. Figure 6.17 shows the evolution of affected bit-cells in both 6T and 8T SRAMs . SEUs start to appear after an initial period of ~18 hours of exposition without events. There is a second time interval of ~41 hours without events (between t=23 h, and t=64 h), this is explained in terms of flux interruptions during the experiment (Figure 6.18), the flux was stopped between t≈30 h, and t≈60 h. Finally, new events, including MCUs, were detected again in the last interval of ~21 hours. Again, it seems that the SER depends not only on the flux or particle energy but also on the TID.

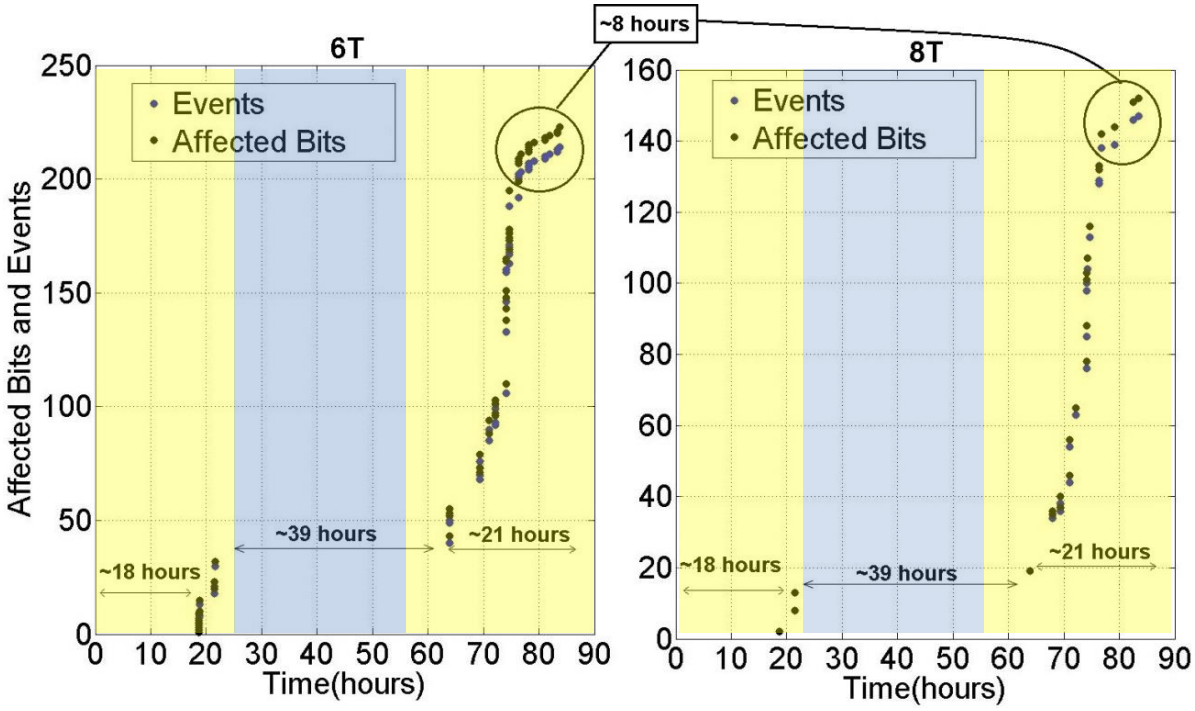


Figure 6. 17. Number of SEUs and MBUs, and a number of affected bits as a consequence of HEH_{eq} irradiation. The differently shaded regions represent no irradiation time(blue) and irradiation time (yellow).

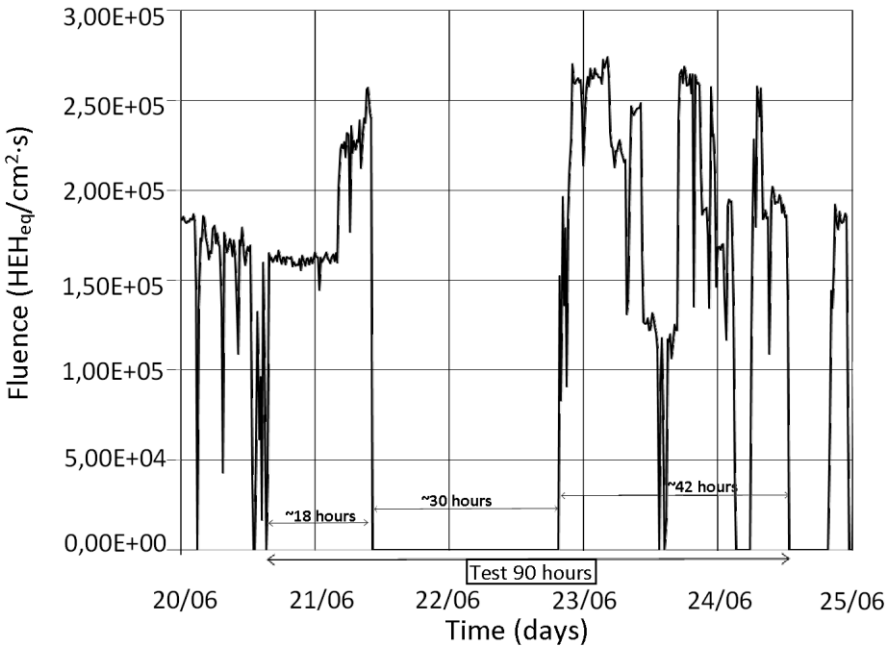


Figure 6. 18. Fluence environment in CHARM test area during the 90 hours irradiation.

According to the Figure 6.18, the total fluence in this test was ~$4 \cdot 10^{10}$ HEHeq/cm^2.

In order to compute the TID related to the HEH_{eq} experiment, we considered that the accumulated dose is due to irradiation of protons in the energy range comprised between 1 MeV to 1 GeV as shown in Figure 6.18 and from protons with energies between 5 GeV to 500 MeV generated by neutron scattering with atoms present in the semiconductor device (from CRÈME/geant4 simulations [CRE96]). Charge collection effects have been obtained using equation 2.12 and LET calculator [ZAI04]. The primary protons are responsible for generating a collected charge comprised from 2.8 to 400 fC, on the other hand a collected charge from 2.6 fC to 3.5 fC can be attributed to secondary protons (assuming a path length of 150 µm for protons). Finally, we get a TID below 3 krads after the second irradiation period.

The cross section in both SRAMs as a function of the HEH_{eq} dose is shown in Figure 6.19.

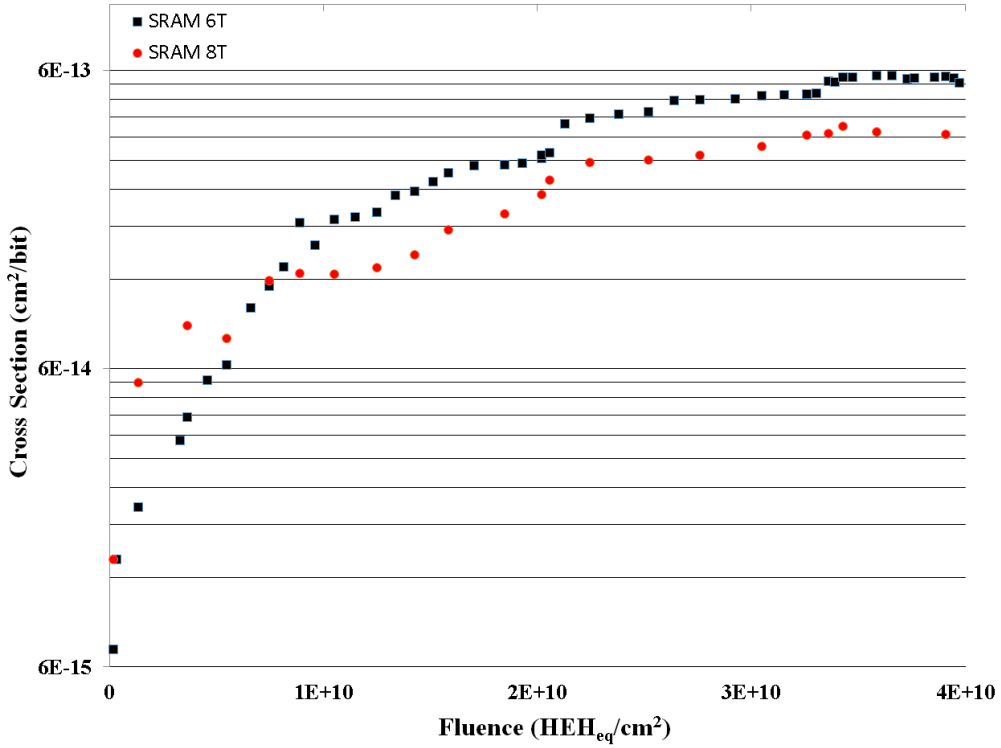


Figure 6. 19. Cross Section as a function of the fluence in HEH_{eq} irradiation.

The cross section values (mean cross section and final cross section) are presented in Table XV.

Table XV. Cross-sections in HEH_{eq} 90 hours test.

	σ_{SEUm} (cm^2/bit)	σ_{SEUf} (cm^2/bit)
6T	$3.57 \cdot 10^{-13} \pm 55\%$	$5.36 \cdot 10^{-13} \pm 55\%$
8T	$2.27 \cdot 10^{-13} \pm 54\%$	$3.67 \cdot 10^{-13} \pm 54\%$

Note that the values shown in Table XV refer to the total number of affected bit-cells. It is also interesting to observe that, although the fluence is lower in the HEH_{eq} test, the collected charge generated by a particle hit could be greater than in the previous neutron irradiation or proton irradiation experiments due to broader energy spectrum, as seen in Figure 3. 18, the HEH_{eq} spectrum contains energy ranges, which produce a higher LET able to deposit higher charges in the SV, (equation 2.12)

To identify the sensitivity to MBUs in both SRAM architectures, the number of bits affected in each event has been analysed (Figure 6.20), using the method already described in the proton case.

Table XVI. Multiple bit upsets.

		SEUs	MBU or MCU (2)	MBU or MCU (3)	MBU or MCU (≥4)	Total Events	Affected bits
SRAM	6T	205	9	0	0	214	223
	8T	142	5	0	0	147	152

Figure 6. 20 shows the placement of all the measured events for each SRAM in HEH_{eq} experiment of 90 hours together with the presence of MBUs (circles).

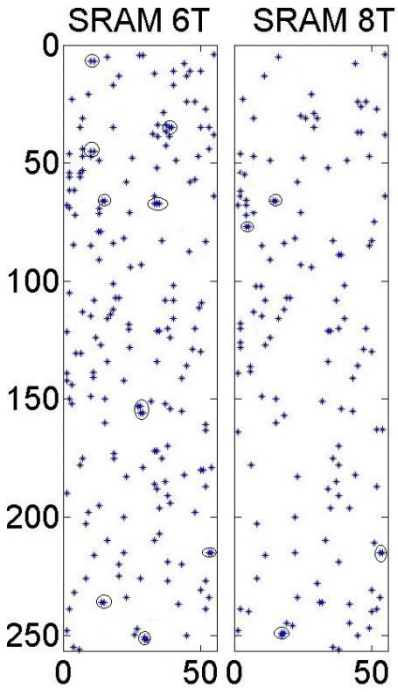


Figure 6. 20. Bitmap of detected SEUs produced by HEH_{eq} irradiation. Circles denote the presence of MBUs.

A third irradiation period of ~12 hours was performed after several days of the second irradiation sequence. The mean flux during the test was ~$2 \cdot 10^5$ $HEH_{eq}/cm^2 \cdot s$ (slightly above the ~$1.5 \cdot 10^5$ $HEH_{eq}/cm^2 \cdot s$measured in the second irradiation sequence of ~90h). It is important to remark that the DUT remained in the CHARM room and was exposed to radiation during the 15 days comprised between the second and third irradiation sequences (no events were produced during this time interval as the memories were unbiased).

Table XVII. Multiple bit upsets.

		SEUs	MBU or MCU (2)	MBU or MCU (3)	MBU or MCU (≥4)	Total Events	Affected bits
SRAM	6T	97	3	3	2	100	120
	8T	69	1	0	0	70	71

As in the cases of monoenergetic sources, the total number of events involving multiple bits in 6T devices is higher than in 8T ones, see Table XVII.

The higher cross-section observed in the experiment performed at CHARM can be justified by the presence of pions, which have not been considered in our previous analysis. However, pion contributions in the atmospheric environment are below 1%, even at the highest altitudes [GAR14], (pions created through the interaction of high-energy hadrons with aircraft materials are not included in the percentage). Pions are typically present in the CHARM environment, see Figure 3. 18, and it has been reported that the soft error rate related to pions is twice that of protons at 200 MeV.

Figure 6. 21 shows the simulated differential contribution of each hadron as a function of energy according to the ESA SEU Monitor model in the H4IRRAD[2] environment, which can be considered similar to CHARM environment as both are mixed-fields [GAR14]. Furthermore, pions have an inelastic interaction resonance around 150 MeV, giving rise to a greater number of errors than those related to neutrons and protons.

[2]The H4IRRAD test area at CERN is typically used to generate a mixed radiation field through the interaction of several hundred GeV energy beams with a target and, before the construction of the CHARM test facility, it was used to similar SEE tests.

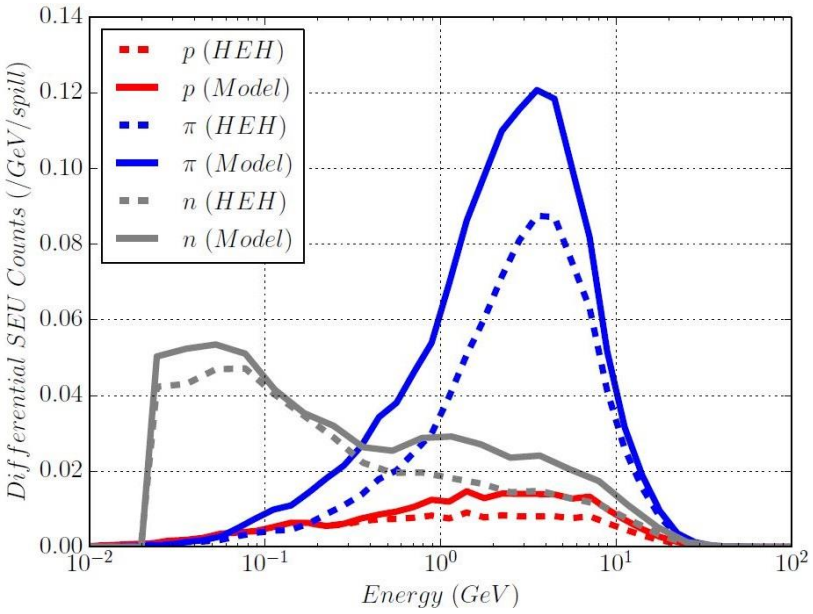


Figure 6. 21. Simulated contribution to the total SEU rate per HEH type as a function of energy, both for the HEH approach and the model output. One spill corresponds to 10^9 protons on target, source [GAR14].

6.7 Conclusion

The cross sections of the memory with protons (18 MeV), thermal neutrons, intermediate neutrons (5.8-8.5 MeV) and HEH mixed-field have been measured for two samples. The cross section for neutrons in the 5.8-8.5 range is ~3 times higher than for 18 MeV protons. The cross section for mixed-field in larger energy range is between 10 and 30 times higher than for neutron in the 5.8-8.5 range, as in HEH irradiation it is observed a dependency with the accumulated TID, observing an increase in the cross section above ~$9 \cdot 10^{10}$ HEH_{eq}/cm^2.

The tests show that these SRAM memories could be a good candidate to be used as HEH monitors. Despite being a COTS device, the SRAM did not show any latch-up below a fluence of $1.7 \cdot 10^{11}$ HEHeq/cm^2 and are working until TID values up to 120 krad (Si). These levels are better than the current radiation monitoring system equipped at the LHC tunnel, the so-called RadMon system [SPI14]. Moreover, the thermal neutron contribution to the total number of SEUs can be neglected, as it was not observed sensitivity to thermal neutron at CNA. This feature could be a significant advantage in order to be able to distinguish the contribution of HEH from thermals to the radiation field.

The cross section for 6T and 8T SRAMs used in this thesis show a cross section between 2 and 4 times higher than the SRAM chip previously used on the RandMon [DAN14], permitting to

significantly increase the resolution of the HEH fluence measurement and with less maintenance tasks[DAN14].

In order to use these SRAMs as a particle detector, it could be recommended as a neutron detector, as sensitivity to neutron seems to have an acceptable resolution, see Figure 6. 22. One of the many benefits of using SRAMs as neutron detectors is that they do not produce SEUs in response to gamma or beta radiation, and it is known that they are often in radiation environments where neutrons are present.

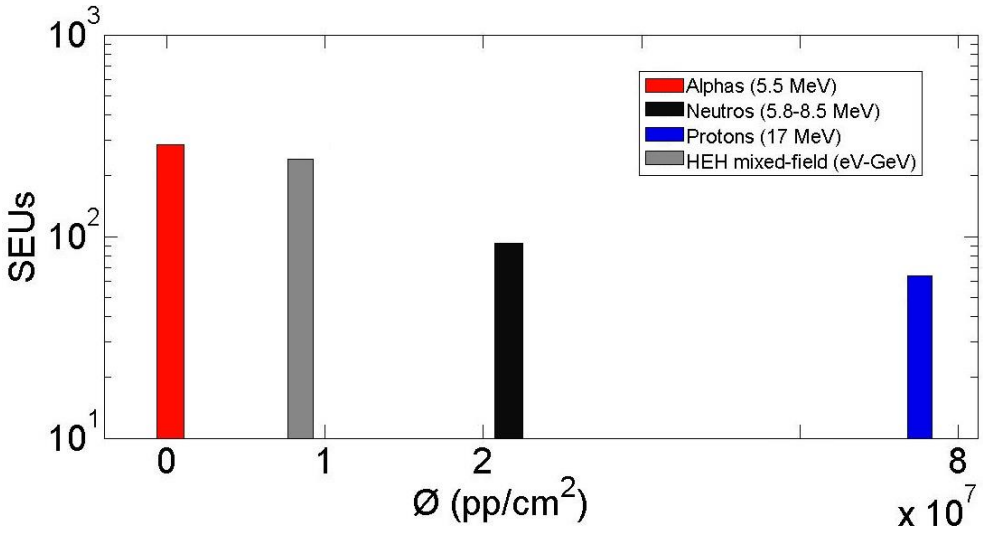


Figure 6. 22. SEU comparison as function of fluence for different particles and energies on DUTs.

In proton tests and in the mixed-field tests we observed that SEU events appear after a certain TID level has been reached, although we believe that more experiments are needed to confirm this hypothesis.

Our results also indicate that the total number of multiple bits affected in 6T devices is higher than in 8T ones, i.e. 8T memories are more robust in terms of MBUs. MBUs make the implementation of error correction more difficult, and consequently, if error detection and correction techniques were adopted, they would be more effective in 8T SRAMs than in 6T ones. According to the results, it is expected that in a mixed field, due to the large range in energy particles, the SEU contribution is proportioned by particles from lower energies, and the MBU contribution is associated with higher energies. Therefore, in order to differentiate between low and high energies, the combination of both 6T and 8T SRAMs could play a role

that makes this DUT in a good candidate to identify if radiations are composed by high particles or low particles.

CHAPTER 7

CONCLUSIONS AND OUTLOOK

7.1 Thesis summary

This thesis is focused on the analysis of the SEE rate calculation and comparison between 6T and 8T memory cells implemented on a 65 nm commercial CMOS IC technology. However, in order to introduce the analog part in the physical process of transmission of information, a ΣΔ modulator is also introduced in the work, and it is shown that high-order single-loop modulators are only conditionally stable, demonstrating that instability can be triggered by SET, for reasonable levels of injected charge.

SRAM memories are elements present in many electronic systems. In addition, although the dimensions of the devices forming the SRAM cells have decreased in each successive technological generation, the number of cells used has increased at a higher rate. The growing demand for memory in complex Systems on Chips has caused that a large part of the silicon area is dedicated to SRAM memory, thus, system reliability largely depends on these modules.

Among all the effects of radiation, this thesis focuses on the transient events in SRAM memories or ΣΔ Modulators and, more specifically in the so-called Single Event Upset (SEU) and Single Event Transient (SET) which, the first one consists of the corruption of the information stored in an SRAM cell and the second one consists in a momentary voltage spike at a node in semiconductors produced by the electric field separation of the charge induced, both effects caused by the interaction with an energetic particle. These effects are not destructive and although this can cause a loss of data, which in turn can cause a system failure, the affected devices can be restarted and operate normally, as long as TID effects do not overcome critical levels, which lead the devices to an irreversible state by other destructive effects.

These effects on both devices mentioned throughout this work are obviously a concern for space applications, as these environments contain high levels of particles, which can reach sensitive nodes and provoke these single events.

In the case of the study dedicated to SRAMs, experimental and simulation results are used in combination in order to quantify the derived SEE cross section and to estimate the error or failure rate in a given operational context.

Different radiation environments have been used in this thesis at different facilities as the Cyclotron and Tandem at the Spanish National Accelerator Facility (CNA) in Seville and the CERN High-Energy Accelerator Mixed-field (CHARM) radiation facility, Geneva. Among all types of radiation, those sources that compare with real space environments have been identified. There are four types of radiation that cause most of the soft errors in SRAM memories according to the experimental data obtained:

(i) Alpha particles emitted by the constituent elements of the circuit itself or its encapsulation.
(ii) Protons interacting with the atoms of Silicon.
(iii) Fast neutrons interacting with the atoms of Silicon.
(iv) Pions interacting with the atoms of Silicon.

At the same time, we want to highlight other interesting results obtained in the thesis:

- We did not detect single event upsets in the radiation experiments carried out with low-energy neutrons (~30 keV) which are able to interact with the Boron atoms present in the circuit. The results provide a Soft Error Rate comparison between 6T and 8T memory cells implemented on a 65 nm commercial CMOS IC technology. SEU events were observed after irradiation with 17 MeV monoenergetic protons and neutrons in the range from 5.8-8.5 MeV thus confirming the presence of neutron-induced SEUs in the 1-10 MeV energy range.

- An irradiation experiment was carried out with a high-energy mixed-field accelerator at CHARM with a broader set of particle species as protons, neutrons or charged pions (with a spectra extended to the GeV range). Experimental results show that environments which contain larger operational energies range will increase the cross-section (and thus the risk to experiment soft-errors), simulation results suggest that a contribution to the observed cross-section increase should be attributed to the presence of pions.

- The presence of MBUs is more evident when the SRAM is exposed to high energy particles, an effect that is more pronounced in 6T cells.

- The cross-section values obtained from the 6T cells experimental results were in agreement with previously published values. Results show that regardless the number of transistors composing the memory cells, the total number of events recorded is quite

similar as far as the devices are equally sized. However, the percentage of MBUs is clearly higher in 6T than in 8T given the inherent higher density of 6T in addition to the isolation provided by the read circuitry in 8T.

- The occurrence of MBUs is a factor hindering the implementation of Error Correction Codes for memory hardening. Remembering the results provided in [BOT15] reporting that SER during alpha particle irradiation improves when reducing the pull-down transistor width of the bit-cell, so that, their conclusion about the fact that 8T memories offer a better performance against radiation than 6T (as 8T bit-cells can be implemented with minimum-size nMOS pull-down devices given their dedicated read-port) results reinforced with our experiments.

- Another interesting result is that SRAMs disclosed neutron vulnerability during radiation sensitivity tests at CNA.

- It has been demonstrated that instability can be triggered by SETs in ΣΔ Modulators. In such a case, the performance of the A/D converter is greatly decreased but not necessarily easily detected from the output bit-stream. This implies that a SET could lead to long-term wrong acquisitions.

7.2 Future work

Nowadays, the availability of new devices, which enable the possibility of particle detection in a broader range of radiation fields has become crucial, for example in environments subjected to high levels of radiation such as high-energy physics environments.

SRAM devices have been used to detect charged particles as protons [MAK07]. These sensors should have sensitive volumes to ensure a uniform response over the active area and measurement in real time. Another characteristic should be to have good enough sensitivity and dynamic ranges and should be preferably equipped with a digital interface to enable easy connection with the SRAM devices to a computer network.

The SRAMs exposed in this thesis shows that data measurement in a few different places and accelerator facilities can be monitored and sent to the main computer and gather in a database

for future display and analysis, but the setup could be modified to work in real time and to be used as a radiation particle detector.

Several subjects of future research interest related in the study presented in this thesis are listed below.

First of all, to resolve the issue in the connections from chip and SRAMs in order to have the availability of use this DUT at another distinct facilities tests. It would be interesting to try a larger time test at CHARM and also try other rack positions, which have different radiation spectra exposition. A 24 GeV proton measurement would be interesting in order to find the MBUs sensitivity to high energies, and this kind of tests is possible at CHARM as well.

To setup a test in which monoenergetic pions are dominant in the environment also an interest means of benchmarking the SEU models here obtained and therefore, more accurately determining their potential impact upon the SEU rate.

In particular, whereas this thesis concentrates mainly on SEU effects in digital components as SRAMs, other failures in electronics such as SETs are, likewise, highly relevant for the system radiation hardness assurance. Therefore, it would be pertinent to extend this study to such effects, notably through measurements to other devices as analogue systems, using future setup designs to check ΣΔ Modulator exposed in chapter 4 on facility tests. Further work will be focused on the experimental verification of the described effects through pulsed-laser testing or particle accelerator facility, and unlike the use of SRAMs, in this case, on the development of design methods to mitigate the consequences of these effects.

We observe in an individual experiment at CHARM (during 12 hours exposition, just after of a 90 hours test), that the cross-section values seem to increases to higher radiation doses. Due that it was not possible to confirm with other tests, these were not present in this work, but this would be a subject of potential research interest related to the study presented in this thesis in order to observe dependence between cross section and the TID. This information would conclude that SRAMs became more sensitive to SEUs as it accumulates dose, while no Latch up was observed.

Likewise, devices which use new materials are also a potentially relevant subject to further study based upon the work here presented, because of the potential impact on the radiation hardness assurance.

Furthermore, it would be of interest to be able to continue testing the DUT under different conditions and setups in order to improve the equivalent model exposed in this thesis and to try

to get and simplify the model capable of distinguish between the contributions from the distinct particles to the soft error rate within a coherent range approximation.

Further work will be focused on the experimental verification of the described effects through pulsed-laser testing on ΣΔ modulators, and on the development of design, methods to mitigate the consequences of these effects.

7.3 List of publications

The work performed during the doctoral thesis here presented has led to the publication of one main author paper and two conference papers. The published work is listed below.

"**Soft error rate comparison of 6T and 8T SRAM ICs using mono-energetic proton and neutron irradiation sources**", D. Malagón, S.A. Bota, G. Torrens, X. Gili, J. Praena, B. Fernández, M. Macías, J.M. Quesada, Carlos Guerrero Sanchez, M.C. Jiménez-Ramos, J. García López, J.L. Merino, J. Segura, In Microelectronics Reliability, Volume 78, 2017, Pages 38-45.

Abstract: We present experimental results of soft errors produced by proton and neutron irradiation of minimum-size six-transistors (6T) and eight-transistors (8T) bit-cells SRAM memories produced with 65nm CMOS technology using an 18MeV proton beam and a neutron beam of 4.3–8.5MeV. All experiments have been carried out at the National Center of Accelerators (CNA) in Seville, Spain. Similar soft error rate levels have been observed for both cell designs despite the larger area occupied by the 8T cells, although the trend for multiple events has been higher in 6T.

"Single Event Transients trigger instability in Sigma-Delta Modulators", D. Malagon, J. M. de la Rosa, R. del Río and G. Leger. Proceeding of the 2014 Conference on Design of Circuits and Integrated Systems, Madrid, Spain, November 2014.

Abstract: In this paper we emulate the errors caused by SET in a Flexible 4th-Order ΣΔ Modulator with DC-to-44MHz Tunable Center Frequency in 1.2-V 90-nm CMOS. We identify the virtual ground of the integrators as a sensitive node and show that a charge injection may drive the modulator into long-term instability.

"Radiation effects in nanometric SRAMs induced by 18 MeV protons", D. M. Periánez; J. L. Merino ; G. Torrens ; J. Segura ; S. A. Bota ; M. C. Jiménez-Ramos ; J. García López. "2015 10th Spanish Conference on Electron Devices (CDE)".

Abstract: This paper presents experimental results of Soft errors produced by proton interaction in SRAM memories implemented with a 65 nm CMOS technology using the 18 MeV proton facility at the National Center of Accelerators (CNA) in Seville.

"Memory State Transient Analysis (MSTA), a new Soft Error Rate measurement method for CMOS memory elements based on stochastic analysis." Sebastià A. Bota, Senior Member, IEEE, Gabriel Torrens, Jaume Verd, Senior Member, IEEE, Josep L. Merino, Daniel Malagón-Periánez, and Jaume Segura, Member, IEEE. IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 62, NO. 6, DECEMBER 2015.

Abstract: We analyze the evolution of SRAM memory logic contents under irradiation by defining the memory state as the number of cells storing a given logic value (i.e. number of cells storing a logic-1). We find that the memory state evolution under irradiation follows an Ehrenfest urn model due to the constant effect of single event upsets, and that in large memories it can be associated to an Ornstein-Uhlenbeck process. Memory state transient analysis has been applied to determine the device Soft error rate for an SRAM fabricated in a 65 nm commercial CMOS process obtaining a very good correlation. Furthermore, our analysis shows that the technique is applicable to systems composed by various dissimilar memory components, providing-under certain circumstances-the specific Soft Error Rate of each component.

"65-nm Reliable 6T CMOS SRAM Cell with Minimum Size Transistors" Torrens,G. J.; Segura, J. Senior Member, IEEE; Bota, S. A, Senior Member, IEEE; Malagón,D; Jaume Verd,Senior Member, IEEE. IEEE Transactions on Emerging Topics in Computing (Volume: PP, Issue: 99), 14 July 2017.

Abstract: As minimum area SRAM bit-cells are obtained when using cell ratio and pull-up ratio of 1, we analyze the possibility of decreasing the cell ratio from the conventional values comprised between 1.5–2.5 to 1. The impact of this option on area, power, performance and stability is analyzed showing that the most affected parameter is read stability, although this impact can be overcome using some of the read assist circuits proposed in the literature. The main benefits are layout regularity enhancement, with its consequent higher tolerance to variability, cell area reduction by 25% (with respect to a cell having a cell ratio of 2), leakage current improvement by a 35 %, as well as energy dissipation reduction and a soft error rate per bit improvement of around 30 %.

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