Universitat
de les Illes Balears

DOCTORAL THESIS

2018

DEVELOPMENTS FOR AN EMBEDDED AND RELIABLE FLOATING GATE DOSIMETER

Joan Cesari Bohigas

Universitat de les Illes Balears

DOCTORAL THESIS

2018

Doctoral Programme of Electronic Engineering

DEVELOPMENTS FOR AN EMBEDDED AND RELIABLE FLOATING GATE DOSIMETER

Joan Cesari Bohigas

Thesis Supervisor: Dr. Miquel Jesús Roca Adrover

Thesis tutor: Dr. Jaume Agapit Segura Fuster

Doctor by the Universitat de les Illes Balears

Universitat de les Illes Balears

Dr Miquel Jesús Roca Adrover, of Universitat de les Illes Balears

I DECLARE:

That the thesis entitled "*Developments for an embedded and reliable floating gate dosimeter",* presented by Joan Cesari Bohigas to obtain a doctoral degree, has been completed under my supervision and meets the requirements to opt for an International Doctorate.

For all intents and purposes, I hereby sign this document.

Signature

Palma de Mallorca, October 15th, 2018

Acknowledgments

This thesis is the result of six years of research at Integrated Circuits Malaga SL, at the Universitat de les Illes Balears and at CERN, which for me has been an enriching and challenging experience.

I am deeply grateful to Alvaro Pineda, CEO at Integrated Circuits Malaga SL, to give me the opportunity to participate and to work in this research field from the very beginning of the project, and to give me as well all the support needed and comprehension related to all the problems related or not to the work.

I want to express a deep and sincere gratitude to my CERN supervisor, Salvatore Danzeca. He has been more than a mentor, a real friend. He supported me in all the activities and, with his wide knowledge, followed my work constantly. He gave me the opportunity to be autonomous, responsible and to grow up as a better engineer. I am thankful to him also for his big humanity and comprehension of all the problems related or not to the work.

I would like to express my sincere gratitude to my Professors in Mallorca, Miquel Roca, Jaume Segura and Eugeni García. I felt always supported by them and my research has always been encouraged. Their advices and support have always been important to me. Their guidance helped me in all the time I spent doing this work.

I want to thank all my colleagues, Angel, Guillermo, Tomeu, Angela, Louisa, Riccardo, Rudy, Thomas, Gabriele, Chiara, Raffaello, Gilles, Paul, Georgios and Matteo. They create a very nice working environment and I love to work with them.

I want to thank my closest friends, without them, my life in Mallorca and in Geneva would not be the same. Joan, Jose, Tuni, Jaume, Maria, Toni, Marta, Llucia, Yann, Delphine, Fanny, Andrea, Carlo, Isidre, Marco, Dani, Gorka and many others, the time spent with them is invaluable. They supported me in all the moments of the day. They make me a better person and I am grateful to have met them.

Finally, I would like to thanks my girlfriend Cristina, my brother Albert and his partner Ari, my parents Mercè and Eduard, my aunts Maria Dolors and Júlia, and my cousins Margarida and Josep Oriol. They are always supporting me and encouraging me with their best wishes always pushing me to do the best.

Abstract

Electronic devices are constantly affected by radiation in natural environment at ground level and more severely in harsh radioactive environments like high altitude, space and particle accelerators. The study of radiation effects on electronic devices is complex and requires the combination of multidisciplinary knowledge from nuclear physics to high-level system design, electronics and material science.

Radiation measurements in a mixed radiation field, as the one present at CERN, is a complex task. A reliable and accurate total ionizing dose (TID) sensor is necessary to evaluate the dose deposited on the electronic equipment installed in the Large Hadron Collider (LHC). The floating gate sensor (FGDOS®), developed and manufactured by iC-Malaga, has been proven to be a good candidate for the use in the LHC radiation monitor system (RadMON). Its high sensitivity and ease of use make it a good sensor for low dose measurements.

This work describes the process followed to improve the floating gate based dosimeter, so called FGDOS®, developed by iC-Malaga. Starting from the already existing version (named TC919), and from this, trying to find out which aspects can be improved for future versions (resulting of this work, TC974). Features as the controlled discharge of the floating gate, or increasing the sensitivity or the lifetime when it is exposed to the radiation or lower the signal-to-noise (SNR) ratio at the output given by the sensor in order to improve its minimum detectable dose will be described and discussed. Other important parameters as the radiation hardness of the different structures embedded on-chip and processes as the charge injection into the floating gate or the sensitivity degradation will be also presented and discussed.

In order to investigate and to better understand all those parameters a defined methodology was followed. The study of the radiation effects in electronic components and at device level first, and second the analysis of the most sensitive zones in the FGDOS® were the starting point to design and develop simpler structures in different Test Chips (TC). The measurement and analysis of the radiation effects in those TC are the starting point of this work to finally make possible the design of a new complete FGDOS® on-chip, adding all the upgrades previously studied. From the results of those tests, the limits of our technology could be foreseen in terms of radiation hardness and reliability.

Moreover, the radiation effects described in the literature, and detected in the radiation campaings will be mitigated by using radhard by design (RHBD) techniques at layout level in order to improve the robustness of the entire new FGDOS® in the technology which is fabricated and produced.

Radiation campaigns were necessary to investigate the radiation response against different radiation environments. To do so, different radiation facilities were used. In this work the different facilities will be described. As well the aim of each test will be presented and why the use of different kind of radiation sources, e.g. 60-Co source or Mixed-Field environment will be discussed.

At system level the configuration modes chosen to configure the FGDOS® and the data post processing will be also presented and explained to better understand the working principle of the sensor when it is embedded in a real application.

After this, the final version of the FGDOS® will be described and analyzed. It will consider all the discussion on the improvements included from the tests previously carried out. In addition, some experimental results under different radiation environments will be presented.

Finally, to conclude this work a new topology of a floating gate based sensor will be described and presented. This topology permits to overcome some of the limitations of the FGDOS®, resulting from this thesis.

Resum

Els equips electrònics es veuen constantment afectats per la radiació de l'ambient, a nivell del mar i més severament en entorns radioactius a gran altitud, a l'espai o dins acceleradors de partícules. L'estudi dels efectes de la radiació a dispositius electrònics és complexa i requereix la combinació de coneixements multidisciplinars desde física nuclear a disseny de sistemes a alt nivel, electrònica i ciència de materials.

Les mesures de radiació en un camp de radiació mixt, com el present al CERN, són una tasca complexa. És necessari un sensor de dosis total ionitzant (TID) fiable i precís per avaluar la dosi dipositada en els equips electrònics instal·lats al Large Hadron Collider (LHC). El sensor de porta flotant (FGDOS®), desenvolupat i fabricat per iC-Malaga, ha demostrat ser un bon candidat per a ser usat en el sistema de monitorització de radiació (RadMON) del LHC. La seva alta sensibilitat i facilitat d'ús el converteixen en un bon sensor per a dosis baixes.

Aquest treball descriu el procés per millorar el dosímetre basat en porta flotant, anomenat FGDOS®, desenvolupat per iC-Malaga. Partint de la versió ja existent (anomenada TC919), i a partir d'aqui, tractant d'esbrinar quins aspectes es poden millorar per a la futura versió (com a resultat d'aquesta feina, TC974). Funcions com la descàrrega controlada de la porta flotant, o augmentar la sensibilitat, o el temps de vida quan s'exposa a la radiació, o disminuir la relació senyal / soroll (SNR) a la sortida que el sensor dóna per millorar la mínima dosis detectable es descriurán i discutirán. Altres paràmetres importants com la resistència a la radiació de les diferents estructures integrades en el xip i processos com la injecció de càrrega a la porta flotant o la degradació de la sensibilitat també seran presentats i discutits.

Per tal d'investigar i comprendre millor tots aquests paràmetres, es va seguir una metodologia definida. L'estudi dels efectes de la radiació en els components electrònics a nivell de dispositiu primer, i segon l'anàlisi dels punts més sensibles al FGDOS® van ser el punt de partida per dissenyar i desenvolupar estructures més senzilles en diferents xips de proves (TC). La mesura i anàlisi dels efectes de la radiació en aquests TC són el punt de partida d'aquest treball per finalment fer posible el disseny d'un nou FGDOS® complet, afegint totes les millores prèviament estudiades. A partir dels resultats d'aquestes proves, s'han pogut fixar els límits de la tecnología usada en termes de resistència a la radiació i fiabilitat.

A més, els efectes de la radiació descrits a la literatura i apreciats durant les campanyes de radiació es mitigarán mitjançant tècniques de disseny (RHBD) per tal de millorar la robustesa a la radiació del nou FGDOS®.

Les campanyes de radiació van ser necessàries per investigar la resposta a diferents entorns de radiació. Per fer-ho, es van utilitzar diferents instal·lacions de radiació. En aquest treball es descriuran les diferents instal·lacions. Així mateix, es presentarà l'objectiu de cada prova i s'explicarà el perquè va ser necessari l'ús de diferents tipus de fonts de radiació, com per exemple la font de Co-60 o entorn mixt the radiació.

A nivell de sistema, els modes de configuració escollits per configurar el FGDOS® i el processament de les dades del sensor també es presentaran i explicaran per comprendre millor el principi de funcionament del sensor quan s'inclou en una aplicació real.

Després d'això, es descriurà i comentarà la versió final del FGDOS® on s'inclourà tota la discussió sobre les millores incloses en les proves realitzades anteriorment. A més, es presentaran alguns resultats experimentals en diferents entorns de radiació.

Finalment, per concloure aquest treball, es descriurà i presentarà una nova topologia de sensor basat en porta flotant. Aquesta topologia permet millorar algunes de les limitacions del FGDOS®, resultant d'aquesta tesi.

Resumen

Los equipos electrónicos se ven constantemente afectados por la radiación del ambiente, a nivel del mar y más severamente en entornos radiactivos a gran altitud, en el espacio o en aceleradores de partículas. El estudio de los efectos de la radiación en dispositivos electrónicos es compleja y requiere la combinación de conocimientos multidisciplinares desde física nuclear a diseño de sistemas a alto nivel, electrónica y ciencia de materiales.

Las medidas de radiación en un campo de radiación mixto, como el presente en el CERN, son una tarea compleja. Es necesario un sensor de dosis total ionizante (TID) fiable y preciso para evaluar la dosis depositada en los equipos electrónicos instalados en el Large Hadron Collider (LHC). El sensor de puerta flotante (FGDOS®), desarrollado y fabricado por iC-Málaga, ha demostrado ser un buen candidato para ser usado en el sistema de monitorización de radiación (RadMON) del LHC. Su alta sensibilidad y facilidad de uso lo convierten en un buen sensor para dosis bajas.

Este trabajo describe el proceso para mejorar el dosímetro basado en puerta flotante, llamado FGDOS®, desarrollado por iC-Málaga. Partiendo de la versión ya existente (llamada TC919), y a partir de aquí, tratando de averiguar qué aspectos se pueden mejorar para la futura versión (como resultado de este trabajo, TC974). Funciones como la descarga controlada de la puerta flotante, o aumentar la sensibilidad, o el tiempo de vida cuando se expone a la radiación, o disminuir la relación señal / ruido (SNR) a la salida que el sensor da para mejorar la mínima dosis detectable se describirán y discutirán. Otros parámetros importantes como la resistencia a la radiación de las diferentes estructuras integradas en el chip y procesos como la inyección de carga en la puerta flotante o la degradación de la sensibilidad también serán presentados y discutidos.

Con el fin de investigar y comprender mejor todos estos parámetros, se siguió una metodología definida. El estudio de los efectos de la radiación en los componentes electrónicos a nivel de dispositivo primero, y segundo el análisis de los puntos más sensibles del FGDOS® fueron el punto de partida para diseñar y desarrollar estructuras más sencillas en diferentes chips de pruebas (TC). La medida y análisis de los efectos de la radiación en estos TC son el punto de partida de éste trabajo para finalmente hace posible el diseño de un nuevo FGDOS® completo,

añadiendo todas las mejoras previamente estudiadas. A partir de los resultados de estas pruebas, se han podido fijar los límites de la tecnología usada en términos de resistencia a la radiación y fiabilidad.

Además, los efectos de la radiación descritos en la literatura y apreciados durante las campañas de radiación se mitigan mediante técnicas de diseño (RHBD) para mejorar la robustez a la radiación del nuevo FGDOS®.

Las campañas de radiación fueron necesarias para investigar la respuesta a diferentes entornos de radiación. Para ello, se utilizaron diferentes instalaciones de radiación. En este trabajo se describirán las diferentes instalaciones. Asimismo, se presentará el objetivo de cada prueba y se explicará el porqué fue necesario el uso de diferentes tipos de fuentes de radiación, como por ejemplo la fuente de Co-60 o entorno mixto the radiación.

A nivel de sistema, los modos de configuración elegidos para configurar FGDOS® y el procesamiento de los datos del sensor también se presentarán y explicarán para comprender mejor el principio de funcionamiento del sensor cuando se incluye en una aplicación real.

Después de esto, se describirá y comentará la versión final del FGDOS® donde se incluirá toda la discusión sobre las mejoras incluidas en las pruebas realizadas anteriormente. Además, se presentarán algunos resultados experimentales en diferentes entornos de radiación.

Finalmente, para concluir este trabajo, se describirá y presentará una nueva topología de sensor basado en puerta flotante. Esta topología permite mejorar algunas de las limitaciones del FGDOS®, resultando de esta tesis.

List of acronyms and abbreviations

ALICE	A Large Ion Collider Experiment
ATLAS	A Torodial LHC Apparatus
CERN	European Organization for Nuclear Research
CMOS	Complementary Metal Oxide Semiconductor
CMS	Compact Muon Solenoid
DD	Displacement Damage
DUT	Device Under Test
FGDOS®	Floating Gate Dosimeter
FGTIA	Floating Gate TransImpedance Amplifier
FPGA	Field-programmable gate array
HEH	High Energy Hadrons
HI	Heavy Ion
LET	Linear Energy Transfer
LHC	Large Hadron Collider
LHCb	LHC-beauty
MDD	Minimum Detectable Dose
NIEL	Non Ionzing Energy Loss
PS	Proton Synchrotron
PSB	Proton Synchrotron Booster
RadMON	Radiation Monitor System
RHBD	Radhard by Design
SEB	Single Event Burnout
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt

SEGR	Single Event Gate Rupture
SEL	Single Event Latchup
SET	Single Event Transient
SEU	Single Event Upset
SNR	Signal to noise ratio
SPS	Super Proton Synchrotron
TID	Total Ionizing Dose
TidMON	Total Ionizing Dose Monitor
TMR	Triple Modular Redundancy
UIB	Universitat de les Illes Balears

List of Publications

The work carried out during this thesis has led to several international conference paper presentations, both oral and poster and IEEE Transactions on Nuclear Science (TNS) journal articles. The list of articles is listed below.

Journals:

- S. Danzeca, J. Cesari, M. Brugger, L. Dessau, A. Masi, A. Pineda and G. Spieza "Characterization and Modeling of a Floating Gate Dosimeter with Gamma and Protons at Various Energies", IEEE Transactions on Nuclear Science, vol. 61, no. 6, pp. 3451 – 3457, November 2014.

- M. Álvarez, C. Hernando, J. Cesari, A. Pineda, E. García-Moreno "Total Ionizing Dose Characterization of a Prototype Floating Gate MOSFET Dosimeter for Space Applications", IEEE Transactions on Nuclear Science, vol. 60, no. 6, pp. 4281 – 4288, December 2013.

- E. García-Moreno, E. Isern, M. Roca, R. Picos, J. Font, J. Cesari and A. Pineda "Temperature Compensated Floating Gate MOS Radiation Sensor with Current Output", IEEE Transactions on Nuclear Science, vol. 60, no. 5, pp. 4026 – 4030, September 2013.

- E. García-Moreno, E. Isern, M. Roca, R. Picos, J. Font, J. Cesari, A. Pineda "Floating Gate CMOS Dosimeter with Frequency Output", IEEE Transactions on Nuclear Science, vol. 59, no. 2, pp. 373 – 378, February 2012.

- M. Brucoli, S. Danzeca, M. Brugger, A. Masi, A. Pineda, J. Cesari, L. Dusseau and F. Wrobel "Floating Gate Dosimeter Suitability for Accelerator-Like Environments", IEEE Transactions on Nuclear Science, vol. 64, no. 8, pp. 2054 – 2060, March 2017.

International Conferences:

- J. Cesari, B. Servera-Mas, S. Danzeca, M. Roca, A. Pineda, A. Masi, M. Brucoli and E. Isern "High-Speed Floating Gate Based Dosimeter System", Proceedings at 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS). September 2018.

- J. Cesari, M. Brucoli, S. Danzeca, A. Pineda, A. Masi, M. Brugger, S. Gilardoni, E. Isern, M. Roca and E. García-Moreno "Study of Floating Gate MOS Structures to improve the noise and sensitivity as Radiation Dosimeter", Proceedings at 16th European Conference on Radiation and Its Effects on Components and Systems (RADECS). September 2017.

- J. Cesari, A. Pineda, S. Danzeca, A. Masi, M. Brugger, M. Fernandez, E. Isern, M. Roca and E. García-Moreno “Analysis of two different charge injector candidates for an on-chip Floating Gate recharging system”, 12th International Conference on Design & Technology if Integrated Systems in Nanoscale Era (DTIS). April 2017.

- J. Cesari, A. Barbancho, A. Pineda, G. Ruy, and H. Moser “Floating Gate Dosimeter Measurements at 4M Lunar Flyby Mission”, The Nuclear and Space Radiation Effects Conference (NSREC) Radiation Effects Data Workshop (REDW), Boston, July 2015.

- J. Cesari, D. Gomez, M. Roca, E. Isern, A. Pineda and E. García-Moreno “Floating Gate P-MOS Radiation Sensor Charging Cycles Characterization” The Nuclear and Space Radiation Effects Conference (NSREC) Radiation Effects Data Workshop (REDW), Paris, July 2014.

- L. Sanz-Ceballos, J. Cesari, A. Barbancho, A. Pineda, A. Ramirez-Navarro and J. Llamas-Elvira “99m-Technetium radionuclide radiation measurements using a miniaturized gamma dosimeter”, European Association of Nuclear Medicine (EANM) Conference, Molecules to Man (M2M): Radiopharmacy, November 2016.

- L. Sanz-Ceballos, J. Cesari, A. Barbancho, A. Pineda, A. Ramirez-Navarro and J. Llamas-Elvira “On-chip gamma dosimeter measures comparison between ^{99m}-Technetium and ^{60}-Co radionuclides”, European Association of Nuclear Medicine (EANM) Conference, Molecules to Man (M2M): Radiopharmacy, November 2016.

- M. Brucoli, S. Danzeca, J. Cesari, M. Brugger, A. Masi, S. Gilardoni, A. Pineda, L. Dusseau and F. Wrobel “Investigation on the Sensitivity Degradation of Dosimeters based on Floating Gate Structure”, Proceedings at 16th European Conference on Radiation and Its Effects on Components and Systems (RADECS). September 2017.

- E. Isern, M. Roca, E. García-Moreno, J.C. Font, J. Cesari and A. Pineda “Characterization of a floating-gate sensor for X-ray dose detection”, Proceedings at 14th European Conference on Radiation and Its Effects on Components and Systems (RADECS). September 2013.

- E. García-Moreno, E. Isern, M. Roca, R. Picos, J. Font, J. Cesari, A. Pineda “Improved Floating Gate MOS Radiation Sensor with Current Output”, Proceedings at 11th European Conference on Radiation and Its Effects on Components and Systems (RADECS). September 2012.

- M. Brucoli, S. Danzeca, M. Brugger, A. Masi, A. Pineda, J. Cesari and L. Dusseau “A complete qualification of floating gate dosimeter for CERN applications”, Proceedings at 15th European Conference on Radiation and Its Effects on Components and Systems (RADECS). September 2016.

- M. Brucoli, S. Danzeca, M. Brugger, A. Masi, A. Pineda, J. Cesari, L. Dusseau and F. Wrobel “Investigation on Passive and Autonomous Mode Operation of Floating Gate Dosimeters“, Proceedings at 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS). September 2018.

Contents

List of Figures

List of Tables

Chapter 1. Introduction

The Floating Gate DOSimeter (FGDOS®) is a radiation sensor designed and manufactured by iC-Malaga. The design process of this sensor has been a long and complex process. It started from the very basics on the principle of detection and up to nowadays with this work providing a complete radiation tolerant FGDOS® system on chip. After 6 years of investigation with the collaboration of the UIB, the FGDOS® has become a sensor; reliable, easy-of-use and very sensitive, as radiation detector.

The research started with the investigation of the floating gate (FG) principle to foresee if the technology could retain the charge on it and be sensitive enough to the radiation [1, 2]. After, the system topology was designed and tested under different kind of radiation sources to find out the limitation on the first version of the FGDOS® [3, 4]. All this work is out of the scope of this thesis and only provides the basis to improve the current design at this time.

The scope of this thesis starts from the first version of the FGDOS® and, from this, investigates all the weaknesses and limitations of this version to try to make a better detector in terms of radiation detection sensitivity and radiation hardness to enlarge its lifetime under harsh environments.

The agreement signed between iC-Malaga and The European Organization for Nuclear Research (CERN) in January 2016 set the contents for this work. The aim of this agreement was to investigate in more detail the FGDOS® limitations and to improve it to make a better detector to be used under the radiation environments found at CERN like the ones at the LHC and its injection lines [5, 6].

At CERN the importance of monitoring the radiation in the different areas where the particles are accelerated is crucial [7]. The four main experiments conducted at CERN, (ATLAS, ALICE, CMS and LHCb) are in charge of investigating the fundamental structure of the universe. This task is performed by using particle accelerators with very high energies and intensities. These energies and intensities make CERN accelerator's environment unique in the world. Moreover, the different

accelerators at CERN perform a large chain of rings with different characteristics and diameters (so called LHC injection lines, as PS, SPS and PSB accelerators). Smaller rings are in charge of boost the energy of the beam of particles, when it is accelerated this preaccelerated beam is injected into the next stage (larger ring) in the sequence. The last stage of this chain is the Large Hadron Collider (LHC) that can accelerate the energy of the beam up to 14 TeV.

The basic operation of the LHC at CERN is, as commented above, to accelerate the particles up to the very high energy needed to carry out the collision of the particles inside the different four experiments placed along the LHC. To make it possible the beam must be guided along the LHC's 27-kilometer ring by using superconducting dipole magnets. Those magnets need extremely high currents (up to 12 kA) when the energy of the particles increases because they are accelerated up to TeV. In addition, superconductivity is a low-temperature phenomenon, so the coils must kept be at very low temperature (about -271 ˚C). All those very special characteristics on the LHC make CERN environment unique around the world.

After explaining the basics on the technologies used at CERN to carry out the four main experiments based on high-energy physics it is easy to understand why the radiation monitoring is of main importance in the experimental zones and its injection lines found at the LHC. The radiation environments found at CERN are unique in terms of energy generated and mixed particle types but because of the different range of fluxes and dose that are possible to find in the different zones of the accelerators. If the equipment installed in those areas start to fail due to the radiation they could not work on the experiments and non-desired technical stops can happen. This is the main reason of monitoring the radiation environments and from this to make decisions in advance before failures could happen in the equipment in charge of making possible these experiments.

The FGDOS® detector proved to be a good candidate to be used at CERN after its first test at H4IRRAD experimental area in Prevessin site (North Area) in November 2014. This area received a proton beam at hundreds of GeV from the SPS and it collided with a copper target to generate a mixed field environment similar to the one found at the LHC and its injection lines. In these experiments, the results from the FGDOS® were very promising owing to its high linear response to the

radiation and its very low noise at the output permitting to reach a minimum detectable dose lower than its predecessors under the same conditions.

The applications where the FGDOS® is suitable to be used are wider than those that are found in CERN environment. It is sensitive enough to be used in space radiation monitoring [8] and medical applications as in-vivo or personal dosimetry. The FGDOS® is fabricated in standard CMOS technology, which means that there is no need to add special layers in the fabrication process of the chip. This characteristic makes it very easy and cheap to fabricate. In addition, its standard power supply voltage (+5V) and its easy configurability and readout through a standard serial interface by using a microcontroller or FPGA based application makes it very attractive from the application developer point of view.

As it is shown in ***Figure 1.*** *FGDOS® basic block diagram*, is composed by three main circuitries on-chip. First, the floating gate sensor and injection circuitries, secondly the evaluating circuitry and finally the digital circuitry.

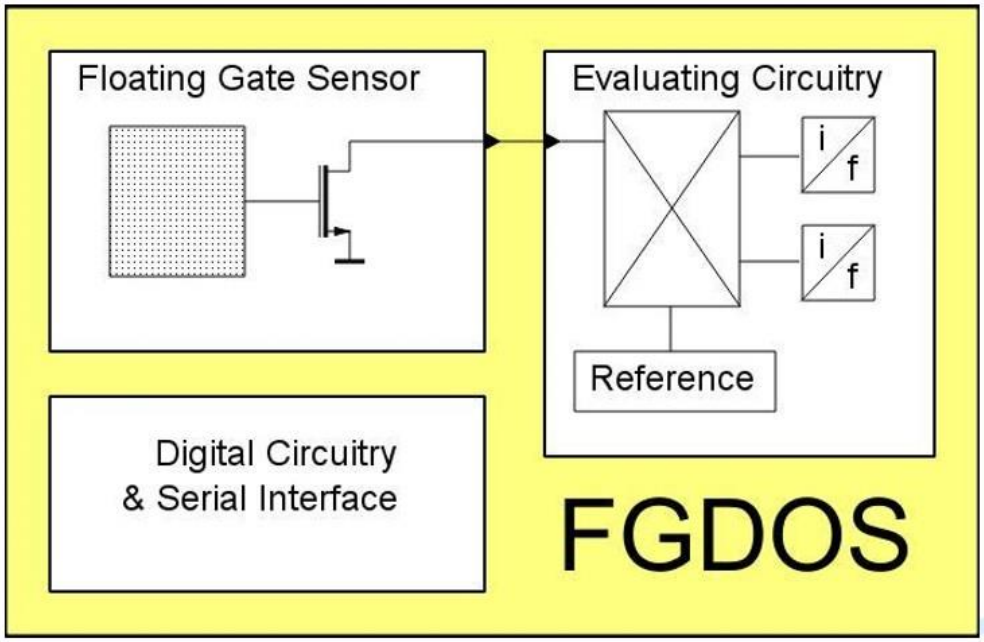

Figure 1. FGDOS® basic block diagram

The floating gate sensor and injection circuitries block is composed by the floating gate core structure, the injector and all the circuitry needed to carry out the recharge of the floating in a controlled way. The evaluating circuitry embeds all the analog circuitry needed to enhance the signal from the sensor block and to improve the

sensor response in terms of noise and temperature dependence. To conclude, the digital circuitry block is in charge of making possible the configuration of the different parameters on the analog circuitry present through a RAM memory embedded on-chip. The serial interface is used to communicate with an external user through a microcontroller or a FPGA based application; the digital word readout provided by the system can be easily processed by these applications.

The FGDOS® overcomes some of the drawbacks from similar sensors, as can be the RadFET device. RadFET usually needs an external analog circuitry to convert the analog signal to the digital world. In addition, RadFET have a non-linear response to the radiation, which makes them non-suitable for radiation monitoring without a precalibration of each sensor on the radiation conditions under they will be used. Other drawbacks will be explained in more detail in Chapter 4.

One of the main advantages of the FGDOS®, in front of other similar detectors is the possibility of monitoring the radiation when the sensor is not supplied. It means the sensor can still detect the radiation present in its area when it is in passive detection mode. It is a great advantage in battery-based systems or ultra-low power systems. Applications as personal dosimetry, satellite mission in the space or very harsh areas where the access is limited few times a year makes it very interesting to save the energy from the system whereas the monitoring is ongoing.

In this work, the first version of the FGDOS®, has been used as starting point to analyse the limitations in terms of detection and radiation endurance. From those studies simpler structures on-chip have been designed on-chip and tested under radiation trying to improve the complete system.

Features as the radiation lifetime limit, the sensitivity, the minimum detectable dose, the controlled discharge of the floating gate for debugging purposes and the sensitivity degradation due to the radiation have been studied and improved. Moreover, some other extra features have been added in the FGDOS® version resulting from this work i.e. ID number on each sensor or an embedded charge pump on-chip for making the floating recharge fully on-chip (without need of external circuitry or extra supply) or a standby mode to enter a power safe mode if needed.

To characterize all those new features and improvements, a variety of radiation environments as 60-Co source, proton beam and mixed field radiation environment

have been used. The radiation response, in terms of TID and SEU, have been checked.

The structure of this document is as follows. Next chapter (Chapter 2) gives an overview of the radiation effects on electronics. The first part of this chapter is dedicated to summarize the principal effects on electronics and concretely on the FGDOS®. The second part of the chapter is dedicated to describe each effect in most detail finishing with the most important effect in our sensor, which it is the TID effect on MOS technologies.

The old FGDOS® is described in Chapter 3, its working principle, the introduction of the old FGDOS® version, its real implementation and some issues found during its design process are presented.

Chapter 4 is the main chapter in this work. This chapter is dedicated to the new FGDOS® version, starting with the improvements and new features description and then presenting in more detail the different test chips and simple structures designed and tested. Here are also presented the different test setups and radiation facilities used, as well. Finally, the results on the different tests are presented in detail. In order to conclude, a summary of this chapter is included to explain the results and main features of the new FGDOS® design and test process.

The new proposed version of a Floating Gate based sensor is reported in Chapter 5. This sensor is based on the same principle but it is conceived for a different kind of applications with different constraints. This new architecture permits high-speed measurements, and offers more resolution in the radiation monitoring.

The last chapter, Chapter 6, is dedicated to the Conclusions and Outlooks, to resume all the process done during this work to try to improve the FGDOS®. Thus, the outlooks, open questions and future work scenarios are discussed in this chapter.

Chapter 2. Radiation Effects on Electronics

The radiation effects on electronics have been investigated since electronics exists. Electronic based systems have been used in harsh environments as space or high-energy physics facilities for more than 50 years. While upsets in the data downlink or spurious glitches in the power supply consumption may be considered minor effects, a loss of the orbit control or a loss of the control on the navigation instruments may be catastrophic. Failures in the measurement of pressure, temperature, altitude or other kind of sensor that monitor crucial parameters in spacecrafts or the high-energy physics facilities may have a huge impact in the space mission or in the high-energy physics facility owing to abrupt failures and non-desired stops.

To get an idea of the importance of the radiation effects on the electronic systems, during 25 years the National Geophysical Data Center recorded over 4500 spacecraft malfunctions or anomalies due to the space radiation environment. Another example is the forced stop in 2007 of the experiment conducted in the CNGS (CERN Neutrinos at Gran Sasso) facility at CERN, owing to a failure in the ventilation system.

This chapter will introduce briefly the most common and important mechanisms that play an important role on the radiation effects in the electronics. It will focus more in the most common radiation effects at component level and concretely in the Total Ionizing Dose (TID) effect which is the most important effect regarding the FGDOS®. This effect will be explained in more detail later in this chapter focusing in the CMOS technology that is used to fabricate the FGDOS®.

2.1. Radiation effects on electronic components

The radiation effects on electronic components can be separated in two main groups. One, with the long-term effects, where it can be found the TID and the Displacement Damage (DD) effects and the other group with the transient or single particle effects, where we can find the single event effects (SEE) producing soft or hard errors in the electronic components depending on the incident radiation and the electronic component affected.

Depending on the incident particle, one or other effect can be produced. **Figure 2** shows this dependence between the effect on electronic components and the type of particle.

The SEE and TID are effects associated with the indirect or direct ionizing radiation, whereas the displacement damage is related to the rate of energy loss due to atomic displacement when a particle crosses a material, so called Non Ionizing Energy Loss (NIEL).

The presence of all three-radiation effects inside the experimental areas at CERN and in the space environment makes necessary its explanation. Moreover, in our case, its evaluation and mitigation in the FGDOS® during the radiation campaigns and the design process is the main goal in this thesis.

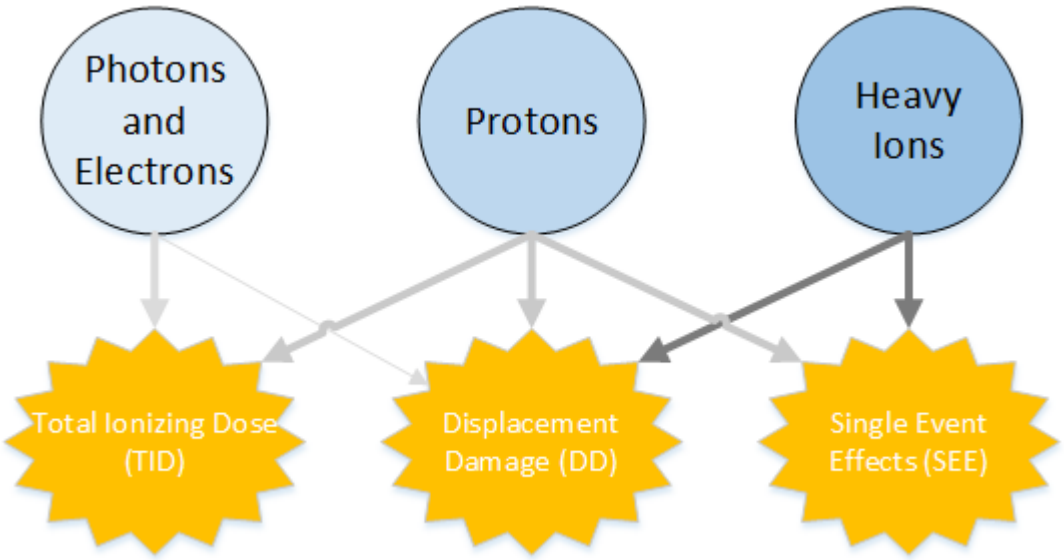

Figure 2. Radiation effects depending on the type of particle

2.2. Displacement Damage

As it is commented above one of the cumulative effects of radiation are displacement damage effects [9, 10]. These effects are based on a bulk damage mechanism. This damage occurs when radiation interacts with the material and energy is imparted to the atom. If this energy is high enough it can overcome the binding energy of the atom, in the crystal lattice of the material. Once it happens, the normal position of the atom is displaced due to Non Ionizing Energy Loss (NIEL). Therefore if the regular order of the crystalline lattice is disturbed the unique

properties in the semiconductor materials given by this order are lost. This disorder may generate changes in the operation of the affected device. Those changes can cause from a non-desired increase of the leakage currents to a loose in the amplification in MOS transistors [11, 12 and 13].

As displacement damage effects are cumulative effects, they are similar to total ionizing dose effects and produce permanent changes in the device properties. If the device is exposed to a small amount of radiation, the observable effects are small but effects build up with long term exposures.

2.3. Single Event Effects

Single event effects (SEE) are caused by direct and indirect ionizing radiation owing to a single particle. Once this particle interacts with the crossing material, it produces different kind of effects in the electronic device or component. SEE are produced mainly due to the material interaction with a heavy ion (HI). Thus, lighter particles, as for example neutrons or protons, usually do not generate charge enough to produce a SEE in a device. If generated, they are owing to indirect mechanisms. This collected charge produced by incident heavy particles along the semiconductor path lead to a logic upset or latchup in the circuit [14, 15].

The mechanism for generating SEE when a HI particle impinges a device can be explained easily in a reverse polarized pn junction. This kind of structure is particularly sensitive to SEE. When an ion strikes the structure, it generates an ionizing path along its trajectory, a funnel of charges. Afterwards two effects occur, one promptly in the high electric field regions in the depletion region where a drift or funneling collection effect is pointed out, when electrons are attracted to the pn junction generating a transient current in the junction zone. Secondly, a delayed diffusion component effect occurs in low electric field regions when carriers move due to the influence of carrier concentration gradients within the depletion region. This second effect leads to a slightly increase of the current in the junction zone but with longer recombination times.

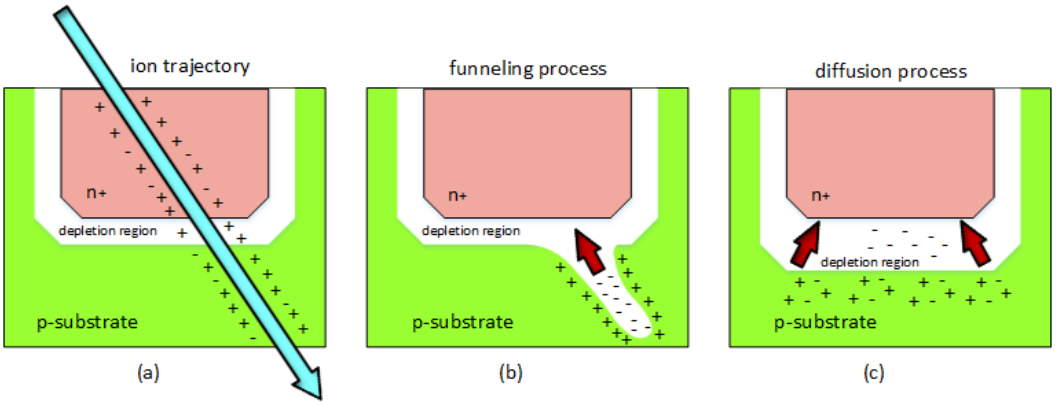

Figure 3. Ion strike charge collection process in a reversed pn junction: (a) ion strike instant, (b) prompt component; drift/funneling process and (c) delayed component; diffusion process

From the engineering point of view, it is more important to predict the rate when these events occur than how upsets occur. Since not all physics behind SEE generation is well understood nowadays, the only way to predict and characterize SEE in devices is conducting experiments under different radiation environments. Those experiments are carried out in special facilities where every particle and event in the device under test (DUT) can be monitored and controlled

The resulting data from those experiments usually are expressed as cross section versus energy for protons and cross section versus linear energy transfer (LET) for heavy ions. Both cross section and LET are very important parameters for SEE characterization of an electronic component. Cross section indicates how easy it is to have a SEE from the DUT. It means larger cross section numbers imply more susceptibility to have SEE and smaller numbers, less. Cross section is expressed as area unit, usually cm^2. On the other hand, LET indicates how a particle crossing a material losses energy as it passes through it. Higher LET expresses that the crossing particle deposits higher amount of energy in that material. In this case, LET units usually are expressed as $MeV \cdot cm^2/mg$.

These effects if triggered can be destructive and non-destructive depending on the device type, amount of injected charge, technology and localization point. Depending on those parameters, the type of SEE is different as it is presented in ***Table 1***.

Table 1. Non-destructive and destructive SEE

Acronym	Effect name	Effect result	Description
SEU	Single Event Upsets	Non-destructive	Storage element changes its state
SEFI	Single Event Functional Interrupts	Non-destructive	Temporal loss of device functionality
SET	Single Event Transients	Non-destructive	Transient failure of an internal node
SEL	Single Event Latch-up	Destructive	Current path owing to parasitic thyristor activation
SEB	Single Event Burnout	Destructive	Localized high current path in power mosfet and bipolars
SEGR	Single Event Gate Rupture	Destructive	Gate isolation destruction in power mosfet due to heavy ion
SHE	Single Event Hard Errors	Destructive	Cells unable to change state due to large energy deposition

A single event upset (SEU) usually generates a corruption of the information in a memory element and it is needed a power-on or reset to recover normal function of the device. When a single event functional interrupt (SEFI) occurs, often it is owing to a SEU in the control circuitry of the device and alike it is needed a power-on or reset to recover normal function of the device. SEFI are commonly detected in complex digital circuitries; i.e. flash memories, microcontrollers, FPGA or advanced memory devices. Instead, single event transients (SET) usually do not require a power-on or reset because they recover the normal state of the device once the transient is over. SET affect mainly circuitries that strongly depend on the bias condition i.e. comparator circuitries or as well generating time violations in memory units, by affecting their latches or flip-flops. This can led into a failure on subsequent circuitries if those are not well filtered at design level. All three, SEU, SEFI and SET are non-destructive effects and the device or system may be able to continue its normal function after a minor intervention i.e. a power-on or reset.

The destructive SEE usually appear with higher LET than non-destructive SEE. Single event latch-up (SEL) can cause a circuit lockup leading to a fatal device failure. Since fabrication technologies scale, SEL are less common due to use of lower supply voltages and new technological properties (e.g. an EPI layer reduces substrate parasitic resistance compared with traditional high resistive substrates). Moreover, as SEL depends on parasitic devices activation, it is strongly affected by temperature conditions. Usually SEL threshold decreases with higher temperatures and higher cross sections are obtained.

In the case of a single event burnout (SEB), the sensitive volume usually is the p-well that contains the NMOS devices. When it is turned on the parasitic bipolar (NPN) due to a localized current in the body of the device, it is created a current path directly between drain and source of the NMOS device. This normally affects devices with low doping concentrations and is always destructive. SEB is commonly triggered by heavy ion only, and in a minor probability owing to protons or neutrons.

A single event gate rupture (SEGR) is triggered only by a heavy ion and it is always destructive. It is triggered depending on the electric field in the gate oxide and the angle of incidence of the heavy particle. When a SEGR occurs the isolation of the gate oxide is broken and the device is permanently damaged. Usually the most affected devices are power MOSFETs due to its thicker gate oxide and higher electric fields in the gate oxide.

The rarest SEE is the single event hard error (SHE), and it happens only when rare amounts of energy are deposited in the device and thus, individual cells on it are unable to change the state. This effect can be triggered owing to micro latch-ups or micro-dose effects nearby of the affected device. Sometimes it is recoverable by making a power cycle.

2.1. Total Ionizing Dose effects on MOS

The term, total ionizing dose (TID), implies that the dose is only deposited to the electronics through ionization radiation effect and it is a long-term radiation effect. Charged particles and high-energy photons (i.e. electrons, protons or energetic heavy ions) are able to ionize when they are crossing a material generating electron-

hole pairs. This ionizing process occurs due to the interaction of the incident particle with the atoms of this material [16].

Ionization-induced damage by photons initiates when electron-hole-pair (ehp) are generated from secondary electrons emitted via photon-material interactions along the track of the incident particle. Other kind of charged particles as protons also generate ehp leading to ionization damage in the material. The amount of ehp generated along the path of the charged particles crossing the material is proportional to the energy transferred to the target material, expressed usually with the LET magnitude.

In **Figure 4**, it is shown the basic radiation-induced processes related to the generation, transport, trapping of holes and induced buildup of interface traps at the SiO_2-Si interface for the case of positive bias applied to the MOS gate. Four basic steps describe the physical processes from the initial energy deposition by ionizing radiation to the creation of ionization damage. (1) generation of ehp and partial recombination of the ehp generated, (2) transport of remaining free holes in the oxide through the SiO_2 bulk, (3) formation of trapped charge owing to hole trapping and (4) formation of interface traps onto Si bandgap .

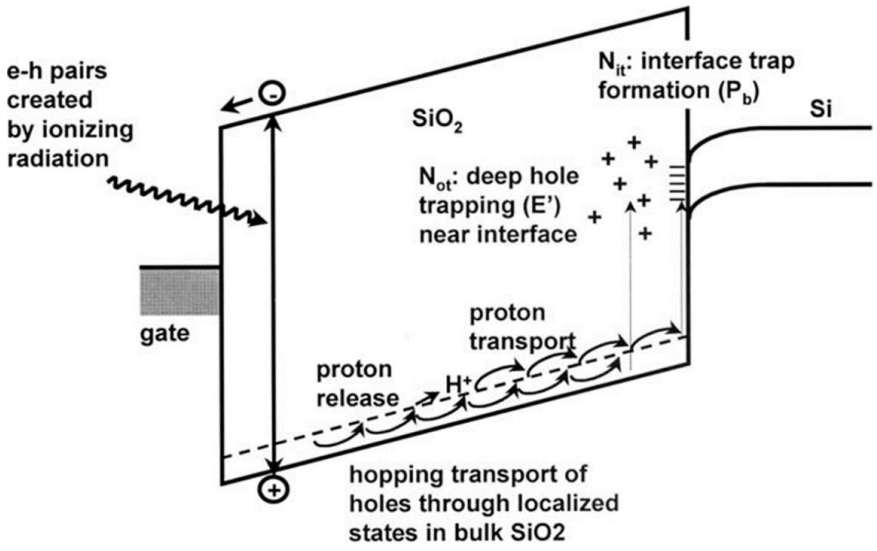

Figure 4. Energy band diagram for a biased MOS device under TID [17]

The energy deposition in the material needed to generate an ehp is 18 eV. The amount of energy deposited will strongly depend on the type of material and, the kind of energy of the incident particle. The LET magnitude provides this information. The

recombination effect in SiO_2 is a prompt process due to the mobility of the electrons in this material. The holes, in the other side, are practically immobile, depending on the field and temperature while electrons are swept out of the oxide very rapidly. Then even without bias, electrons recombination will take place within few picoseconds and just leaving few holes remaining almost in the same position where they were generated. In order to describe in more detail this process recombination models such columnar model or geminate model are usually used [18].

The holes transport in SiO_2 starts from the excess of electrons and holes which did not recombine after its generation. It is a process carried out within few picoseconds. Because of that, those electrons and holes are free to move in the SiO_2 owing to any applied electric field. As explained above, electrons are with high mobility and are swept out from the oxide to the positive electrode quite rapidly. Instead, holes are with low mobility and remaining close to the generation point. This generates the threshold voltage shift. Thus, a fraction of this holes are transported toward the negative electrode where they are collected, so called, deep holes trapping near Si-SiO_2 interface, thereby forming trapped positive charge. In addition, the formation of interface trap may be produced due to reactions between those holes and hydrogen or dopant defects.

Once ionization radiation-generated holes have had time to complete its transport through the oxide, MOS structures usually have a negative V_{th} shift and it persists for hours or even years. This shift can be expressed as:

$$Vth(t) = Vth(0) + \Delta Vth(t)$$

Where $\Delta Vth(t)$ is the variation of the V_{th} owing to the generated charge inside the oxide and $Vth(t)$ the resulting V_{th} along the time, starting from the initial V_{th} value of the MOS structure, $Vth(0)$, where ionizing radiation was not applied yet. The shift of the V_{th} produces a variation on the characteristic curve (I_{DS} vs V_{GS}) of the MOS device. This variation leads to a negative shift of the entire entire curve when ionizing radiation is applied. This behavior is shown, for an n-MOS transistor, at **Figure 5**.

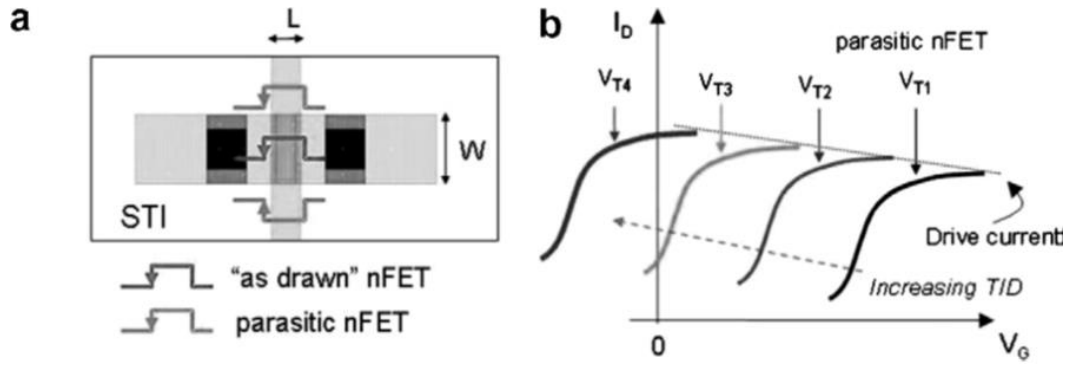

Figure 5. (a) Circuit-level model associated to a n-MOS transistor with parasitic nFETs and (b) TID effects on the threshold voltage of the n-MOS and current increase of the parasitic nFETs [19]

In addition to V_{th}, there is also another cumulating effect coming from the TID damage: the I_{DS} leakage current caused by the parasitic nFET. This effect is the dominant contributor in the n-MOS transistor when V_{GS} = 0. It is coming from the charge trapped in the isolation dielectric at the Si-SiO_2 interface. This charge creates a leakage current path between the drain and the source of the MOS transistor. The effect can be seen as an offset current in the characteristic curve of the n-MOS transistor (see **Figure 5**). Moreover, this effect is mitigated in p-MOS transistors due to its higher p-doping concentration in the p-type body [20].

The TID damage can be mitigated using protection shielding in the electronic systems. In space applications is a common strategy to try to enlarge the electronics lifetime during the mission. A common type of shielding used is the Aluminum. The Aluminum depending on its thickness stops most of the ionizing particles [21] e.g. 3.705 mm of Aluminum, lowered the TID deposited in the device up to five orders of magnitude.

TID damage is a long-term radiation effect. Usually it is measured, according the International System of Units (SI) with the Gray (Gy) magnitude and expresses the unit for the ionizing radiation dose. It is defined as the absorption of one joule of radiation energy per kilogram of matter Gy is used usually in medical/personal dosimetry. Another commonly used system of unit is the centimeter-gram-second (cgs) and its magnitude for measuring the ionizing absorbed dose is the rad. One rad is equivalent to 0.01 Gy. Rad unit in our case are always absorbed dose in silicon, rad(Si). This unit is commonly used in space. In this work, both notations will be used.

The TID is the magnitude measured by the FGDOS® and its principle of detection will be further explained in Chapters 3 and 4.

Chapter 3. Floating Gate DOSimeter (FGDOS®)

In this chapter, the basic concepts on the FGDOS® are introduced. The working principle is detailed at sensor level. Firstly explaining the physics behind the detection principle of the radiation, secondly presenting how it is used to enhance the output response of the sensor.

In addition, later in this chapter, the main configurations and working modes of the FGDOS® are presented and afterwards its limitations and drawbacks, from a practical point of view, depending on the targeted application.

3.1. Working Principle

The FGDOS®, as the name points out, is based on the floating gate (FG) detection principle. This FG node is a capacitor embedded on-chip and has one of the terminals connected to substrate and another floating. The floating terminal, when it is pre-charged, is the terminal that detects the radiation. This charge is pre-stored in the floating node via an injector and this injector is able to act ideally as a switch, keeping the floating node isolated when there is no injection process on going. The radiation detection can be monitored because this capacitor terminal is connected to a gate of an n-MOS transistor, as it is shown in **Figure 6**.

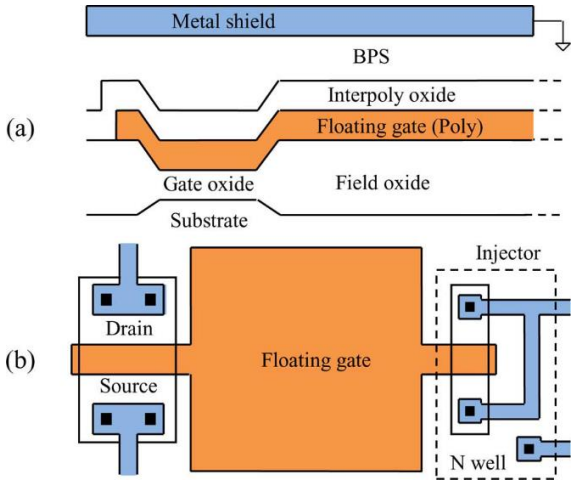

Figure 6. FG sensor core structure, (a) cross section view and, (b) top view [1]

Essentially the floating gate sensor is an n-MOS transistor with the gate connected to the floating capacitor. This floating capacitor is made with polysilicon and has a large extension over the field oxide. When charge is placed, by using the injector, on the FG, a current, I_{DS}, flows through the n-MOS transistor and is used as output of the sensor core structure [2]. This electrical schema is presented in **Figure 7**.

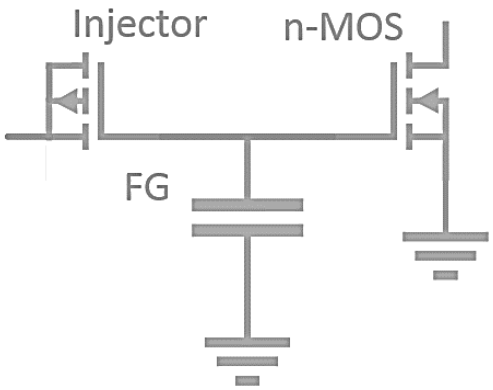

Figure 7. FG core structure electrical schematic with the FG capacitor, the p-MOS transistor as injector and the reading n-MOS transistor

To avoid external couplings or electrostatic fields, the entire area of the floating capacitor is shielded. An upper metal layer connected to ground overlaps the area of the floating capacitor, as it can be seen in ***Figure 6***.

The FG is pre-charged prior to be irradiated. This process can be achieved when is applied a sufficiently large positive voltage to the injector electrode that causes tunneling through the gate oxide of the injector. Tunneling is a physical phenomenon described in detail in [22, 23]. The injector electrode short-circuits the bulk, drain and source terminals from the p-MOS transistor used as injector. Thus, its gate is in the FG side. This required high voltage is generated off-chip and controlled on-chip by an embedded circuitry in order to monitor the process and avoid injector's gate-oxide damage. This circuitry enables and disables the recharge process in a safe way. By monitoring the I_{DS} current of the n-MOS transistor, the desired output current of the sensor core structure is set.

Depending on the high voltage value applied, the recharge process can take several minutes or less than a second. It is a very delicate process and needs special attention in this work. The recharge process is a crucial step on the FGDOS® working principle and it will be discussed in further detail in Chapter 4. Deeper analysis on the

process is done, and results regarding some experiments carried out in the injector structure are presented, to understand better its limitations and performance.

Once the floating capacitor is pre-charged (i.e. V_{GS} = 4V) the n-MOS transistor drives a constant current, I_{DS}, as initial condition. When radiation is applied, ionization radiation particles create electron-hole pairs (ehp) in the field oxide. Immediately, a major fraction of the electrons recombine but since the charge pre-stored in the floating capacitor is positive; the FG electric field sweeps remaining electrons out. This effect discharges gradually the pre-stored charge in the FG and generates a variation on the I_{DS} of the n-MOS transistor.

After or during irradiation, if the V_{FG} went below a desired threshold, the FG recharge process can be triggered again. Thus, a reset of the FG is carried out because the pre-stored charge value is initialized again.

The radiation usually crosses all the circuitry from the chip. Therefore, it means, that all the circuitry is exposed to the ionizing radiation, not only the sensitive part (the FG capacitor). This situation depending on the amount of radiation cumulated on the auxiliary circuitries on chip can generate damage and finally a failure in the chip. Moreover, if the radiation cumulated is enough the sensor core structure can be affected as well in his performance in terms of radiation detection. So, its working principle can be affected. This will be discussed in more detail in Chapter 4, when different circuitry blocks from the previous version of the FGDOS® are investigated and analyzed to foresee possible limitations in the lifetime of the detector.

If the radiation levels are low, only the FG detects the radiation, and the sensor does not have major problems in other circuitries owing to the radiation. If not, if radiation levels are high, different non-desired effects on the circuitry are pointed out. Thus, in this work will be investigated RHBD techniques to be applied at layout level. Those techniques should increase the lifetime of the new FGDOS® version. To permit to detect radiation in harsher environments for longer time different methodologies will be presented and analyzed, avoiding non-desired failures in the surrounding circuitry and avoiding as well premature degradation on the detection parameters of the sensor circuitry.

3.2. Introduction to FGDOS®

The FGDOS® is a silicon radiation sensor based on the floating gate (FG) principle. The output given by the sensor is a frequency-modulated train of pulses proportional to the charge in the floating gate. The FGDOS® embeds on-chip a very low noise signal amplification technique reducing the need of deep-gate discharge and allowing the sensor operation in a linear zone of response. Sensor linearity and resolution are this way enhanced. Temperature effects are internally compensated but if higher precision is needed, a reference output frequency is provided to permit the microcontroller to cancel any temperature offset using a predefined look-up table. Both, the reference and sensor frequencies are read directly via the serial peripheral interface (SPI), as a digital word thanks to counters on-chip. In addition, a digital thermometer is also embedded on-chip. This way, the temperature of the sensor can be monitored through the SPI with one-Celsius degree resolution. The FGDOS® block diagram is shown in **Figure 8**.

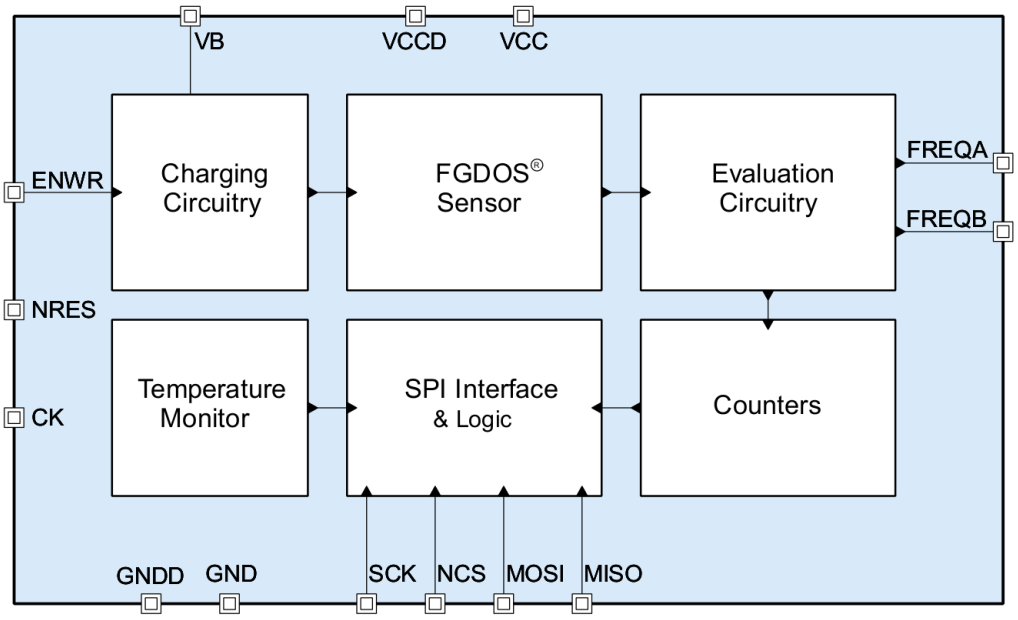

Figure 8. First version FGDOS® blocks diagram (so called TC919)

As stated in the section above, the FGDOS® principle of detection is based on a FG capacitor. Charge is pre-stored in the FG using an on-chip recharging system and is stored indefinitely, unless ionizing radiation is applied. When this occurs, the pre-stored charge at FG discharges. Due to this effect, total ionizing dose (TID) can be measured.

FGDOS® working principle is based on three basic steps, in order to keep sensor's polarization inside a linear range. An illustrative diagram of these working zones is shown in **Figure 9**:

1. Initial recharge of the FG up to a target value (Zone A). It is the first recharge of the sensor to reach the working region, where the sensor has a linear response to the ionizing radiation.

2. A discharge caused by the ionizing radiation occurs at the FG (Zone B). The discharging rate of the sensor is linear with radiation dose. Discharge is faster with higher dose rates and slower with lower dose rates.

3. A recharge is triggered when FG charge reaches the threshold value (Zone C).

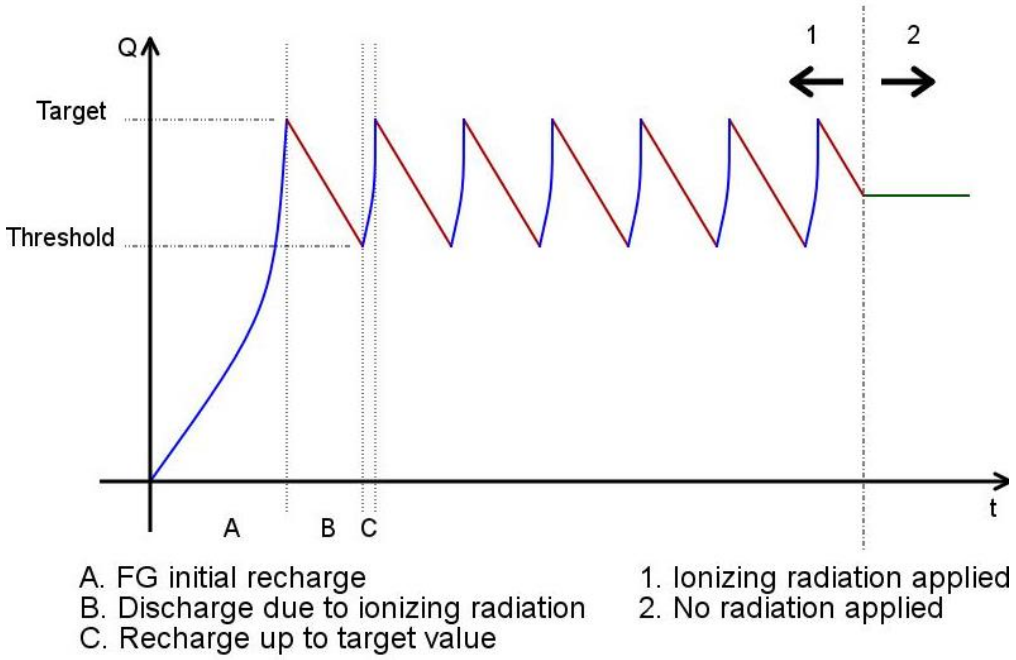

Figure 9. FGDOS® working phases; initial recharge to target, discharge due to ionizing radiation and recharge to target because threshold achieved

The total amount of radiation detected by the sensor is calculated by reading the frequency output and counting the number of recharges carried out. By following these steps and keeping the charge in the FG between target and threshold values, FGDOS® ensures working in a linear zone of detection.

The linearity of the detecting output given by the FGDOS® is of great importance. This high linearity permits to detect the amount of radiation received by the sensor

with high accuracy and makes easier the data post-processing. The linearity of the sensor comes directly from the FG core structure, and it is given by two facts; (a) the discharge of the FG when ionizing radiation is crossing it, -it is a linear process if radiation dose rate is constant-. (b) The I_{DS} response of the n-MOS when V_{GS} decreases owing to the radiation. It is well know the different working regions for MOS devices, and its intrinsic non-linear response.

Because of that, what FGDOS® does, is to use a very small range of the entire dynamic range of the n-MOS, to try to approximate this range to a linear range. **Figure 10** shows this effect. It is shown, how the entire dynamic range from the n-MOS is not linear due to saturation zones, on top and bottom of the curve. Nevertheless if only a small range of the n-MOS is used, and recharges are done to keep this range as a working point for the sensor, it enhances the linearity response of the sensor response by keeping the n-MOS working inside this linear range.

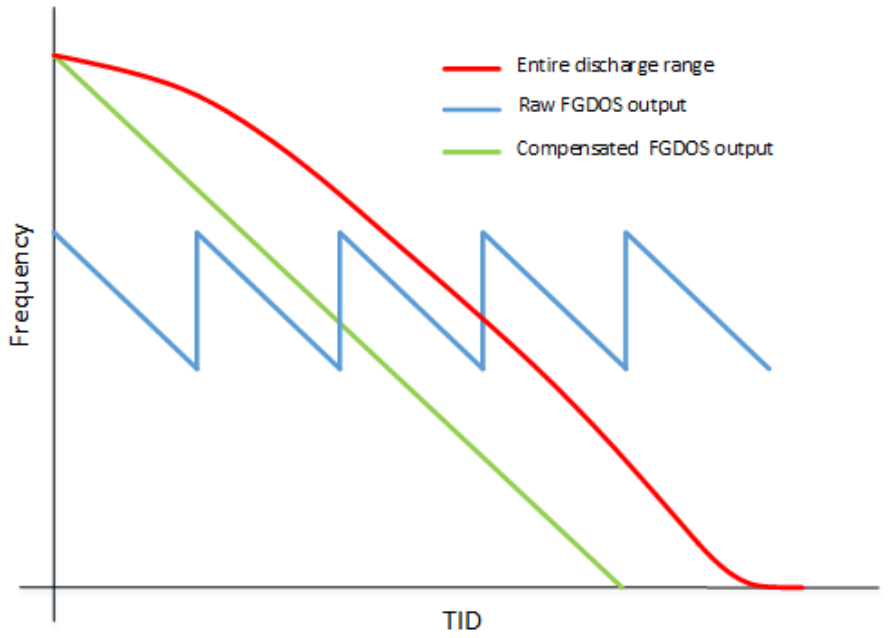

Figure 10. FGDOS® linear range (blue line), and FGDOS® compensated output (green line), in front of entire range discharge (red line). Enhancement of the output linearity is observed (data is not scaled).

Immediately from recharge process and linear zone explained above it can be noticed that FGDOS® can stay recharging more time than detecting depending on the dose rate received and the sensitivity configuration of the sensor. To overcome this, the FGDOS® has two different working configuration modes.

Two FGDOS® configuration modes are used to try to cover the maximum number of applications. One is the High Sensitivity (HS) configuration and the other the Low Sensitivity (LS) configuration. **Table 2** summarizes both configuration modes.

In HS configuration, a typical sensitivity value of 30 kHz/Gy (300 Hz/rad) is achieved. To keep the sensor detection region inside the linear zone, the output frequency ranges are set from 50 kHz (equal to the reference), as target value, and to 30 kHz, as threshold value, to trigger a recharge when is reached. This configuration increases the area of the reading n-MOS ten times with respect to LS configuration and enables the DC compensation of the output. Thus, the output DC current is partially compensated using the current generated from the reference. Hence, 90% of the current generated by the reference output before the current-to-frequency converter is taken and subtracted in the sensor output before the current-to-frequency converter, as well. By doing this, the 90% of the DC current is not present and it enhances the performance of the sensor output.

Table 2. FGDOS® configuration modes

Configuration	Sensitivity [kHz / Gy]	Detection range [Gy / recharge cycle]	Description
HS	30	0.67	DC compensation and reading n-MOS transistor x10 enabled
LS	5	4	DC compensation and reading n-MOS transistor x10 disabled

Instead in LS configuration, a typical sensitivity of 5 kHz/Gy (50 Hz/rad) is achieved and its ranges are between 130 kHz (similar to the reference), as target value, and 110 kHz, as threshold value, to trigger a recharge in order to keep the sensor working inside the linear range. Both the reading n-MOS ten times and the DC compensation are disabled when this configuration mode is used.

FGDOS® is able to detect the radiation even when it is not supplied. The FG principle still detecting radiation if it was previously charged. This working mode of the FGDOS® is very useful for ultra-low power applications, where the power consumption is critical. It must be pointed out that by using this mode, when the sensor is not supplied, recharges cannot be carried out. Hence, either it is only useful

for detecting low doses or if power supply can be switched on time-to-time and the sensor can be read out before its output is below the linear range threshold and if needed trigger a recharge.

3.2.1. Implementation and practical issues

The FGDOS® implementation is done using a standard CMOS technology with high voltage (HV) options. This technology permitted to develop the FG principle. First, retaining the pre-stored charge in the FG node, secondly having sensitivity enough to ionizing radiation to develop a good radiation sensor in terms of linearity, sensitivity and minimum detectable dose.

The FGDOS® chip area is 2 mm x 1.5 mm and the FG area is 200 µm x 100 µm. Moreover, a 60 % of the area is dedicated to the digital circuitry and a 40 % to the analog circuitry and pads. The commercial version of the FGDOS® is distributed in a QFN 32-pin 5 mm x 5 mm, where two sensors dices are embedded symmetrically on it (see **Figure 11**). This approach allows having two sensors in one package for redundancy purpose.

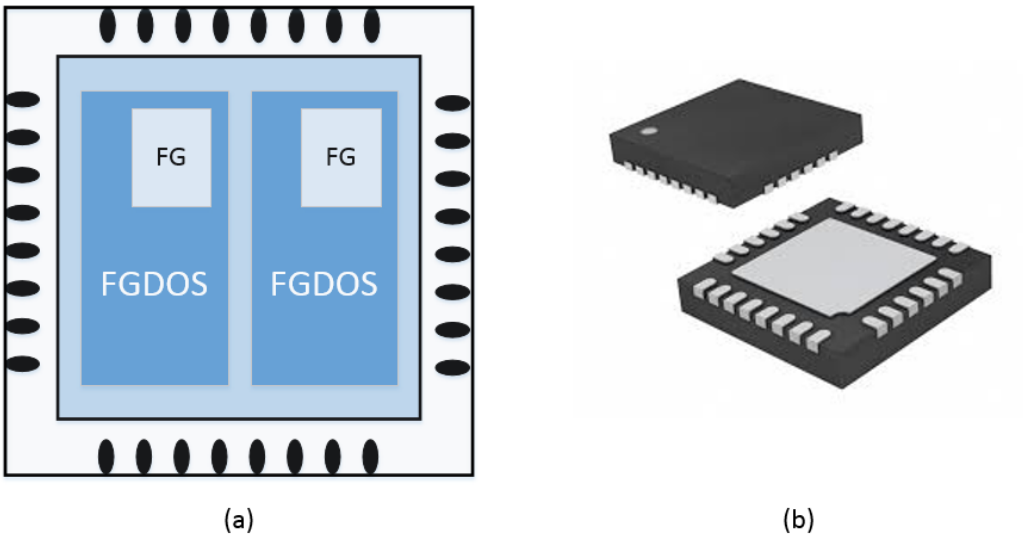

Figure 11. (a), QFN 32-pin 5 mm x 5 mm package layout top view and (b), 3D top and bottom views

The layout methodologies to complete the design of the FGDOS® were standard. Only standard CMOS transistors, bipolars, diodes, resistances and capacitors devices were used. This means, that only standard rules from the fab were applied

on the physical implementation of the chip. This set the endurance to radiation or lifetime of the FGDOS® when exposed to TID; up to 250 Gy (25 krad(Si)) [3, 4]. Also the use of standard devices made that some circuitries showed low tolerance to relatively high levels of radiation (≈ 100 Gy), starting degrading its performance before the complete failure of the chip (≈ 250 Gy). Those implied, e.g. a degradation of the sensitivity owing to the current leakage increase of the reading n-MOS and auxiliary circuitries. Alternatively, an increase of the global current consumption of the chip due to leakage current increase in digital circuitries and voltage threshold shift (V_{th}) on MOS transistors used on-chip.

The sensitivity of the system as stated before (see **Table 2**) depends on the configuration mode set in the FGDOS®. In HS is typically 30 kHz/Gy and in LS, 5 kHz/Gy. These values permit to extract the minimum detectable dose once the noise of the system is known. From experiments carried out at CERN [24], the minimum detectable dose for the FGDOS® configured in the most sensitive mode, HS, is around 160 µGy (16 mrad(Si)).

The recharge of the FG as previously explained in this chapter needs from a high voltage in order to generate the tunnelling effect in the injector and to start the charge injection in the FG node. In the FGDOS®, this high voltage must be externally generated and applied in the dedicated pin of the chip. The system implementation this way is a bit more complicated due to adding other constraints on the global application by the need of this very high voltage (+18 V).

Another important working procedure to be pointed out of the FGDOS® is the new data available sampling rate. The FGDOS® permits to make the counting of the sensor and reference frequencies on-chip by using the counter embedded on-chip. This counting usually is based on a windows time for each of the values to count (the sensor and reference values). The default window used is one second (and it can be scaled down up to 125 milliseconds), this is, two seconds waiting time to get a new pair of data (using the fastest window, 250 milliseconds waiting time), plus the time of the SPI frames (few milliseconds) to readout the values. This makes the FGDOS® acquiring time very slow depending on the application constraints or sufficient if no timing constraints are required at system level to retrieve the amount of radiation detected.

For example, in high-energy physics facilities where accelerators are generating the particle beam, if the profile of the beam wants to be monitored, it is not fast enough with the current FGDOS®. Instead, if the radiation from an area wants to be monitored in a testing zone were only the TID with less resolution in time wants to be measured, the FGDOS® should be good enough. In most of the applications sampling of few seconds is more than enough for monitoring purposes.

Chapter 4. New FGDOS® version

The aim of this work is to design and test a new version of FGDOS® to validate the improvements included on it compared to the previous version. To achieve these objectives, first simpler structures to understand better the limitations of the current FGDOS® shall be tested and validated.

In this chapter, first the desired new features are explained and discussed. Later the tests setups and radiation facilities to carry out the tests are described and presented. Finally, to conclude, all the test chips (TC) designed and fabricated to make possible those improvements in the final version of FGDOS® are presented. All test results obtained from the TC measurements are included.

4.1. Improvements and new features

There are many aspects to be improved in future versions of FGDOS®. Nonetheless, three important aspects have been targeted to be upgraded in this work, whilst keeping sensor architecture. To obtain a fully reliable FGDOS® in terms of radiation tolerant circuitry, sensor radiation detection and chip electrical characteristics, many improvements would be necessary. The upgrade of the entire circuitry from previous version and the inclusion of new circuitry blocks and functionalities would make possible to achieve those goals. Apart from those three important points, other minor issues must be addressed or new functionalities added to have a reliable and functional FGDOS® version to be used in a large spectrum of applications.

The main three aspects to be upgraded are summarized as follows:

1) Starting from previous version of FGDOS® different upgrades can be explained one after the other. First, the very high voltage needed to recharge the FG through the injector, every time it discharges owing to the radiation. This very high voltage implies a limitation at system level because usually from user's side those high voltages are difficult to obtain when commonly systems are working at +5V, +3.3V or even lower voltages. To try to overcome this limitation and facilitate the inclusion of the FGDOS® in low voltage applications, a charge

pump on-chip should be embedded. This means, all extra circuitry from this block and its performance may be tested and validated in advance.

2) Another point to be improved is enlarging the endurance against TID of the whole chip. This goal would permit to improve the radiation tolerance of the chip. It means using RadHard By Design (RHBD) techniques at layout level increasing the TID tolerance of the FGDOS®. In order to do it, the study of our technology is necessary as first step (to find out TID limits depending on kind of device), and then test and validate the new device geometries needed when RHBD techniques are applied. There is expected to enlarge the lifetime of the FGDOS® up to four times (from 250 Gy to 1 kGy or beyond). By achieving this target, the sensor would be useful for harsher environments at CERN. This upgrade will suppose an increase of the area and a completely novel layout in the new FGDOS® version, compared to old one.
3) On the other hand, the sensor core structure will be object of a deep investigation to try to improve the sensitivity of the system and lower the noise. By achieving those two steps, the minimum detectable dose would be improved, which means the sensor would be able to detect radiation levels below 160 µGy [24]. For instance, an objective in this chapter would be to double the sensitivity (currently 30 kHz/Gy) and lower the minimum detectable dose of the system below 100 µGy, where the sensor would start to be a good candidate for personal dosimetry applications.

To conclude, we enumerate other desired upgrades to be implemented at new FGDOS®. It must be pointed out that the controlled discharge of the FG by the user have been since first version of FGDOS® a desired feature. By discharging in a controlled way the FG, it is possible to lower the FG charge in case of over charge or simply in order to validate the complete application system (e.g. microcontroller-based system) by emulating radiation coming onto the system. This functionality will be added in the new version after it has been found out how to discharge it via a FG capacitive coupling effect.

In addition, other minor features will be added in the new FGDOS® version. For example, an ID number to identify each sensor using fuses on-chip will be added. This number would allow the user to identify the chip with an unique number. A factory number provided by the manufacturer to track each chip from fabrication to the end application. As well, the complete new circuitry will permit a standby mode, where the

chip can enter in a very low power consumption (from active, order of mill amperes, to standby mode, order of microamperes) mode. This will allow including the new FGDOS® in very low power applications (battery-based applications) where the power consumption is of crucial importance.

Finally, also a dummy transistor similar to the one used to read the FG, and connected in parallel to that one, will be implemented. This dummy transistor will permit, if desired, to overcome sensitivity degradation of the sensor, by adding via a lookup table (in a microcontroller-based application), a desired offset in the current of the reading n-MOS to keep the sensitivity of the system to the radiation. This will be done by controlling the gate of the transistor, externally, via pin, when the mode is enabled.

All those improvements with respect to old FGDOS® are shown in **Figure 12**.

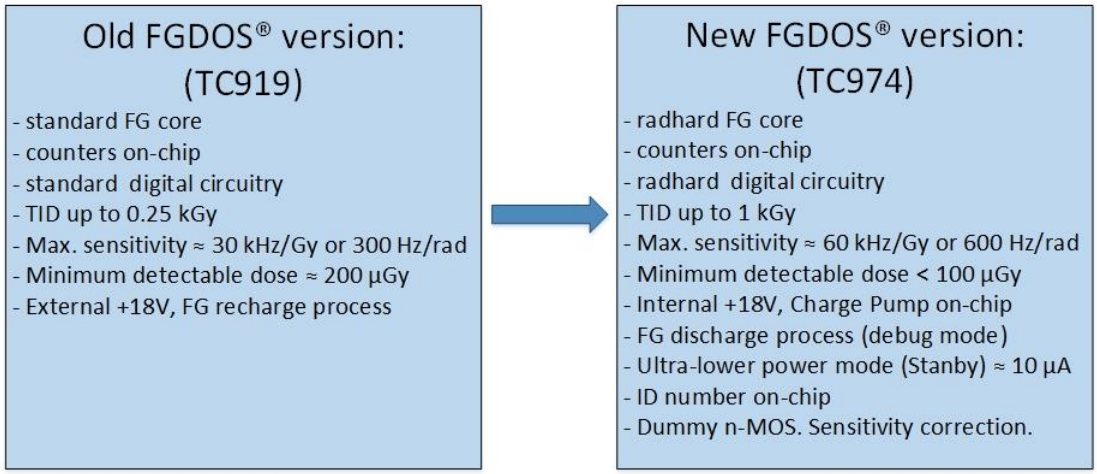

Figure 12. Expected and desired upgrades from old to new FGDOS® versions

4.2. Test chips and measurement setups

The study of the FGDOS® implied the design and measurement of different structures and circuitries embedded on-chip. Once these structures were fabricated, they were measured usually at functional level first, to verify that the expected functionality of the device or circuitry was correctly implemented. Secondly, as the aim of this thesis is the radiation detection and to improve the radiation endurance of the FGDOS®, those structures were measured under different radiation

environments. From all these results, the new FGDOS® was designed and fabricated, and characterized under radiation.

Usually the measurement setup was very simple and it will be explained in further detail for each case in next chapters. Nevertheless, for example in the case of the new FGDOS® version design, the complete sensor integrated with all the auxiliary circuitry, a more complex systems development was required i.e. TIDmon measurement system. Because of this, TIDmon will be explained in further detail in this chapter.

4.2.1. Test Chips (TC)

The investigation of radiation effects in different structures and circuitries on-chip made necessary the development of different kind of test chips (TC). A list of the structures designed, fabricated and tested is shown in **Table 3**.

Those TCs tried to analyse and investigate all aspects related to radiation, that is radiation degradation and effects on different kind of circuitries and devices, and in the sensor part, where noise and sensitivity experiments were carried out to improve both parameters.

In order to test under radiation conditions the performance of a charge pump circuitry, the TC936 was designed and fabricated. This circuitry or a very similar circuitry is the one that should be implemented on the new version of FGDOS®.

On the other hand, TC937 was developed and tested in order to evaluate the response of the input / output (I/O) digital circuitries. This TC includes standard I/O blocks and radhard I/O blocks, where radhard by design (RHBD) techniques had been used to validate those new designs compared with standard ones.

TC941 design was fabricated trying to investigate the injector performance using different injector structures and under different voltage stress conditions.

Table 3. List of TC designed and tested

TC	Radiation Test/s	Description
TC936	60-Co	Charge pump circuitry
TC937	60-Co	Digital I/O cells, standard and RHBD layouts
TC941	-	Injector structures
TC949	60-C0	MOS devices, standard and enclosed layouts
TC956	60-Co	Standard layout sensor core structures
TC971	60-Co	Voltage references with standard and RHBD layouts
TC974	60-Co and mixed field environment	New FGDOS® version
TC993	60-Co	ESD protections with standard and RHBD layouts
TC994	60-Co and mixed field environment	Enclosed layout sensor core structures

This table includes a brief description on each structure and on the radiation tests carried out. The roadmap followed during this work is presented in **Figure 13**. It can be seen, when each TC was designed (D) and tested (T).

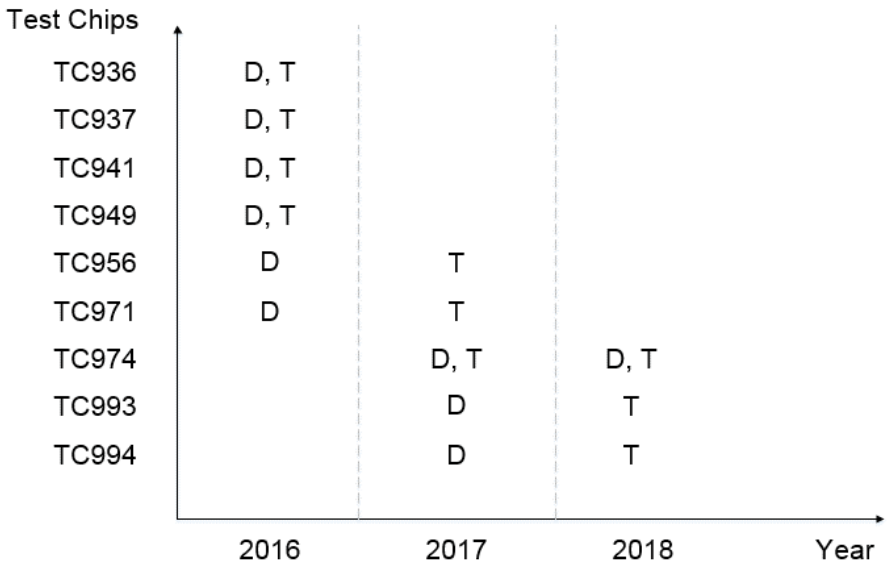

Figure 13. TCs design and test roadmap

TC949, TC956 and TC994 were designed and fabricated to analyse the response under radiation of different sensor core structures, with different geometries and areas. These structures allowed improving the sensitivity and noise of the sensor core structure. Moreover, by using RHBD techniques, the endurance against radiation was increased and non-desired second-degree effects avoided owing to radiation. TC994 will be explained in Chapter 5, as a part of the FGTIA system.

In TC971, few complex circuitries were embedded to assure the good responsiveness of the references block against radiation. That is of special importance because this block is the core of the FGDOS®, where all current and voltage references are generated for the rest of blocks. This TC included different radhard references using different topologies and the standard circuitry reference, to compare during the radiation tests.

TC993 is a TC conceived to validate new ESD protection structures, developed to avoid radiation effects in those kind of structures due to total ionizing radiation. Standard and radiation tolerant structures are embedded on it, in order to compare these behaviours.

Finally, TC974 is the new FGDOS® version. That TC includes all circuitries needed to implement a complete version of FGDOS®. It was developed in two stages, first including all the results up to the second year of this work, and the second stage, it is the final version, designed and fabricated during the third year of this work. This

final version already includes all necessary upgrades to make the FGDOS® a better sensor in terms of radiation detection and TID lifetime.

4.2.2. TIDmon

One of the measuring systems used to carry out the FGDOS® measurements was the TIDmon monitoring system [25]. The TIDmon system is a FPGA-based system developed by CERN and permits to monitor the ionizing radiation by using two different kind of sensors. One is the FGDOS® sensor and the other the RadFET sensor. Each TIDmon allows measuring four FGDOS® and two RadFETs in parallel. **Figure 14** shows the top view of the TIDmon system. It is composed by the TIDmon board and its deported module.

Figure 14. TIDmon system, composed by TIDmon board and deported module

The deported module permits to expose to the radiation only the sensors. By using it, connected to the TIDmon board through a 20-meters long cable, the monitoring system can be exposed to higher TID levels since the control circuitry embedded in the TIDmon board can be placed far from the monitoring point (the deported module), in a safe position. However, the sensors can be also placed in the TIDmon board directly when cumulated TID levels are expected to be low, and then there is no need of the deported module.

The TIDmon has a FPGA-based architecture as it is shown in **Figure 15**. Moreover, all the auxiliary circuitry needed to provide supply voltages to the sensors, the analog-to-digital converters (ADC) for RadFETs readout and transceivers to be able to communicate with a computer via a LabVIEW software are embedded on it. In addition, a PT100 is integrated in the board, to be able to readout the temperature of the system if required.

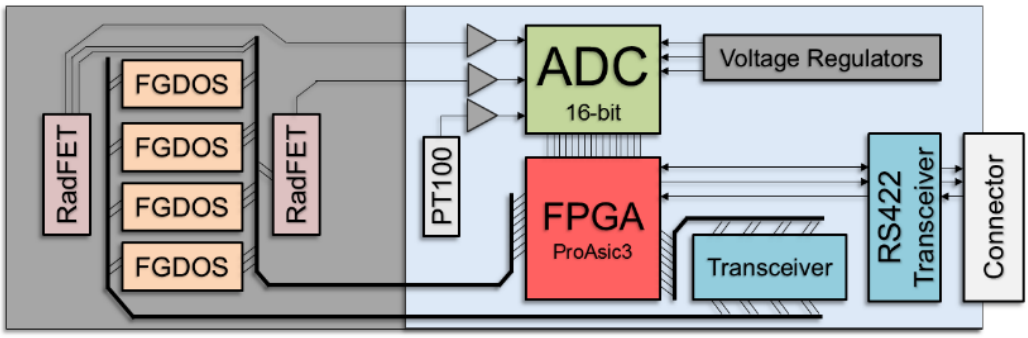

Figure 15. TIDmon system architecture [25]

In this work, the TIDmon was used only with FGDOS® sensors plugged in (RadFET measurements were conducted when needed with another platform from CERN not described here). Due to expected high TID levels usually has been used with the deported module. The TIDmon circuitry lifetime to TID is limited by the ADC up to 22 krad(Si) and new FGDOS® version is expected to last more than 250 Gy (or 25 krad(Si)).

4.3. Implementation and practical issues

The new FGDOS® version design and validation was a complex process due to many different facts. During the design, many considerations had to be taken into account to make it as much as versatile and useful in a wide range of applications.

Different versions of FGDOS® are made pin compatible, then from the user point of view, when a newer version is available it is feasible to include it in the application by adding few changes in the programming of the controller.

In addition, considerations as the area needed to embed all new features and circuitry are of main importance. New version of FGDOS® had very strong constraints in this sense in order to keep the same package used in previous versions. The area used at new FGDOS® version is the maximum available to place two dies in the package (as previous versions).

The area from the digital circuitry increased four times with respect to the standard digital placement owing to the fact of using RHBD techniques in the layout to increase the endurance to radiation. Moreover, due to area restrictions it was not possible to include triple modular redundancy (TMR) techniques in the digital circuitry. Usually

those techniques are used to avoid SEU and HI effect on-chip, or to enlarge its lifetime before a critical failure occurs.

Even if in new FGDOS® version is used the same architecture than in previous versions, many upgrades and new functionalities had been included to improve it in many aspects.

One of the drawbacks from previous FGDOS® versions was the long time needed to carry out the measurements (windows time from 250 ms to 1 second). In the new FGDOS® version in principle the time windows can be the same as previous version but also the user can set externally the time window. This functionality, plus the increase of the resolution of the target and threshold values in the newer version, makes it easier to use when shorter measuring windows are used.

Apart of time window and area upgrades, also the new FGDOS® increases the endurance to radiation, enlarging its TID lifetime above 800 Gy and increasing the sensitivity up to double with respect to the previous version. Other functionalities as the ID number (serial number) in order to track each sensor, and the standby mode to be able to approach ultra-low power applications, make the new version more attractive for a wider field of applications. All those aspects will be commented in more detail in the results section, where all the results will be discussed.

In addition, a counter to monitor the number of recharges carried out by the FGDOS® and a flag bit to know if a recharge is ongoing are included in the new FGDOS® version. Moreover, a flag bit to indicate if an overflow occurs in the sensor and references counters is implemented in the current version of the FGDOS®.

Another important upgrade with respect to previous FGDOS® versions is the option to supply the chip only with +5 V. It means the recharge process in the FG can be carried out using a high voltage generated on chip by an internal charge pump. This permits the user to need only a standard +5 V power supply and not higher voltages in the system. The charge pump circuitry embedded on chip allows generating a voltage range from +12 V to +18 V with configurable three bits (eight different steps) that permit different voltages configuration inside those ranges. New FGDOS® version also by using the charge pump, injects the generated voltage directly to the injector node, not by using a control circuitry in the middle as previous versions. This fact enhances the recharge process avoiding non-desired drops of the

recharge voltage owing to this intermediate circuitry. Thus, lower voltages generated by the charge pump are needed during the recharge process (around +16V instead of +18V in previous versions). However, there still presents the option to make the recharge externally and using control circuitry for the recharge as in previous versions of FGDOS®.

Due to degradation on the sensitivity when TID starts to increase in the FGDOS® a dummy n-MOS has been embedded in the new FGDOS® version. By using the dummy n-MOS, it will be possible to compensate the loose of sensitivity during the lifetime of the sensor. In addition, to increase the sensitivity and from results extracted during radiation campaigns, a lower reference (+2V) has been integrated in order to try to improve the sensitivity when the FGDOS® is configured in LS mode [26]. This way the user can select if lower or higher reference is going to be used.

To control the process when the charge is injected in the FG is of main relevance in the FGDOS®. Not only the recharge process is important but also the discharge of the FG in a controlled manner is of main importance. In the new FGDOS® version, the option of discharging the FG has been implemented and it is possible to be conducted by using the high voltage generated by the charge pump on-chip. The discharge in the FG is achieved by applying a high voltage (from 12V up to 30V) in a layer located all over the FG area and acting as another capacitor between the FG and the high voltage terminal. Thus, the FG couples and increases its voltage producing an effective discharge of the node through the reading n-MOS transistor to ground, by tunnelling. This upgrade leads to the option of emulate the radiation discharge effect in the sensor.

To conclude this chapter it must be mentioned that even applying RHBD techniques and making a radiation tolerant layout the shift of the V_{th} in MOS devices cannot be avoided. Due to this effect, an increase of the current consumption in the new FGDOS® version is expected. It will be commented in further detail in the results chapter. Usually up to 800 Gy (80 krad(Si)), the increase is expected to be slightly more than ten times of the current but keeping all the functionality of the chip.

4.4. Test facilities

Two radiation facilities were used in this thesis in order to find out and analyse the effects of radiation affecting the FGDOS® and both of them are presented in this section. To understand better radiation effects on FGDOS® circuitry, TID and mixed-field tests were of interest because the FGDOS® is a TID dosimeter, and it is a good candidate to be used in mixed field environments as the one present at CERN, to be more precise inside the LHC and its injection lines.

4.4.1. CC60, 60-Co Source

The CC60 room is one of the irradiation rooms in the calibration laboratory (CALLAB) at CERN [27]. CALLAB is a new calibration facility designed according to ISO 17025 requirements. It houses a 60-Co source with a nominal activity of 11.8 TBq in August 2014. Dose rates between 50 Gy/h and 0.5 Gy/h can be achieved. In **Figure 16** is shown the CC60 room, with the source and its radiation beam as well as the decay of the radiation dose rate with the distance from the source (**Figure *17***).

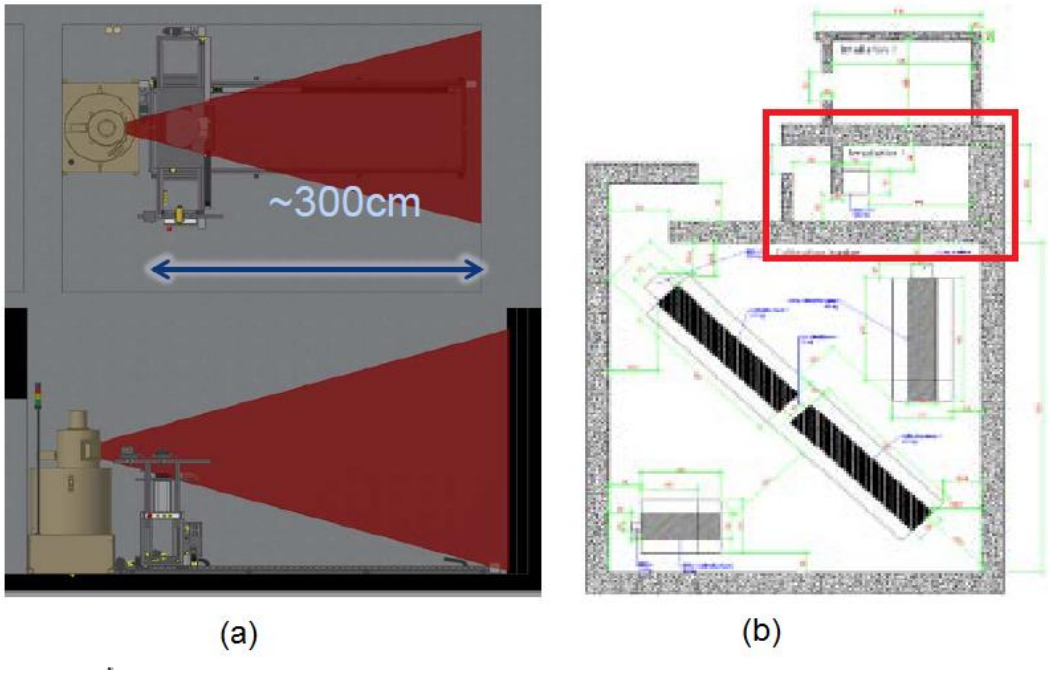

Figure 16. CALLAB facility, (a) top and profile views of CC60 room with irradiator housing and test table, (b) top view, CC60 room enclosed in red [28]

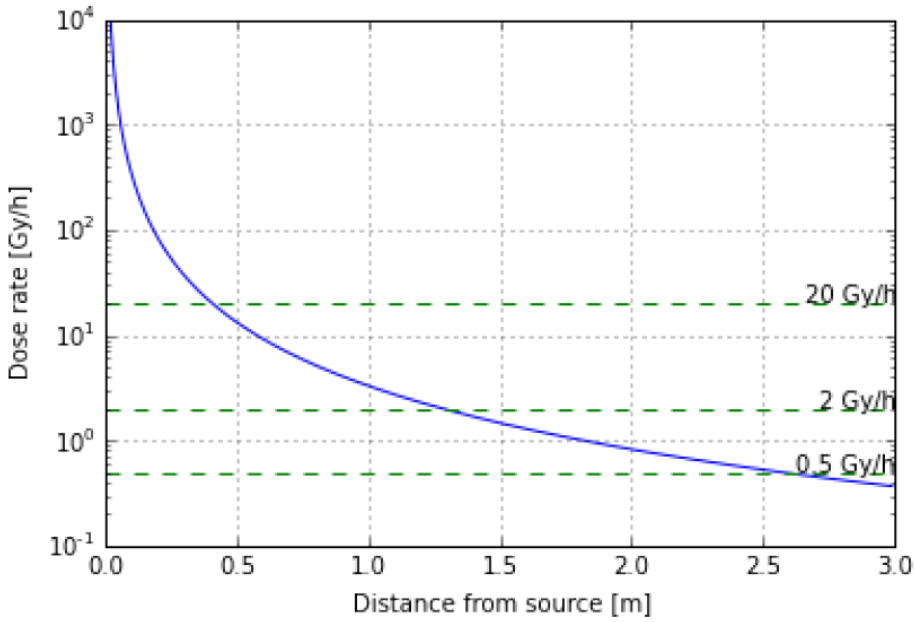

Figure 17. CALLAB facility, CC60 room, dose rate profile as function of the distance to the source [28]

To carry out our tests at CC60 room, the DUTs were placed on the test table at the distance needed to get the required dose rate for the experiment. The dose rate was calibrated always using an ionizing chamber at the exact point where the DUT was supposed to be placed during the irradiation run. Afterwards, when the position was calibrated and the DUT on place, the irradiation run started for longer or shorter time depending on the desired cumulated TID level.

Owing to the nature of the radiation provided by a 60-Co source, the CC60 room was used mainly to find out the limits of the technology used in the FGDOS® in terms of TID. In addition, the TID lifetime and detection sensitivity to TID of the new FGDOS® version were carried out using this irradiation room.

Focusing on future work to be done after the one presented in this work, CC60 room will be upgraded in 2019 with a new 60-Co source with an activity of 100 TBq. It will multiply by ten the dose rates provided by the current source. Hence, higher TID levels will be achieved faster in the DUT exposed to the new source.

4.4.2. CHARM, Mixed Field Environment

The CERN high energy accelerator mixed field (CHARM) facility is installed in the East Experimental Area in Meyrin site and a 24 GeV/c proton beam of the Proton Synchrotron (PS) accelerator serves it [27, 29].

Once the beam coming from PS impinges on the target (aluminium, copper or aluminium sieve), it generates a mixed field radiation environment (generating multitude of particles and energies) inside the test area.

CHARM inside the test area has multiple different configurations (more than 150 different) depending on the target and shielding used or test position selected. As it is shown in **Figure 18**, different shielding (concrete or iron) can be moved in whereas beam is on. Thus, some test locations can be covered by shielding blocks and receive different cocktail of particles and energies spectra depending on shielding applied and position chosen.

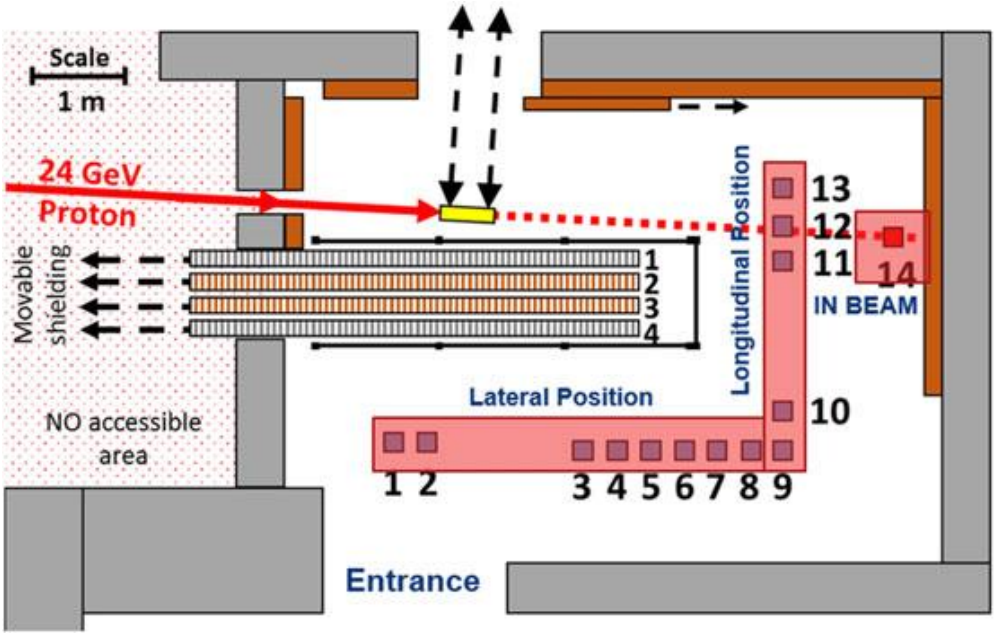

Figure 18. CHARM facility, top view detail of the target area

Typically, a year of exposure in LHC can be reproduced in less than a week exposure at CHARM, depending on selected configuration of the facility [30].

CHARM [31] is a radiation mixed field representative of CERN accelerators. It permits testing electronic equipment and allows studying the equipment radiation

sensitivity to assure its operation requirements at mid, long-term under real conditions. This allows monitoring the possible degradation of the DUT.

The cocktail of particles generated at CHARM is composed by a large spectrum of particles, from high-energy hadrons (HEH) (neutrons, protons, pions and kaons), photons, muons and electrons of energies ranging from thermal energies up to GeVs.

The beam arrives in spills of around 350 ms, every 10 s, on average and its interaction with the target creates the radiation mixed field of particles used to irradiate electronic systems and components.

Radiation dose rates at CHARM, inside the test area, can range from 0.7 mGy/h up to 45 Gy/h depending on facility configurations. In addition, HEH flux for particles with energies above 20 MeV can range from $1.6x10^{6}$ cm^{-2}/h up to $1.4x10^{11}$ cm^{-2}/h.

In this work when a test was carried out at CHARM, first of all the whole setup was tested and validated in the preparation room of CHARM, where same connectors and cable lengths can be found in the racks. Therefore, the exact setup conditions can be validated and tested in advance.

Once the setup was validated usually one week in advance, the access at the target area at CHARM (CHARM access usually on Wednesdays) was carried out when the beam was down (usually less than 24 hours). Due to the inherent radioactivity of the test area owing to the radiation mixed field of particles, the installation within this area had been made as quick as possible, avoiding high-level expositions to radiation.

Finally, when the DUT was installed in the test position, the experiment will last minimum one week until next access to CHARM was possible.

4.5. Test results

In this section, all TCs designed to upgrade FGDOS® related-circuitry are presented. In following subsections, each TC will be discussed and presented; starting from the design concept up to the tests carried out and obtained results.

Depending on the TC, the aim is different. Some of the TC are conceived to analyse the endurance to radiation of a particular device, or instead, to test radiation hardness at circuit level. In addition, other TC are designed to test the device

response under stress conditions and those tests are not related to radiation experiments.

Finally, the new FGDOS® version is also exposed and discussed. The new FGDOS® version implementation is a TC as well, but embedding a complete FG dosimeter system on-chip and adding some extra functionalities compared with previous FGDOS® versions.

TCs presented in following subsections are presented in chronological order of design. Starting from older TCs where very basic standard structures were embedded on them and/or basic circuits, to try finding out the mechanisms playing a role in the technology used when exposed to radiation environments. And ending with the most current TCs where more complex structures, including also the complete new design of the new FGDOS® version, those designs already embedding structures and/or devices thought to be used under radiation environments and including new functionalities and features.

4.5.1. TC936, charge pump

TC936 integrates a first version of charge pump circuitry. The charge pump was conceived to generate the high voltage needed to recharge the FG when it is below the threshold to keep the linear detection region. By embedding it on-chip there is no need of external high voltage to be applied from the user, because it may already be generated on-chip.

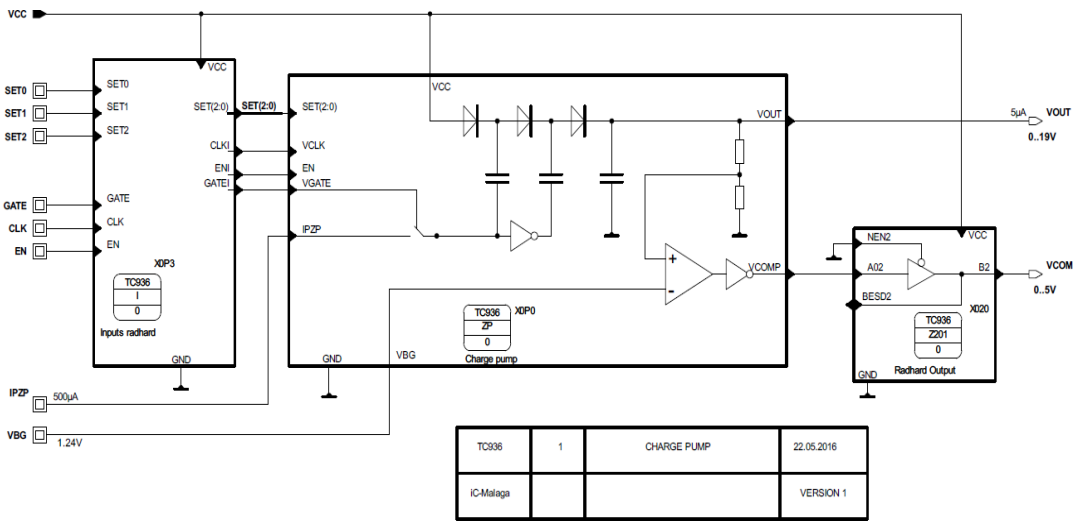

Figure 19. TC936 schematic

The development and design of TC936 was prior of this work, but reused and tested under radiation during the project. The design process of the charge pump was implemented using standard devices. Moreover, its layout implantation was following standard layout techniques too.

As it is shown in **Figure 19**, in TC936 were embedded three main block. First block, was the charge pump circuitry. Other two blocks were dedicated to digital inputs and outputs. Both of them were designed and implemented using RHBD techniques [32, 33 and 34]. This way, the effects from radiation would be appreciated only in the charge pump circuitry.

Charge pump architecture was made with four pumping stages and a configurable output voltage. Three bits were dedicated to have eight possible output voltage configurations. Thus, the charge pump could generate voltages ranging from 17 V to 19 V.

Once first prototypes were fabricated, a radiation test campaign was carried out at CC60 room at CERN and the TID lifetime of the charge pump was investigated.

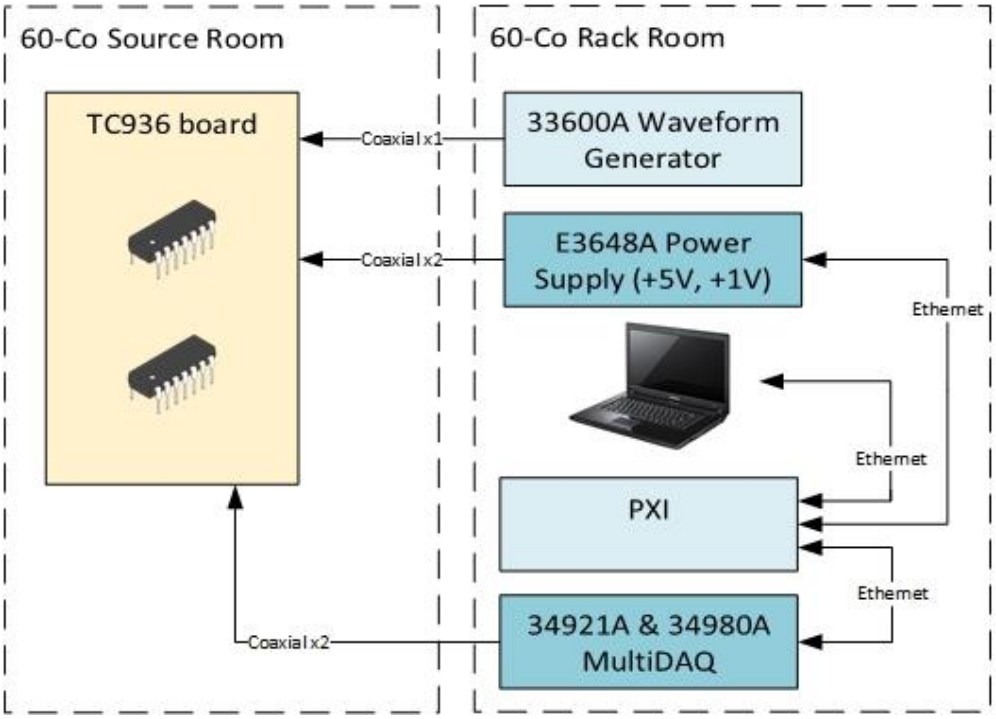

Figure 20. TC936 radiation test setup diagram

As can be seen in **Figure 20**, two samples of TC936 were tested using a waveform generator, a power supply and a MultiDAQ system. The waveform generator

provided a 10 MHz square signal as clock input of the charge pump. From the power supply two channels were used, one to generate +5.5 V (V_{CC}) and provide the power supply to both chips, and another to provide, in both chips as well, the 1 V (V_{BG}) needed as a reference voltage for the comparator. From the multiDAQ, two channels were used to measure both outputs from each charge pump.

In order to find out TID effects during the experiment, both channels of the power supply were monitored, in voltage and in current consumption. **Figure 21** presents the results of the radiation campaign (started in July 29th, 2016 and ending by August 1st, 2016) up to above 1 kGy of TID (1236 Gy) with a dose rate of 16.24 Gy/h.

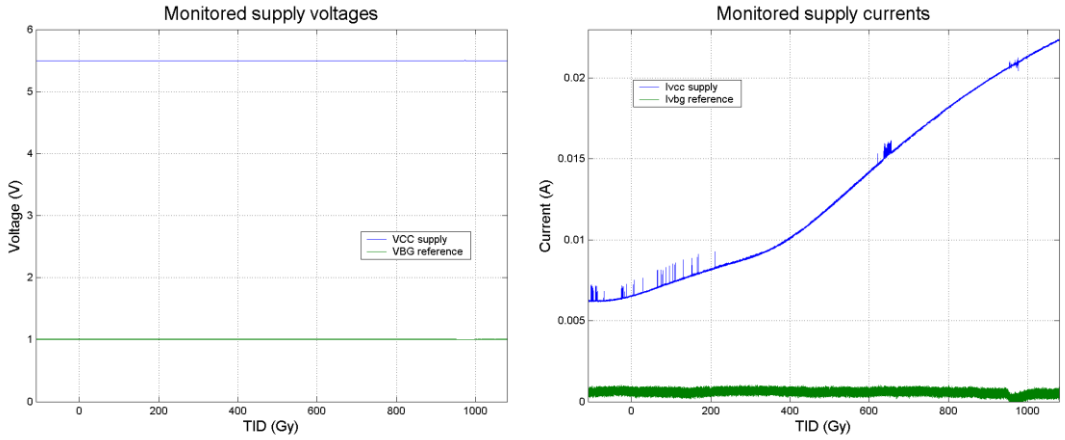

Figure 21. TC936 measurements. Left, V_{CC} (+5.5 V) and V_{BG} (+1 V) voltages and right, I_{VCC} and I_{VBG} currents, during radiation campaign at CC60 room

The voltages remained constant but the current consumption increased for the V_{CC} channel. The increase was, as expected, due to the increase of the leakage current of the system in all their devices owing to TID effect in MOS transistors and ESD protections. It is observed how the slope of the leakage current changes from 400 Gy. This may be caused due to an overlap of TID effects. First, V_{th} shift and parasitic nFET leakage currents are observed and above 400 Gy of TID, probably ESD protections leakage current overlaps those effects. Further discussion on ESD protections TID effects will be done when TC993 is presented.

On the other hand, the current consumption from the other channel (I_{VBG}) remained stable during all the irradiation time. That current, was a current from a pull-down resistor (i.e. no TID effect expected on it) and the node connected to a gate of a MOS transistor, where no TID effect was neither expected.

Both supplies were in common for both chips, so it could not be splitted the current consumption between them. Moreover, it must be mentioned that all ESD protections were standard protections with an important impact when exposed to TID, depending on the biasing conditions.

Finally, also the voltage measurements conducted with the multiDAQ on both charge pumps outputs are presented in **Figure 22**.

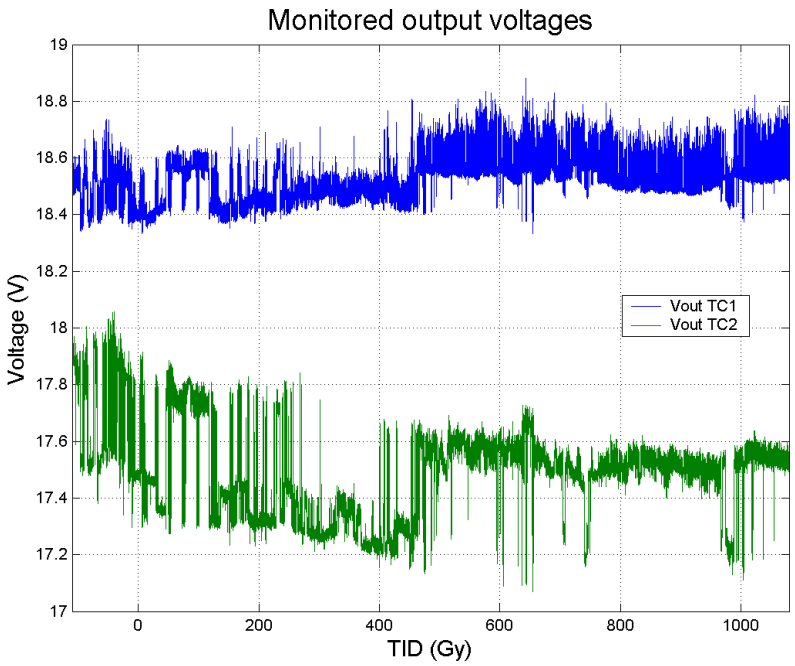

Figure 22. Charge pump outputs (V_{OUT}) from two samples when exposed to TID

The V_{OUT} configuration in both cases was set to “111”, theoretically to 19 V but as a lower reference was used (+1 V) instead of a real V_{BG}, usually with values around 1.24 V, the regulation point was a bit lower. Moreover, the output node from the charge pump is very sensitive to the load connected on it. Probably due to long cables connected from the output of the TC to the MultiDAQ, made the voltage drop tens of millivolts. In addition, oscillations on the regulation point can be observed, and it could be due to setup noise and bad contacts. It must be noticed that 10-meter long cables were used to connect between the instruments and the measuring board.

From the TID lifetime point of view, it can be pointed out that both charge pumps from two different samples were working and regulating the set point up to more than

1 kGy. Even having increased the current consumption during the radiation run, the functionality of the circuit was still unaffected and working correctly.

4.5.2. TC937, radhard I/Os

The aim of TC937 design and tests was to make a first approach to get a radiation tolerant circuit by using RHBD techniques. In TC937, digital input and output circuits were embedded. In order to validate the new RHBD circuit, standard input and output circuits were integrated in the TC as well. The schematic of the TC is shown in **Figure 23**.

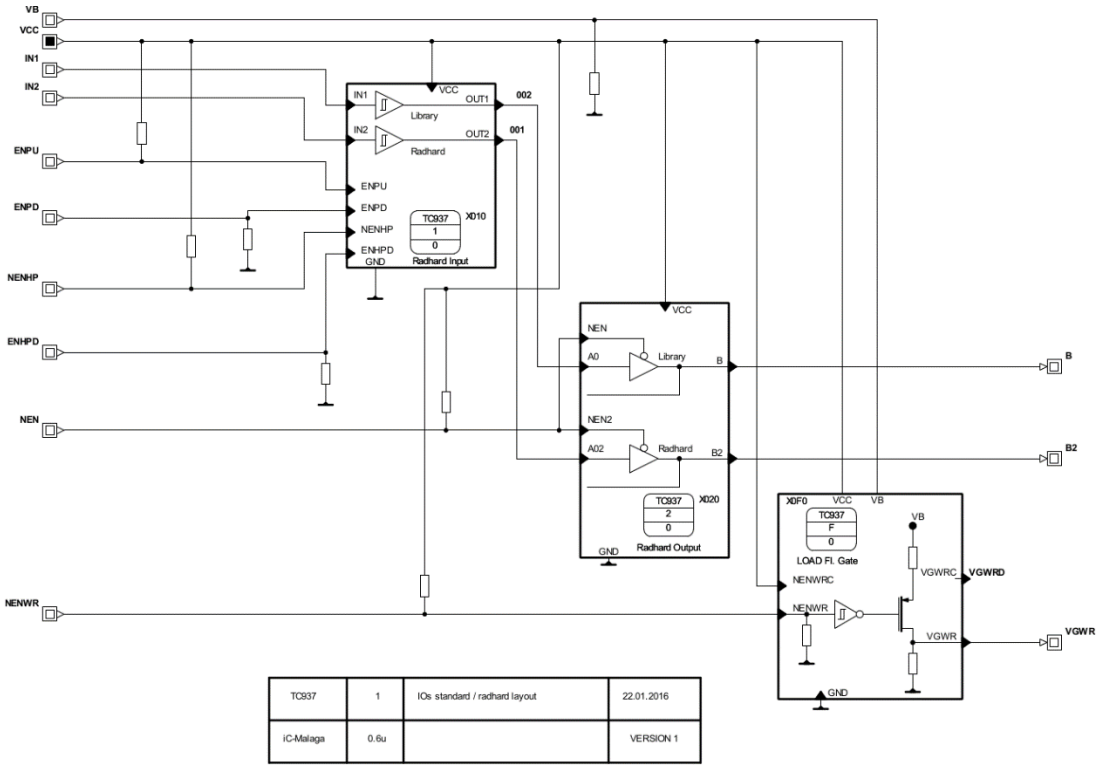

Figure 23. TC937 schematic

As can be appreciated at **Figure 23** both the digital input and output circuits with standard layout design (library) and using RHBD techniques (radhard) were integrated at TC937. In addition, the recharging circuitry of the previous version of the FGDOS® was included too. Due to number of pads restriction, all three circuits had the V_{CC} interconnected.

The development and design of TC937 was prior of this work, but reused and tested under radiation during the project. The main objective of designing this TC was

to better understand if a complete circuit design would be possible by using RHBD techniques, not only improving its radiation endurance but also keeping the circuit functionality from the standard version.

The radiation test campaign was conducted on two samples at a dose rate of 16.24 Gy/h, starting on August 1st, 2016 and ending by August 4th, 2016. The TID achieved was 1047 Gy in the CC60 room.

The test setup (it is shown in **Figure 24**) consisted in a power supply (V_{CC} = 5.5 V) for all three circuits and a 10 MHz square signal generated with a waveform generator, needed as input for the digital inputs (both, radhard and standard designs).

Under these bias conditions, both samples were exposed to TID above 1 kGy. Afterwards were measured in order to check if the output signal given by the digital output circuitry was still inside the acceptable (TTL margins) functional values.

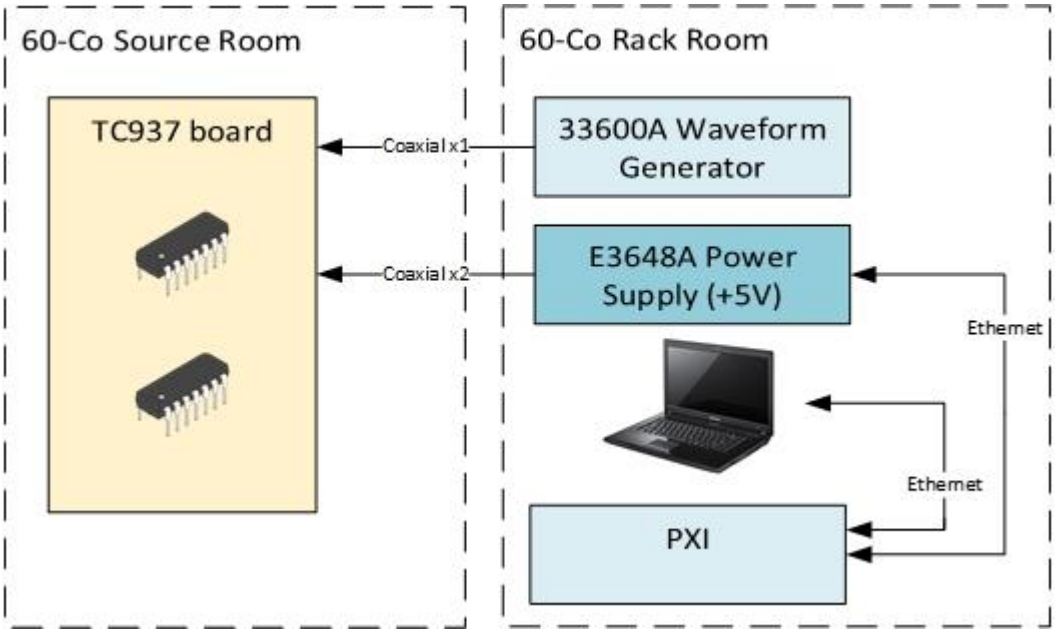

Figure 24. TC937 radiation test setup diagram

During the experiment, measurements were carried out on the supply voltage (V_{CC}) and current to monitor its evolution during the radiation run. In **Figure 25**, it is shown how the current consumption of the circuits increased from around 5 mA up to 37 mA. Nevertheless, as the V_{CC} was the same for all three circuits, it was not possible to distinguish which of the circuits was generating the increase of the current.

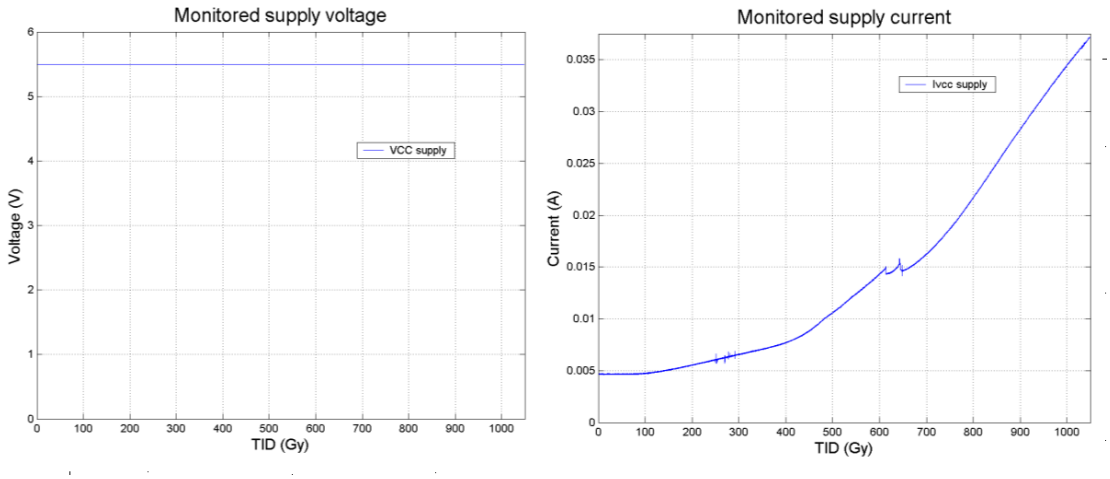

Figure 25. TC937 measurements. Left, V_{CC} (+5.5 V) voltage and right, I_{VCC} current, during radiation campaign at CC60 room

From a functional point of view the circuits, both digital outputs were measured pre and post irradiation under same bias conditions (V_{CC} = 5.5 V and V_{INPUT} 10 MHz square wave) and only the radhard one kept the functionality after the TID test and instead the standard output was not switching after the TID test.

The test on TC937 pointed out how RHBD techniques permit to enlarge the circuit lifetime when exposed to TID. The radhard circuit was performing well above 1 kGy and keeping the full functionality of the circuit (switching and working under TTL premises). Unfortunately, functional measurements were carried out only before and after the radiation campaign. Thus, measurements on the standard circuit noted that it was not working above 1 kGy, but not when exactly (which TID level) stopped working properly.

4.5.3. TC941, injectors

Results from measurements carried out on TC941 lead to an oral presentation in the 12th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS) 2017 and an IEEE publication [35].

The importance of the charge injection in the FG structure consists in the possibility to re-use the sensor several times and increase the measurement range. Indeed, by recharging the FG, the charges lost due to the ionizing radiation are restored back at the initial value and the sensor can restart to work again from the

same point [36]. During the complete lifetime of a FG sensor, the injection can be done hundreds of times before the FG CMOS circuitry starts to malfunction due to the radiation [3]. Because of that is very important to study its correct function during the whole sensor lifetime. TC941 includes two different kinds of injector (one based on a poly1 – poly2 capacitor and the other in a p-MOS capacitor), and factors as the applied voltage needed to start the injection or the breakdown voltage of both structures must be investigated.

TC941 was designed to focus on the FG recharge mechanism. As the FG is a floating node, the charge stored on it can be only injected by using a structure that keeps the FG node isolated. This structure is called the injector. An overview of the effects that play a role on the injection, and the experimental results with two different injector structures are presented.

Owing to the repeated charges of the FG capacitor through the injector, it becomes important to study the behaviour of the injector. The injector is the responsible of charging the FG capacitor every time that the radiation discharges it.

Consequently, there must be noticed that if there is any degradation in the injector oxide, because of this degradation, the charging time can change and the system can start losing charges also without radiation. The injector behaves as a resistance during the charging and like an insulating layer during the normal FG system operation.

After some injections on TC941 structures, the injector oxide degrades and the FG structure is less and less isolated. Thus, the charge stored on it is not removed only by the radiation but a current start to flow also in the injector path.

This probability of being detected on the other side of a barrier has become known as tunnelling, although there is certainly no actual digging going on it.

The application on this effect in CMOS devices has become of importance since technology is lowering its dimensions. It is known that as device technologies are improved, the device dimensions have been reduced dramatically. A few years ago, a potential of 5V was applied across 500 Å oxides in CMOS applications. Nowadays it is more common to use 3.3V drop cross 40 Å oxides. In this case, the oxide electric field has been increasing with time. Thin oxides with high electric field may no longer behave as a perfect insulator. Taking into account this factor, quantum mechanical

tunnelling of carrier through gate oxides can occur. There are three types of tunnelling: Direct tunnelling (trapezoidal barrier), Fowler-Nordheim (FN) tunnelling (triangular barrier) and Trap Assisted Tunnelling (TAT).

In the direct tunnelling, the Schrödinger equation describes that there is a finite probability that a particle can tunnel through a non-infinite potential barrier [37]. As the width of the potential barrier decreases, the probability of particles (electrons and holes) penetrating through the barrier by quantum-mechanical tunnelling rises exponentially. Because of this, the quantum-mechanical phenomenon of a trapezoidal barrier tunnelling is termed as direct tunnelling effect. It happens in very thin gate oxides and requires only a low electric field. Usually direct tunnelling current dominates when the oxide thickness is less than 40 Å. Therefore, below 30 Å the current is excessive for a reliable circuit operation.

The second tunnelling type described is the FN tunnelling [38]. This kind of tunnelling nowadays is used for any field-induced electron tunnelling through a roughly triangular barrier. The FN equations have been reformulated over the years to become the Cold Field Electron (CFE) emission theory, a standard theory by itself. This happened for two reasons [39]:

1. FN plots are the most common tool used to analyse experimental CFE data. Hence, the users of FN plots need to be able to understand standard theory and improved formulation should help.
2. The standard FN type equation was derived for free-electron metals with planar surfaces and has well-known deficiencies including limited applicability to atomically sharp emitters. Reformulation makes it easier to generalize standard theory to treat more realistic tunnelling barriers.

The high field imposed across the oxide (SiO_2 in TC941) which is necessary for tunnelling (approximately 7.5 to 10 MV/cm) results in a large density of electrons which are confined to a narrow potential well at the interface.

Finally, in TAT, last type of tunnelling, a trap-assisted leakage current effect is generated. This effect is not a primary tunnelling effect like others but it must be mentioned.

In TAT transitions inelastic phonon emission are generated. Electrons are captured from the cathode. Consequently, they relax to the trap energy level by the emission of phonons and are emitted to the anode. This effect is produced by generated defects leading to two effects. First, new defects are created in the dielectric layer, and secondly, some of the existing traps become occupied by electrons, and it leads to a shift of the threshold voltage in the device [40, 41]. Only occupied traps generate a shift of the threshold voltage, while neutral defects induce TAT and gate leakage.

During the radiation campaign both the injectors embedded in TC941 were tested. A poly1-poly2 capacitor and a p-MOS capacitor were used both as injectors. The poly1-poly2 capacitor has an area of 100 µm x 100 µm and the MOS capacitor 1 µm x 1 µm. Those structures were designed to analyse the injector charging process with them and study and compare the behaviour between them. The basic schema of both structures with the radiation sensor part can be seen in **Figure 26**.

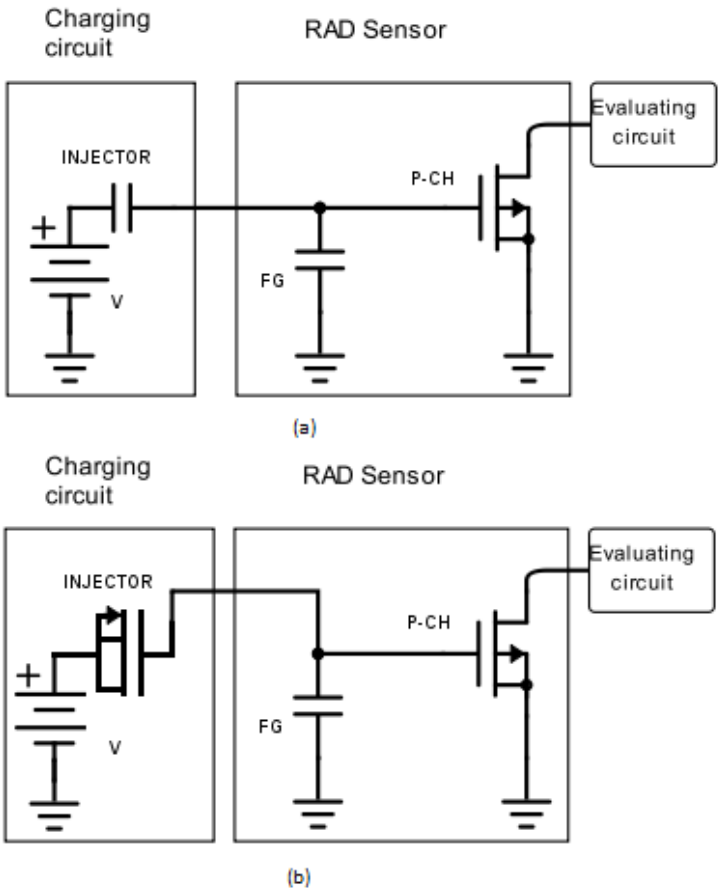

Figure 26. (a) poly1-poly2 injector and, (b) MOS injector schematics embedded with FG sensor

An important detail to keep in mind is that the poly1-poly2 injector has a bigger distance between plates of the capacitor than the MOS capacitor that only has the gate oxide thickness between plates of the capacitor.

The procedure for measuring the oxide degradation was based on **Figure 27**. Measurements were carried out by using a Keysight precision current-to-voltage analyser. A sweep on the V_S voltage was forced and, in the meantime, the currents i_s and i_d were measured for each voltage point during the sweep. The test structures designed on-chip were connected to the measurement station by using needles and contacting directly on the silicon plates structures embedded for this.

The sweep voltage applied at both structures was different owing to its different dielectric thickness. The poly1-poly2 capacitor structures sweep was from 0 V to 25 V making different repetitions. The MOS capacitors structures sweep was from 0 V to 18 V.

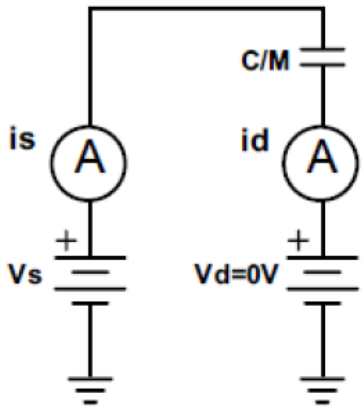

Figure 27. Injectors measurement circuital diagram

The measurements were conducted in four different injector structures of each type. **Table 4** and **Table 5** summarize the results in each structure measured.

As can be seen in **Table 4** the first two structures support up to 17 and 18 repetitions respectively whereas the last two structures only can withstand five repetitions. The voltage applied in all four measurements is higher than 22 V.

Table 4. Poly1-poly2 injector structure measurements

Measure Number	Voltage applied [V]	Repetitions [N]	Breakdown voltage [V]
1	25	18	21.5
2	24	17	24
3	24	5	24
4	22	5	22

Table 5. MOS injector structure measurements

Measure Number	Voltage applied [V]	Repetitions [N]	Breakdown voltage [V]
1	18	12	18
2	18	11	17.7
3	19	5	18.7
4	17	3	16

From **Table 5** data, it can be seen how MOS structures were able to withstand less voltage than the poly1-poly2 and the repetitions were only up to maximum of twelve. Moreover, the breakdown voltage was always higher than 16 V.

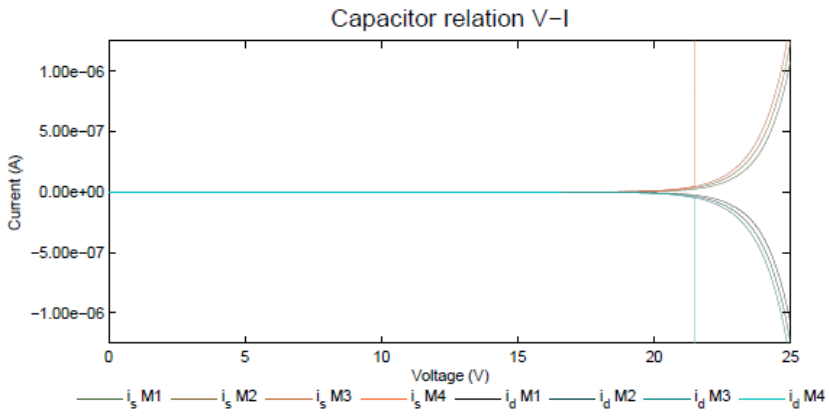

Figure 28. Poly1-poly2 capacitor after 18 repetitions breaks down around 21.5V

In addition, **Figure 28** and **Figure 29** show the behaviour of the poly1-poly2 capacitor structure number 1 when the sweep voltage goes from 0 V to 25 V. From these Figures can be appreciated how the reproducibility in terms of the current flowing through the injector structure is very high during all the 18 repetitions of the voltage sweep between terminals of the capacitor.

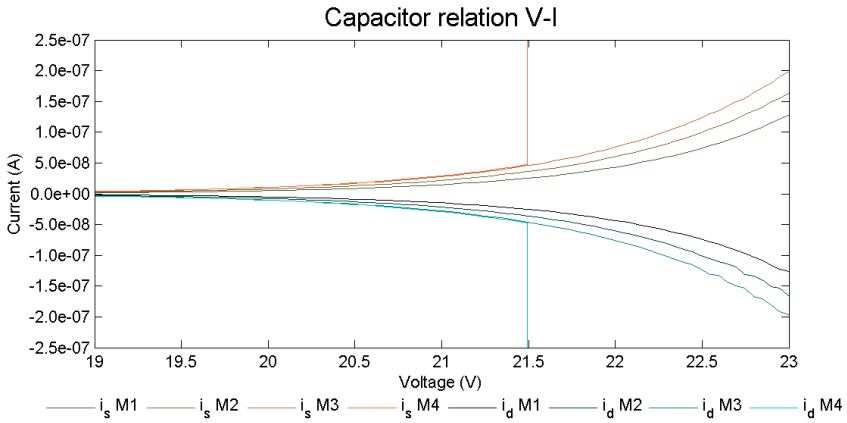

Figure 29. Detail of **Figure 28** in the breakdown zone

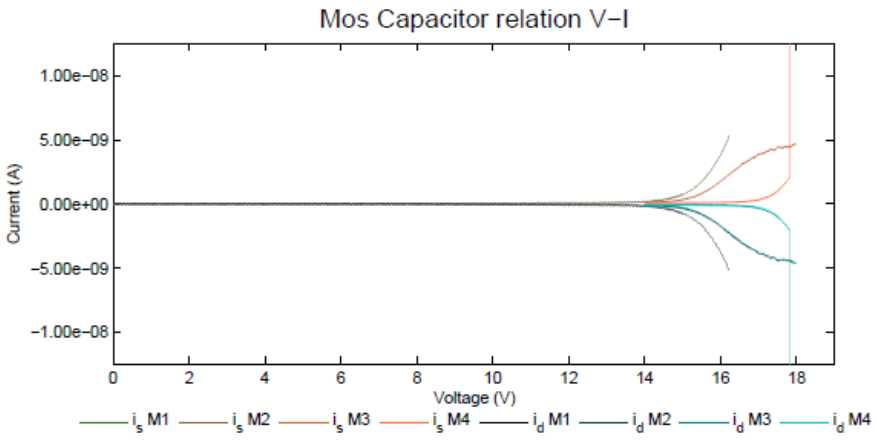

Figure 30. MOS capacitor after 11 repetitions breaks down around 17.7 V

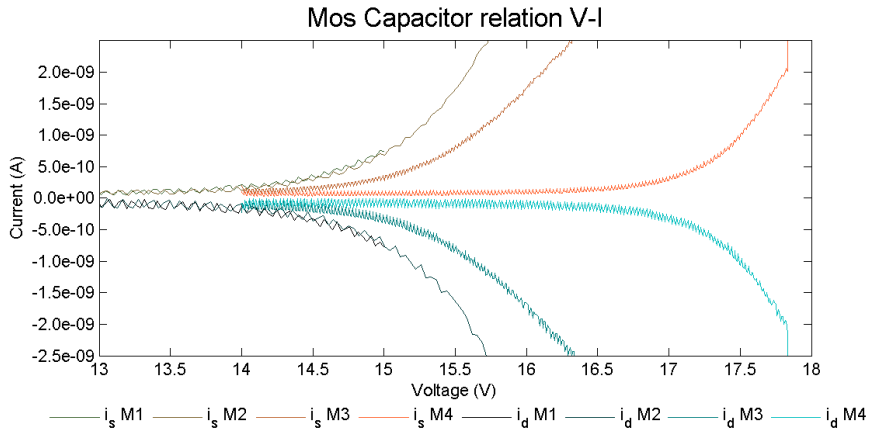

Figure 31. Detail of **Figure 30** in the breakdown zone

In **Figure 30** and **Figure 31** the behaviour of the MOS capacitor structure number 2 is shown, when the voltage sweep goes from 0 V to 18 V. In that case can be seen how the reproducibility between repetitions in terms of current flowing through the terminals of the injector is good only up to 14 V. When higher voltages are applied during the sweep, the current has different behaviours.

From the results shown before both structures show degradation in terms of current flowing after a couple of repetitions and finally break down the injector (Owing to too high voltages used, in order to see injector limitations in terms of voltage applied between terminals). As it is known from the FG dosimeter system, usually the voltage seen between terminals of the capacitor will be around 14 V. Hence, larger amount of repetitions can be achieved before observing any kind of degradation (loss of isolation in the injector when no high voltage applied for recharging purpose or

break down). When the FG starts the charge process, the voltage drop at the injector decreases because the FG voltage increases. For this reason, the voltage at the input of the injector must be raised up in order to maintain the 14 V drop at the injector. This results on a voltage of around 18 V when the FG capacitor is charged at 4 V.

From the measurements conducted on TC941, the behaviour on two different injector structures was compared. Both of the structures could be used as injector for the FG dosimeter system. Nevertheless, the best structures as injector is the MOS injector structures because when it is used in a real system as lower is the voltage needed to start the charging process the better is for the achievement of the system requirements. That is to say, the MOS structure is better because less than 14 V are needed between terminals for current to start to flow and therefore to start the charging process on the FG. In the poly1-poly2 structures, it is needed around 18 V between terminals to start the charging process. It means in terms of FG dosimeter system that the use of this kind of structure requires more than 22 V applied on the pin of the chip.

4.5.4. TC949, standard and radhard MOS devices

Test carried out on TC949 permitted to investigate TID effects on FGDOS® technology at transistor level. TC949 embeds n-MOS and p-MOS transistors as single structures with both the designs, the standard and the enclosed (using RHBD techniques).

During radiation tests, both V_{th} shift and characteristic I-V curves from MOS transistors were monitored and measured, respectively.

In addition, TC949 included also simple FG core structures with different reading MOS (or p-MOS or n-MOS) in order to find out the response of similar structures but using different kind of reading MOS. Within this experiment, parameters as the radiation detection sensitivity and noise of the structure were monitored. Moreover, some capacitor structures were embedded in TC949, as well, but not measured. A basic schematic on the TC949 is shown in **Figure 32**.

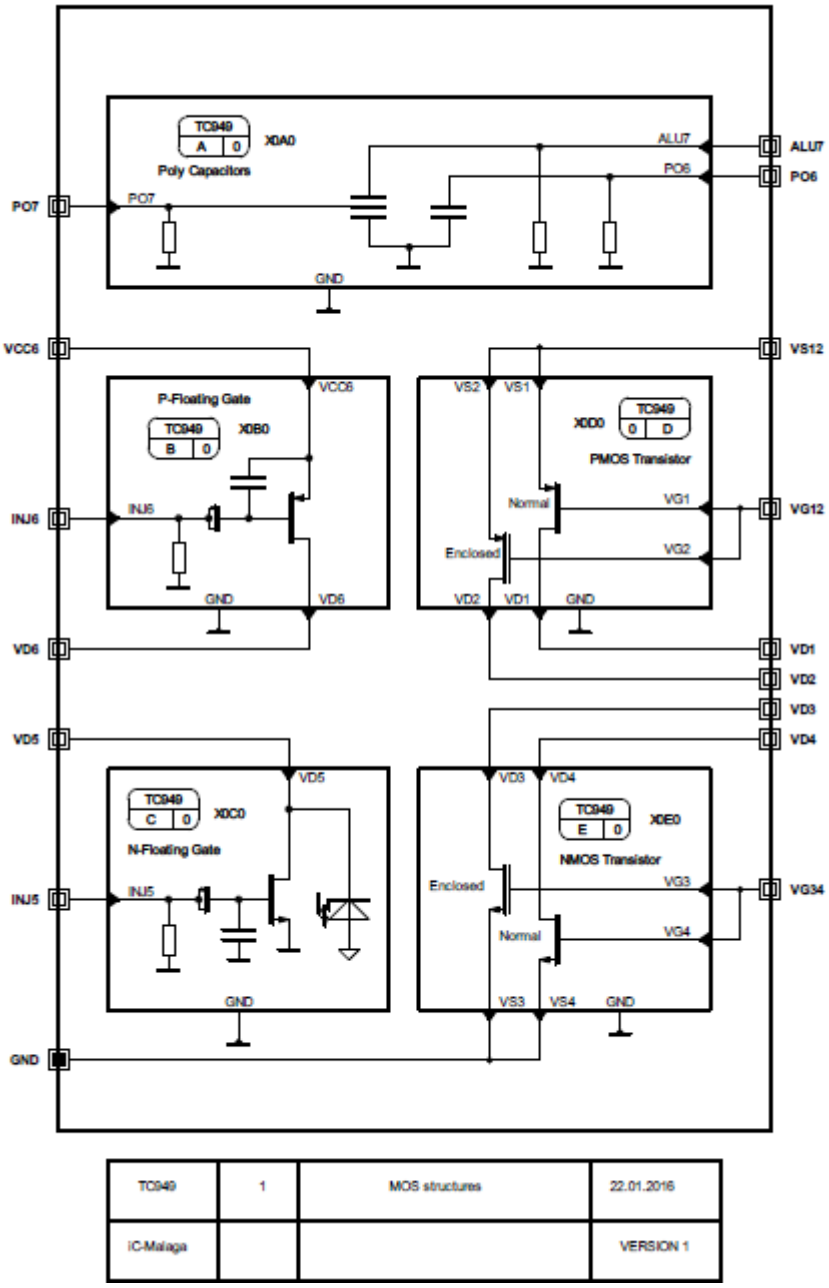

Figure 32. TC949 schematic

The measurements were carried out using a complex measuring system. The system consisted in three main parts, all of them controlled via computer. Part one, composed by a board embedding three TC949 in CDIP16 package, this board was the only one exposed to total ionizing radiation. Part two, including a matrix module (34934A) and connected to a multifunction switch/measure mainframe (34980A), this equipment permitted to switch online between kinds of measurement, during the radiation run. Last part, was in charge of measuring the parameters (voltage and

current) desired, depending on the measurement, and composed by an SMU unit (E5270B).

As different kind of measurements were carried out during the radiation, a LabVIEW software controlled some of the equipment. LabVIEW controlled simultaneously the matrix and the SMU unit configurations. Aside, power supplies were controlled via PXI from the computer too. A diagram on the complete setup architecture is shown in **Figure 33**.

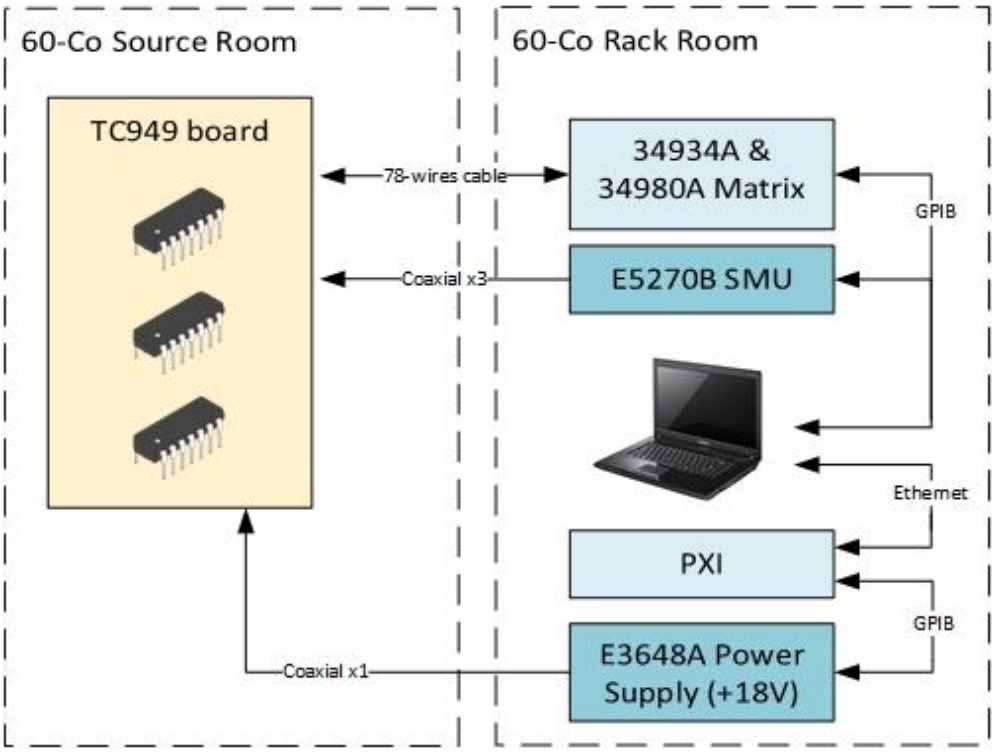

Figure 33. TC949 radiation test setup diagram

The kind of measurements carried out during the irradiation run were two. First, the V_{th} measurement on the single transistor structures where V_{GS} = 5 V and V_D = V_S = 0 V for n-MOS and V_{SG} = 0V and V_D = V_S = 0V for p-MOS, during the irradiation and set in diode configuration for the moment of the measure, and getting the V_{th} value by injecting a 100 µA in the diode. On the other hand, the second measurement was carried out on the FG core structures. Those were biased V_{DS} = 0.5 V during irradiation and measuring times. The measurement consisted on reading the I_{DS} or I_{SD} current either n-MOS and p-MOS reading MOS, respectively, during a full discharge of the FG due to the radiation. Finally, the characteristic curve of the MOS was extracted for the standard and enclosed MOS geometries before and after the

irradiation run. In that case, the shift on the characteristic curve was investigated. Both curves I_D vs. V_D and I_D vs. V_G were extracted.

In total, eighteen measurements were carried in all three TC949 under test during the irradiation by the LabVIEW-based system, six measurements each TC. Four measurements related to standard and enclosed MOS geometries, for p-MOS and n-MOS, and on the other hand two measurements on the p-MOS and n-MOS FG core structures. The sampling rate during the experiment was set to 5 seconds.

The test procedure consisted in irradiating all three DUT in the CC60 room, under a 60-Co source at a dose rate of 16.25 Gy/y up to a cumulated TID of 1.1 kGy. **Figure 34** shows a detail of the setup board position when placed at CC60 room for the 60-Co source irradiation.

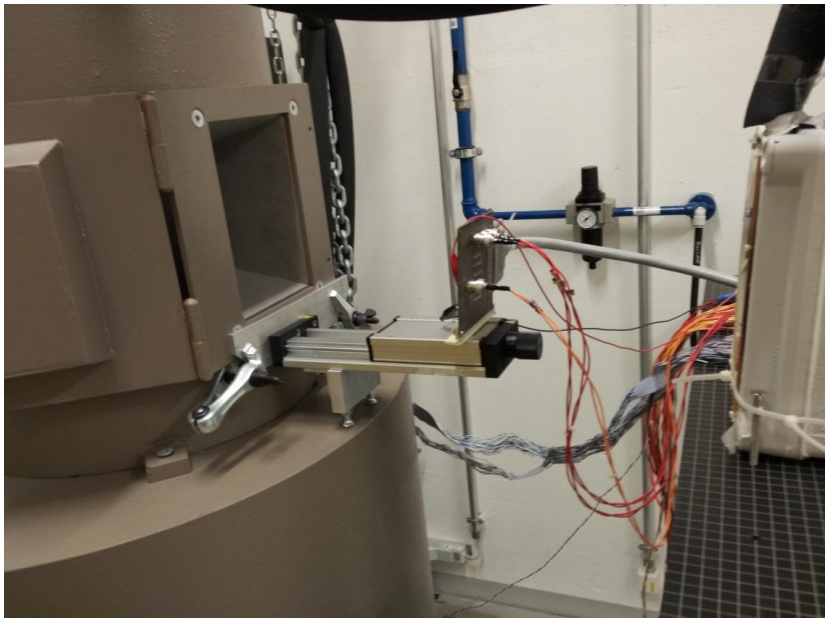

Figure 34. Setup position in front of the 60-Co source at CC60 room at CERN

The V_{th} measurements provided very interesting results, in the sense of better understanding TID effects in the technology used to design the FGDOS®. In **Figure 35** is shown the V_{th} shift experiment results in n-MOS and p-MOS transistors with both geometries standard and enclosed.

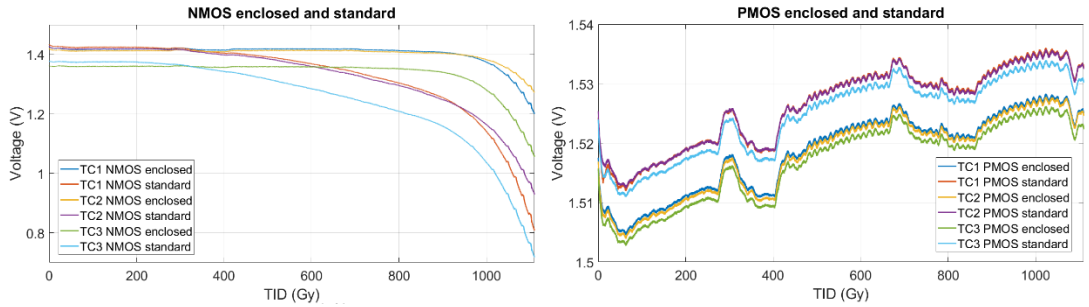

Figure 35. V_{th} shift measurement for, (a) n-MOS and (b) p-MOS, both standard and enclosed geometries

In standard n-MOS geometries, V_{th} shift started to be observed from 300 Gy of cumulated TID. The shift as expected (because carriers are electrons) for n-MOS transistors produced a decrease of the V_{th} when affected by TID. The degradation rate of the standard n-MOS geometries showed two different degradation rates. One, from 200 Gy up to around 900 Gy, of about -0.5 mV/Gy, and another from 900 Gy up to the end of the irradiation (1.1 kGy), of about -3.5 mV/Gy.

In parallel, enclosed n-MOS geometries V_{th} shift exposed to same conditions as standard geometries were able to withstand without any effect in terms of V_{th} shift up to around 900 Gy.

On the other hand, standard and enclosed p-MOS geometries showed similar behaviour when exposed to TID up to 1.1 kGy. Both of them had a positive V_{th} shift trend as expected (because carriers are holes) for p-MOS transistors but only of about +23 µV/Gy. Effects of return to negative values observed in **Figure 35**, are related to temperature dependence of MOS transistors during the experiment and amplified in the plot due to the very small shift of the V_{th}, both effects, temperature and V_{th} shift are in the same order of magnitude.

As will be commented later in this work in the ESD TID test results section, the effect of changing the slope in the V_{th} measured for the standard n-MOS transistor geometries was owing to the ESD protection leakage current at the gate of the transistors. This effect from the ESD added a current to the expected linear degradation of the V_{th} due to the oxide trapped and interface trap charges. The build-up of both oxide and interface trap charge is generated following a linear trend when exposed to TID with a constant dose rate. Instead, the effect from the ESD leakage

current follows an exponential trend, similar to the I_{DS} current from a MOS transistor when the threshold to start conduction from the parasitic transistor is achieved.

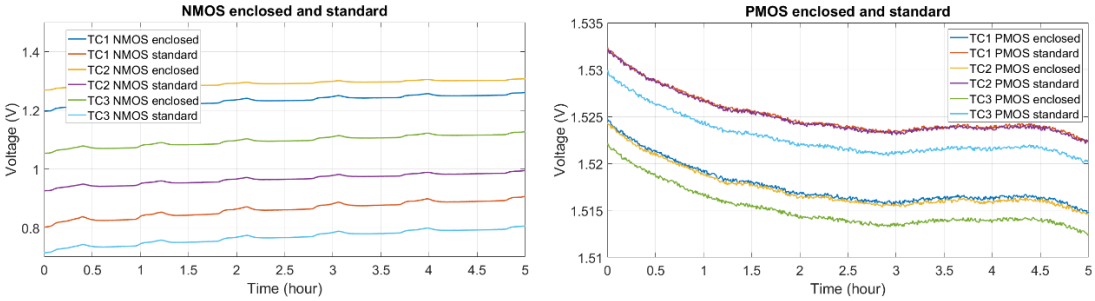

Figure 36. Annealing after 1.1 kGy of TID, (a) n-MOS and (b) p-MOS geometries

Annealing measurements carried out during 5 hours once irradiation stopped, showed expected trends, as it is appreciated when looking at **Figure 36**. Standard and enclosed n-MOS transistor geometries recovered few millivolts (≈ 100 mV for standard, and ≈ 50 mV for enclosed). Instead, for standard and enclosed p-MOS transistor geometries, the annealing effect was the same (≈ 10 mV of V_{th} shift recovering).

As previously pointed out earlier in this section, MOS transistor characteristics curves (p-MOS and n-MOS) were measured before and after irradiation in order to analyse and better understand TID effects along different working points in their characteristic curves (I_{DS} vs. V_{GS} and I_{DS} vs. V_{DS} curves).

Figure 37 and **Figure 38** present I_D vs. V_G curves for both types of MOS transistors and either standard and enclosed geometries. Post irradiation measurements were conducted after three weeks from the end of the irradiation campaign. Owing to this circumstance, the anneal of the V_{th} was practically complete and it is not the main effect appreciated in the plots. Instead, the nFET parasitic leakage due to interface traps has no anneal recovery and it can be seen as the major radiation effect in our post irradiation plots.

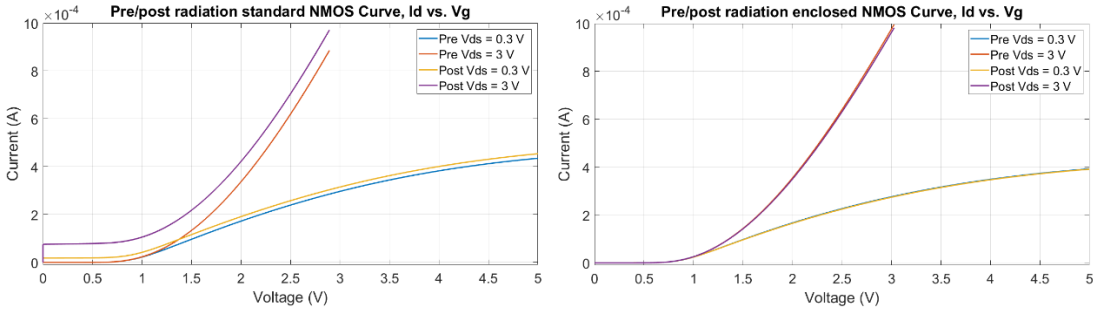

Figure 37. I_D vs. V_G curves pre and post radiation, (a) for standard and (b) enclosed n-MOS geometries

Pre and post measurements seen in **Figure 37** for different V_{DS} polarizations of the n-MOS transistor show the TID effect depending on the geometry. In (a) where standard geometry devices are plotted is possible to appreciate the V_{th} shift and how the devices are not able to achieve the non-conduction state after the irradiation. In addition, the effect of the parasitic nFET leakage current in the standard geometry is added to the V_{th} shift effect. Even with V_{GS} = 0 V a current I_{DS} is flowing. On the contrary, in (b) where enclosed geometry approach was used, the pre and post characteristic curve is the same. No effect is appreciated in that curve for enclosed n-MOS transistors.

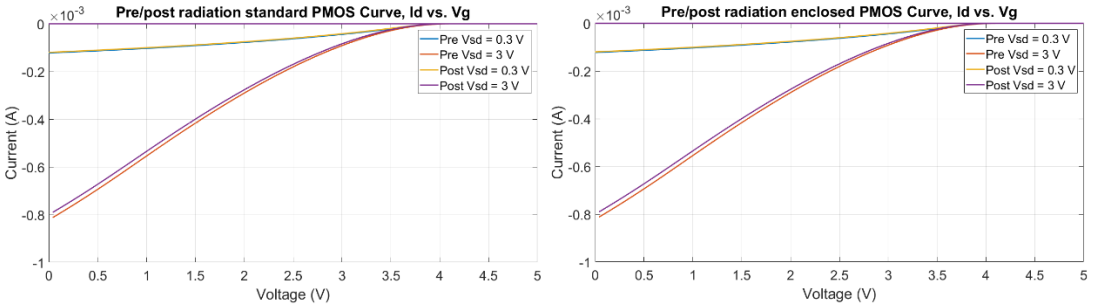

Figure 38. I_D vs. V_G curves pre and post radiation, (a) for standard and (b) enclosed p-MOS geometries

Nevertheless, in **Figure 38** where the I_D vs. V_G curve is plotted for p-MOS transistors, the effect of the TID cumulated is practically negligible. Pre and post irradiation characteristics curves in both standard and enclosed geometries are the same.

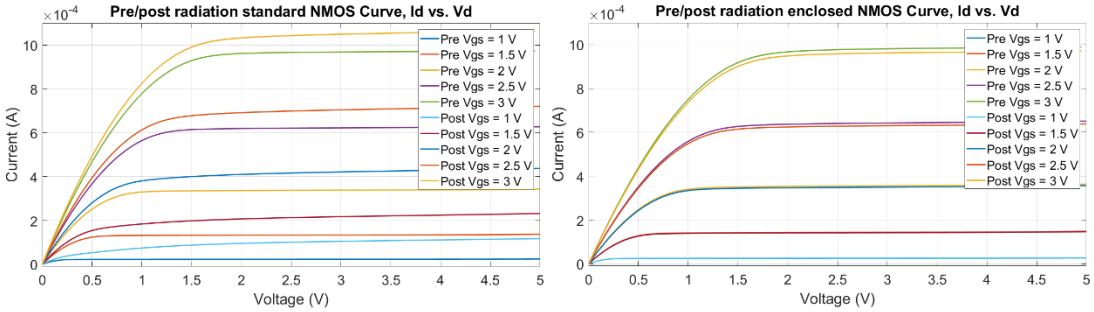

Figure 39. I_D vs. V_D curves pre and post radiation, (a) for standard and (b) enclosed n-MOS geometries

In **Figure 39**, measurement results for n-MOS transistors on both geometries are presented. Standard n-MOS geometry (a) has a large variation in the response in both the regions of the MOS. In the linear region from post irradiation measurements it can be seen how the device has a higher transimpedance, that is, a more pronounced slope in terms of current for the same V_{DS} and V_{GS} applied. This effect is even more visible in the saturation region of the n-MOS transistor. Here the complete saturation region is never reached. When V_{DS} increases, I_{DS} increases too, for post irradiated measurements.

When (b) is observed where enclosed n-MOS geometries pre and post measurements are shown, no difference can be appreciated between both measurements. Enclosed geometry has no TID effects in terms of I_D vs. V_D curve. As previously commented, the V_{th} shift was already practically annealed already and the nFET parasitic transistor leakage current is not present for enclosed geometries.

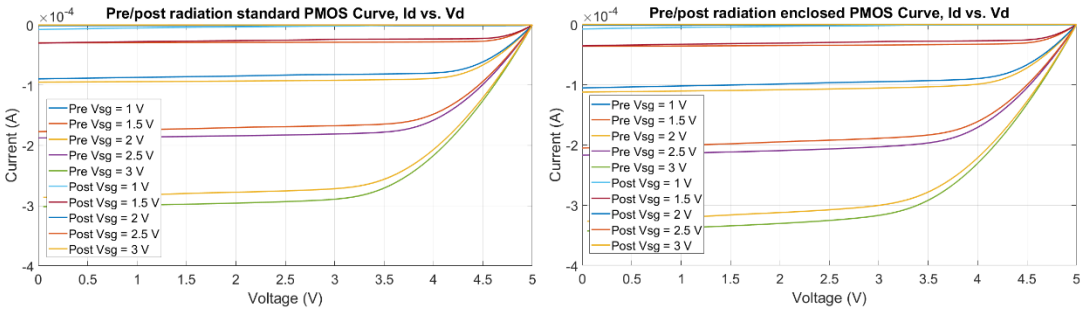

Figure 40. I_D vs. V_D curves pre and post radiation, (a) for standard and (b) enclosed n-MOS geometries

Standard and enclosed p-MOS transistor geometries are slightly affected in their I_D vs. V_D curves if pre and post radiation measurements are compared. As it is shown in **Figure 40**, p-MOS transistors have similar curves pre and post radiation but in post

radiation devices seem to be less resistive and have larger transimpedance in both linear and saturation MOS transistor regions.

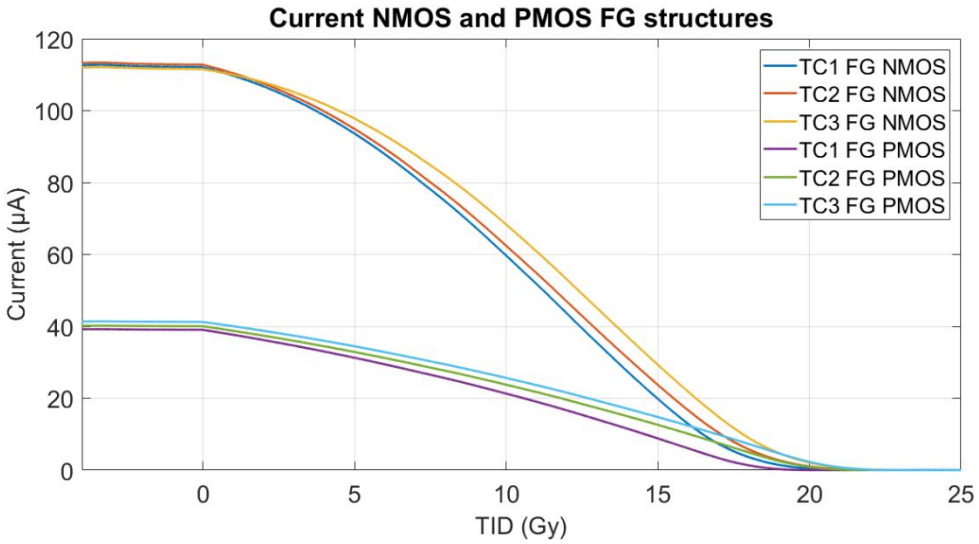

Figure 41. FG core structures with p-MOS or n-MOS reading MOS transistors

FG core structures complete discharge was measured to compare between reading n-MOS and p-MOS transistors. In **Figure 41**, are shown the results for both structures from all three DUT. The structures were the same in terms of area. Because to this, FG core structures with reading p-MOS were practically 3 times less sensitive than reading n-MOS structures. It is because n-MOS transistors have a smaller (approximately three times less) R_{DS} per unit area because of the different mobility between holes and electrons. Mobility of holes is lower than that of electrons and it affects directly in the p-MOS transistor response, if compared with n-MOS transistor, when area is the same. Therefore, FG structures with reading n-MOS transistors demonstrated to be a better candidate to be used in the new FGDOS® version. Similar response as reading p-MOS based FG structures can be achieved with near three times less area.

4.5.5. TC956, floating gate core structures, standard geometries

Design of TC956 was conceived to investigate the way to improve the new FGDOS® version, in terms of not only radiation tolerance but also sensor sensitivity to TID and sensor minimum detectable TID.

To face this challenge, first the study of different theoretical models had been done trying to predict the FG behaviour under TID. In addition, simulations on different FG core structures were also carried out to understand better the noise on this kind of structures. Finally, three topologies were designed and embedded in TC956 with the structure of the previous FGDOS® sensing core structure version, to compare against it. Once TC956 was designed and fabricated experimental measurements were conducted to crosscheck them with theoretical model and simulations results.

All work related to TC956 is presented in this section, and it came out with a poster presentation at RADECS 2017, in the dosimetry sessions [42].

As previously summarized in this section, TC956 design was focused on the FG core structure improvement. The FG core structure is the bare sensor block made of the injector, the FG capacitor and the reading MOS [1]. The sensitivity and response against radiation were compared to the prediction models to verify their effectiveness and improve future sensor structures. Moreover, it is well known that ionizing radiation produces an increase of the interface states at the Si-SiO_2 interface and of the charge trapped inside the oxides. Both effects are the main cause of MOS devices degradation due to the radiation. Being the FG based on a silicon dioxide structure these effects affect also the floating capacitance used as active sensor area and the injector and reading n-MOS. Because of that, it is very important the study of these effects in the technology of which the sensors are built [18, 43].

Two theoretical models were analysed and both models extrapolate the key parameters playing important roles for the FG sensor core sensitivity. First, it is presented the theoretical model developed in [2] by E. García-Moreno et al. which is based on the charge collection efficiency, hereinafter referred as “first model”. Secondly the theoretical model developed in [44] by S. Danzeca, which is based on the charge yield hereinafter referred as “second model”.

Both models are focused only in the FG behaviour when ionizing radiation is applied. Because of that, apart of the models, the effect of the reading MOS transistor in the core structure sensitivity must be considered. Two effects coming from it can improve the sensitivity; one the g_m of the device and the other the low frequency noise.

The first theoretical model on the FG charge collection efficiency is based on different assumptions as it is described in [2] and mentioned below. First, the assumption that the radiation generated electron hole pairs are all generated in the field region of the field oxide below the FG. In addition, the charge collection efficiency is assumed proportional to the electric field and assumed 0.1.

As can be seen in the equation 1, the electron charge q, the area of the FG (A_{FG}), the oxide density (ρ_{ox}), field oxide thickness (t_f), collection efficiency (f_0), the energy needed to generate an electron-hole pair ($W_{e\text{-}h}$), and the total capacitance of the FG sensor system (C_T), play a role in this model. All these parameters are used to describe the FG capacitance sensitivity (S) to ionizing radiation.

$$S = \frac{q\, A_{FG}\, \rho_{ox}\, t_f\, f_0}{W_{e\text{-}h}\, C_T} \qquad (1)$$

Nevertheless, if we make the assumption that in the total capacitance of the system only the capacitances from the n-MOS transistor, used as readout, are described and the FG capacitance is significant during the radiation detection process, the equation 1 can be re-written as follows:

$$S = \frac{\rho_{ox}\, t_f^2\, f_0}{W_{e\text{-}h}\, \varepsilon_{ox}\left[1+\frac{A_g\, t_f}{A_{FG}\, t_g}\right]} \qquad (2)$$

When the total capacitance is replaced for the effective areas of the transistor gate (A_g) and the FG (A_{FG}), and the gate oxide thickness (t_g) owing to the n-MOS transistor contribution.

From the equation (2), it can be seen how this model takes into account the geometrical ratio between the floating capacitor and the transistor as the main parameters for the sensitivity. All other variables are constants.

The second theoretical model on the FG charge yield sensitivity is based on different assumptions as it is described in [44]. Herein the main assumptions are; that the most significant effects to get an influence on the FG voltage are the electron-hole pair generation and charge trapping in the SiO_2 on both the top and bottom side of the FG capacitor. In addition this model considers only the volume covered by the FG over the field oxide for the sensitivity and discards the effect from the injector and the reading n-MOS because the first one is bigger (tens of times) than the other two.

In consequence the equation 3 to extract the sensitivity of the FG sensor block is composed by the charge density (g_0) generated by the ionizing radiation, the charge yield (f(En)) that is a function of the energy (En), the area of the FG (A_{FG}), the thickness of the oxide from the substrate to the FG polysilicon layer (t_{down}), the thickness of the oxide from the FG polysilicon layer up to the aluminium layer shielding in Metal 1 layer (t_{up}) and the sum of all the capacitances (C_{sum}), coming from the FG area, the reading MOS and the injector.

$$S = \frac{g_0 \, f(EN) \, A_{FG} \left[t_{down} + t_{up}\right]}{C_{sum}} \qquad (3)$$

From the equation 3, the sensitivity of the sensor can be calculated as V/rad. The equation shows how the sensitivity is directly proportional to the area of the FG and inversely proportional to the sum of all the capacitances. However, since the capacitance is directly proportional to the area and the capacitance from the injector and the reading MOS are very small compared to the FG capacitance, the sensitivity is not mainly dependent on the area of the FG. From this model then the increase of the sensitivity is coming from the thicknesses of the oxides and from minimizing the value of the sum of the capacitances of the sensor structure.

The theoretical models extract the sensitivity coming from the ionizing particles generated in the floating capacitor. On top of this, the overall sensitivity of the sensor comes from the multiplication of the sensitivity, S, given in V/rad, for the transconductance (g_m) of the reading MOS which permits to have a current output proportional to the charge on the FG.

The g_m from the reading n-MOS in theory can infinitely increase the sensitivity of the sensor block. Nevertheless, this is not true because the bigger it is the reading MOS area, the worse it will be the FG sensitivity owing to the capacitance increase (see equation 3). In addition, the low frequency noise [45] coming from the reading MOS geometry can be reduced by increasing the area of the device and make its length (L) as large as possible. This assumption leads to an exponential distribution therefore at relatively small areas it is possible to reduce the noise more than 90 %.

Thus, the g_m and the noise follow similar objectives to improve them. The g_m needs width (W) larger than the L or keep the ratio W/L large. The noise needs large L and

large W. Due to these constraints both of them are not good to improve the sensitivity on the FG because they increase the capacitance on this node.

Along with the verification of the FG sensitivity models, several simulations have been carried out for the g_m and noise in the reading n-MOS. These simulations were also used to design the real structures presented in the following paragraph.

After the analysis of both, theoretical models and simulations, four different structures were designed and embedded in TC956. The four different candidate structures were:

1. Structure 1: previous FGDOS® version, FG core structure
2. Structure 2: Lower noise, FG core structure
3. Structure 3: Smaller area, FG core structure
4. Structure 4: Best performance, FG core structure

All four structures consist of a FG capacitance, one reading MOS and one injector. The structure 1 is the same used in the previous FGDOS® version [3, 4, 8 and 46] and implemented to be compared with the other three, thus taken as the reference structure. In the structure 2, the only difference with respect to the structure 1 is the increase on the reading MOS area, in order to improve the noise. Moreover, the g_m was increased to compensate the loss of sensitivity due to the reading n-MOS capacitance increase. The structure 3 made the FG area four times smaller and kept the reading n-MOS area the same as the structure 1. With this structure, it was possible to verify if saving area on-chip would be possible to have the same sensitivity as predicted by the models. Finally, the structure 4 was designed to try to have the best performances in terms of better noise response and keeping high sensitivity. In this case, the reading MOS and the FG area were increased but the ratio W/L was kept as in the structure 1.

These four structures had been developed to verify if the FG theoretical models and the noise simulations fit with the experimental measurements.

In addition, four dummy n-MOS transistors were implemented on-chip next to the reading n-MOS of each structure with the same size and topology. These dummy structures were used to set the exact same voltage in the FG for each structure by measuring the current for an applied V_{DS} at the structure, it meant that the desired amount of charge was already placed at the FG to generate same V_{GS} voltage than

in the dummy when same current was measured on it. With such a process, it was possible to compare all four structures under the same initial polarization conditions (same initial V_{GS}, or voltage at the FG).

Table 6. FG theoretical model calculations.

Structure	First model		Second model	
	S [mV/rad]	ΔS* [%]	S [mV/rad]	ΔS* [%]
1	1.10	100	1.71	100
2	0.78	71	1.29	75
3	0.86	78	1.39	81
4	1.05	95	1.57	92

*ΔS is the sensitivity percentage with respect to structure 1.

The sensitivities of the structures described above have been calculated using the theoretical models. **Table 6** reports models results for each proposed structure. It can be noted that the results from the two models differ because they use different approximations to describe the FG discharge behaviour owing to the ionizing radiation.

In the structure 2 the W/L ratio changed from 6.66 as in the structure 1 to 8.90 (33.6 % more) to try to compensate the loss of sensitivity due to the reading n-MOS area increase in the readout current. All other structures kept the W/L ratio at 6.66. In addition, noise simulations had been carried out to choose the best n-MOS W/L ratios and sizes to minimize the noise without much reduction in sensitivity of the sensor. Those simulations were carried out for a low frequency noise of 1 kHz and with V_{DS} = 0.5 V and V_{GS} = 4.2 V using iC-Malaga's noise models, which are provided by the fab for each device. In **Table 7** the simulations and experimental measurements are reported. It can be noted how the noise is reduced when the reading n-MOS transistor area is increased, for example in structure 2.

Table 7. Reading n-MOS noise simulations and measurements

	Simulations		Measurements	
Structure	**N [nA_{pp}]**	**ΔN* [%]**	**N [nA_{pp}]**	**ΔN* [%]**
1	6.6	100	5.3	100
2	3.4	52	3.0	56
3	6.6	100	4.0	75
4	2.5	38	3.7	69

*ΔN is the noise percentage with respect to structure 1.

The results obtained in either noise measurements and simulations were very similar. The results for each kind of structure were within the same order of magnitude. If they are compared one by one, noise behaviour between structures is correlated. Nonetheless, the absolute values differ by some nano amperes depending on the structure. The main variation, which can explain the small difference between simulations and measurements, is that in structure 4, the reading n-MOS and the FG were measured and in simulations, only the reading n-MOS was considered.

The radiation characterization process was carried out in the CC60 room at CERN, under the 60-Co source, performing one complete discharge of the structures and irradiating up to 49 Gy at 1.25 Gy/h. **Figure 42** shows the discharge process of all the structures monitored during the irradiation.

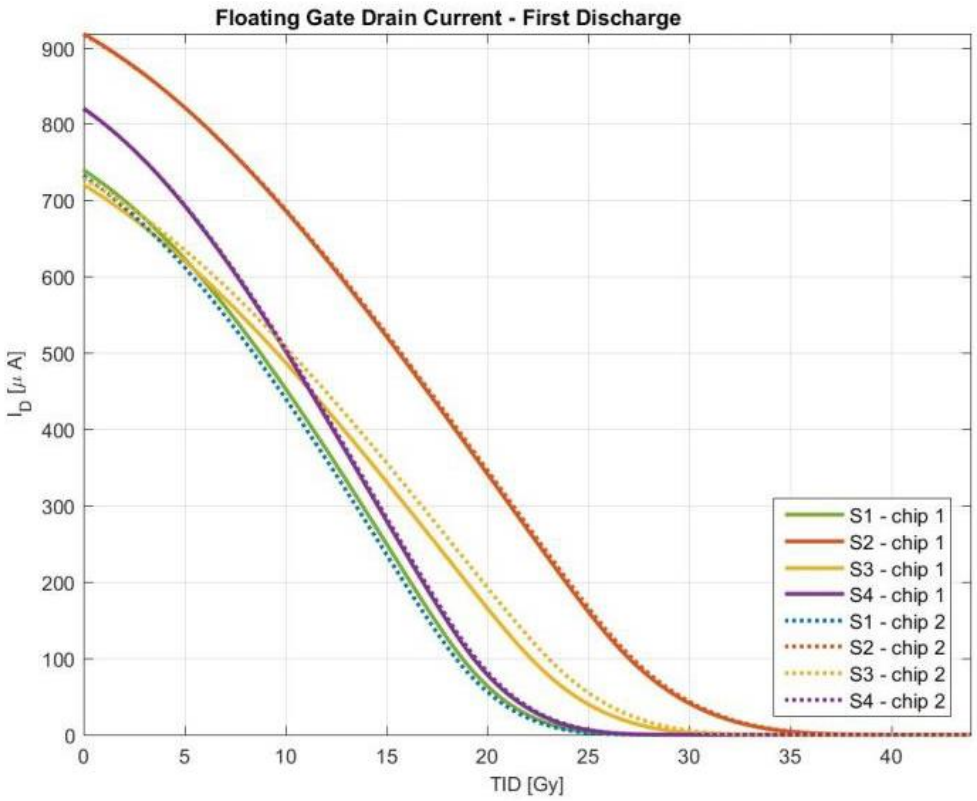

Figure 42. FG core structures complete discharge. Results from two TCs with four FG structures each. Irradiated under 60-Co at CC60 room

As it is observed from **Figure 42**, different starting points on the output currents given by different kind of structures can be noted. It is due to the same FG initial voltage setting condition. It can be seen also how between different TCs it is obtained the same shape during the complete discharge for the same kind of structure meaning that all the structures in different chips behave the same. **Table 8** shows sensitivity results as a comparison between theoretical models and measured data on proposed structures.

Table 8. FG models and TC data measurements comparison

	First model		Second model		TC data	
Structure	**S [mV/rad]**	**ΔS* [%]**	**S [mV/rad]**	**ΔS* [%]**	**S [mV/rad]**	**ΔS* [%]**
1	1.10	100	1.71	100	2.00	100
2	0.78	71	1.29	75	1.53	77
3	0.86	78	1.39	81	1.70	85
4	1.05	95	1.57	92	2.02	101

*ΔS is the sensitive percentage with respect to structure 1.

Comparing both models, one notices the same trends in sensitivity for all tested structures. Instead, if absolute values of those measurements are compared with results obtained from the models, the first model has a factor two of difference and the second model only the 30 % difference compared to data from experimental measurements. Structure 2 is more sensitive than expected in TCs due to the geometry of the transistor. Larger transistor means better g_m. In this case, also the W/L ratio was enlarged. Structure 3 was more sensitive than expected because of the perimeter effect at the capacitance on the detection where the electric field is stronger and it is not considered in the FG models. Finally, structure 4 was slightly more sensitive for the same reason as structure 2, where a larger transistor area is implemented, resulting in better g_m for the same W/L. In addition, comparing theoretical models, the second model fits better with experimental results, as the charge yield value is extracted from measurements and considers the entire FG volume (top and bottom sides of the FG capacitance are considered and the capacitance associated with the injector and the reading n-MOS discarded) as detection area. The limitation of the first model is the assumption on the collection efficiency and the fact that the FG detection volume is not considering the surface below the FG.

The work done on TC956 can lead to design a better performance FGDOS® in terms of noise and sensitivity. The prediction of the FG radiation detection behaviour is well described by both models but the second model from S. Danzeca [44] shows a strong correlation with the experimental measurements collected. The new FGDOS® version considered both theoretical models during the design process. In addition, both the noise and the g_m were also considered to make a better FGDOS® dosimeter in sensing the TID.

Further work was done on TC956. That work was focused in investigating the sensitivity degradation in FG core structures [47]. This research is still on going and pending for publishing more results in 2019. This work is part of another PhD thesis, and it is out of the scope of this work although there is co-authorship.

4.5.6. TC971, standard and radhard references

It is well known that an important circuit in any chip design is the references generator circuitry. Usually these circuits are in charge of generating all voltage and current references needed in other circuitries within the chip.

The references produced by these circuits have to be accurate, stable against power supply, temperature and fabrication process variations. In our case, also it is needed the design of a stable reference generator, under ionizing radiation environments for at least a cumulated TID of 1 kGy. Following this purpose, the design of TC971 was raised.

TC971 design was complex owing to the importance of the reference circuit within the FGDOS®. Hence, first steps were done to try to understand better TID effects in standard CMOS technology and more precisely in bandgap references, as previous FGDOS® version reference circuit was based on a bandgap reference circuit. Thus, the main challenge by using a bandgap reference [48, 49] is that those kind of references are based on bipolar devices and bipolar devices have a different TID degradation behaviour than CMOS devices [50, 51, 52, 53, 54 and 55].

In parallel, other topologies or design approaches of voltage references were investigated to make the reference circuit hard or tolerant to ionizing radiation. MOS based voltage references were a good candidate due to their well-known TID responsiveness if RHBD techniques are used during the design process but instead

MOS based references in general are less stable and worse references than bipolar ones, among other causes because of worse device-to-device matching and sample-to-sample device characteristics variation during the fabrication process. Thus, MOS based voltage references are less precise than bipolar-based ones.

In TC971, three voltage reference designs were embedded. One bipolar based voltage reference using RHBD techniques, herein after referred as VBGR reference. Another, the MOS based voltage reference using RHBD techniques (herein after named as VBGM) and only CMOS devices (p-MOS and n-MOS transistors only and passive components as capacitors or resistances). Finally, the voltage reference used in the previous FGDOS® version, bipolar based and standard layout implementation (herein after cited as VBG). All three references and single bipolar structures were embedded in TC971 design as it is shown in the schematic from ***Figure 43***.

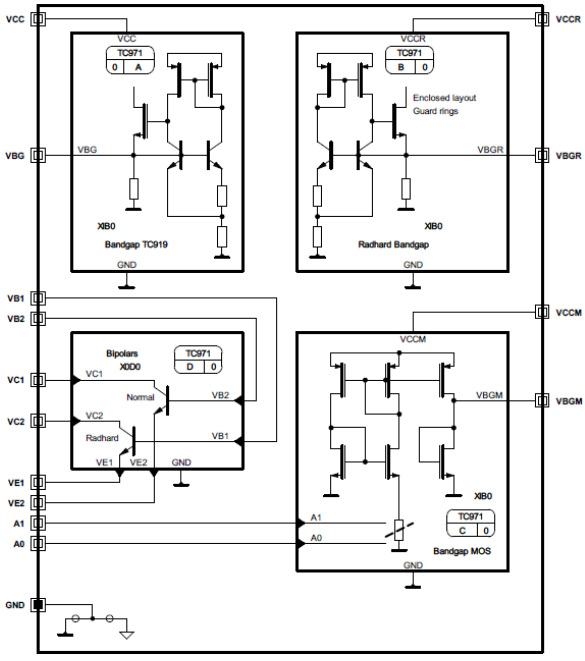

Figure 43. TC971 schematic

Single bipolar structures were not tested because bipolar-based voltage references highlighted a good performance during the radiation campaign up to 1 kGy of cumulated TID. Their results are presented and discussed later in this section.

The VBG reference design implemented a standard layout design based on bipolars, p-MOS and n-MOS transistors, and resistors and capacitors. It was the same design used in previous FGDOS® version.

Instead of VBG voltage reference, in VBGR reference, during the design process RHBD techniques [32, 33, 34, 56 and 57] were applied to increase the TID lifetime of the circuit. In addition, the temperature dependence at the output of the circuit and the current consumption were enhanced if compared with previous design. Bipolar transistors were vertical NPN transistors with enclosed layout. Polysilicon layer plates were added between terminals (base, emitter and collector) of the device connected to ground, in order to avoid positive charge deposition in the field oxide, avoiding possible parasitic transistors conduction. Finally, guard rings between devices were used. In MOS transistors side, n-MOS transistors were only used for the start-up circuitry, and voltage reference design slightly changed in order to use only p-MOS transistors. Guard rings surrounded all MOS transistors in order to avoid parasitic transistors between devices when charges are deposited in field oxide due to ionizing radiation.

MOS based voltage reference design was complex. Different architecture options were investigated. First of all MOS voltage reference based on weak inversion [58, 59, 60], but this approach was not used finally because of the simulations models used, where weak inversion is not well described and the error during the design would be too large. Hence, a MOS voltage reference based on a diode and a current generated with a proper temperature dependence in order to compensate the output voltage dependence to the temperature was designed [61, 62, 63]. Due to current temperature-dependence fine-tuning, VBGM reference design included two configuration bits for resistors tuning purpose. All n-MOS transistors used during layout design process were with enclosed geometry and guard rings.

Table 9. TC971 voltage references simulated characteristics

Reference	I_{VCC} [µA]	V_{REF} [V]	$T_{coeff.}$* [ppm/ºC]
VBG	240	1.26	+ 342
VBGR	220	1.17	- 62
VBGM	50	1.15	- 575

** Within range of temperature from -40 ºC to 125 ºC*

Table 9 compares some design parameters from voltage references exposed. VBGR reference design was enhanced and tuned by improving all parameters with respect to other references.

When TC971 was fabricated and first prototypes arrived in house, a radiation campaign was conducted at CC60 room. Checking the TID lifetime of the voltage references was the aim of the test. To do so, measurements on some parameters from all three voltage reference circuits were carried out during the test.

The set of parameters monitored were three on each reference circuit. From one side, the output voltage on each reference circuit; expected to be similar to the one simulated during the design process as shown in ***Table 9***. On the other side, in parallel each supply voltage and current were measured using two power supplies, E3648A and E3649A. Three power supply channels (each VCC from each circuit) and three channels for measuring the output voltages, using 34921A MultiDAQ with 34980A measuring unit embedded, composed the measuring setup. All equipment was controlled and data logged via BenchVue software from a computer.

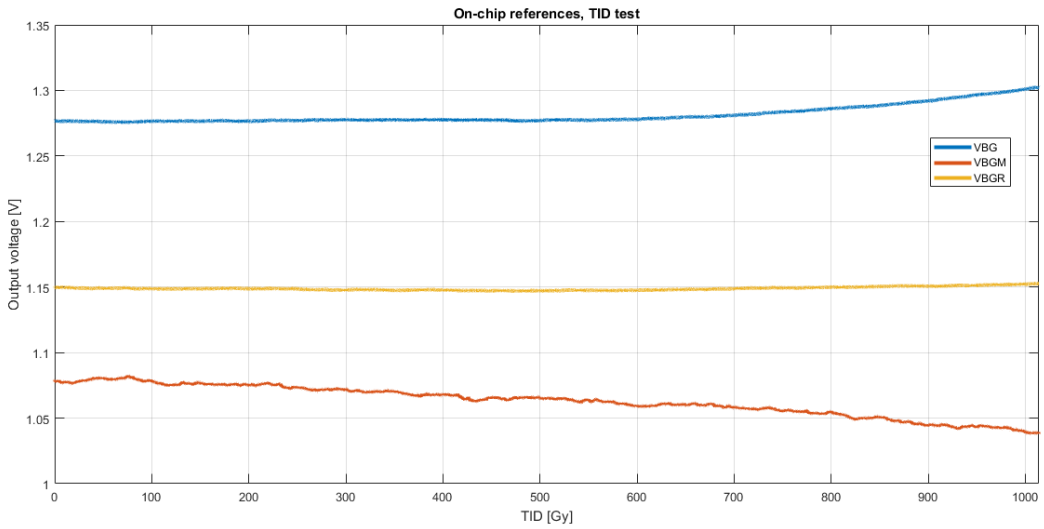

Figure 44. Output voltages from all three voltage references candidates under TID exposure at CC60 room

TC971 position inside CC60 radiation area allowed a dose rate of 9.16 Gy/h during the test. A TID of 1016 Gy was achieved after 111 hours.

The results obtained during this campaign contributed in a better understanding of TID effects in FGDOS® circuits. As it is shown in ***Figure 44***, all proposed architectures endured the output voltage regulation up to the end of the test, up to more than 1 kGy of TID. VBG reference had a regulation voltage of about 1.27 V, VBGR reference of 1.15 V and VBGM reference of 1.05 V, all of them inside expected regulation values. However, VBGM showed a noisy behaviour in the output voltage whereas VBG and VBGR were very stable.

An effect of voltage regulation drift was observed in VBG and VBGM references. This effect was caused by the increase of temperature experienced while TID was being cumulated in the circuitry and can be better understood by having a look at the monitored current consumption curves.

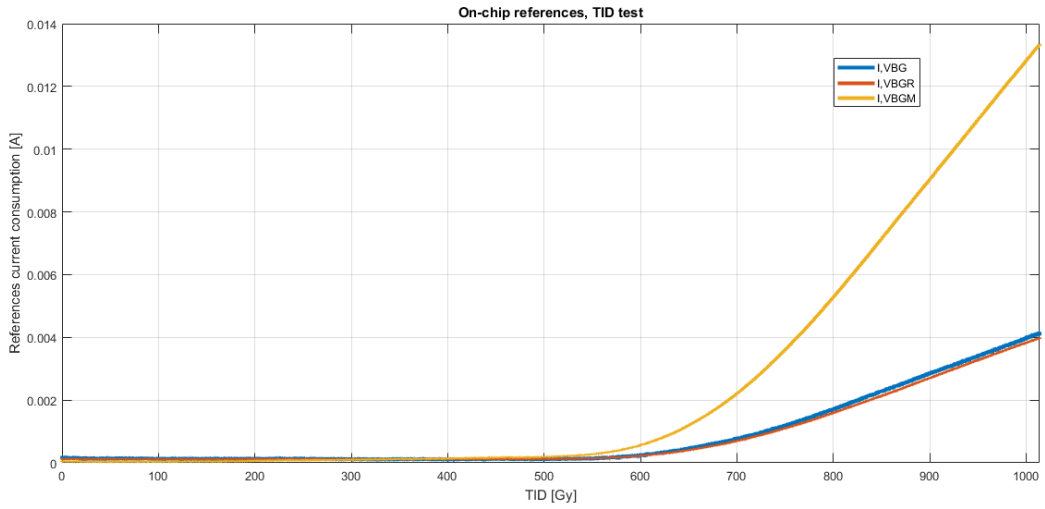

Figure 45. Current measurements profile under TID exposure at CC60 room for all three voltage references candidates

Current consumption increase was observed from 500 Gy and experienced an exponential increase. As it can be seen in **Figure 45**, all currents highlighted this behaviour. Nevertheless, VBG and VBGR reference circuits had very similar increment, but on the contrary VBGM reference circuit showed an increment of about three times more than other two.

After looking at the TC971 design, it could be pointed out that the difference between the references was the number of pins connected at V_{CC} in each case. Whereas in VBG and VBGR references only the V_{CC} pin was connected to the power supply (+ 5 V), in VBGM design three pins were connected to + 5 V, its V_{CC} and the two resistor tuning configuration pins. By considering this, immediately was found out that the source of the current increase was the ESD protections embedded in each pin. These protections were standard ESD structures, and its geometry made them especially specially sensitive to ionizing radiation owing to snapback feature, where two n+ doped lines placed one next to the other, without any guard ring, and at different potentials (one at + 5 V and the other to ground).

The difference of potential amplified the current consumption increase due to the trapped charge in the field oxide between both n+ lines, allowing the parasitic npn transistor to start conducting current.

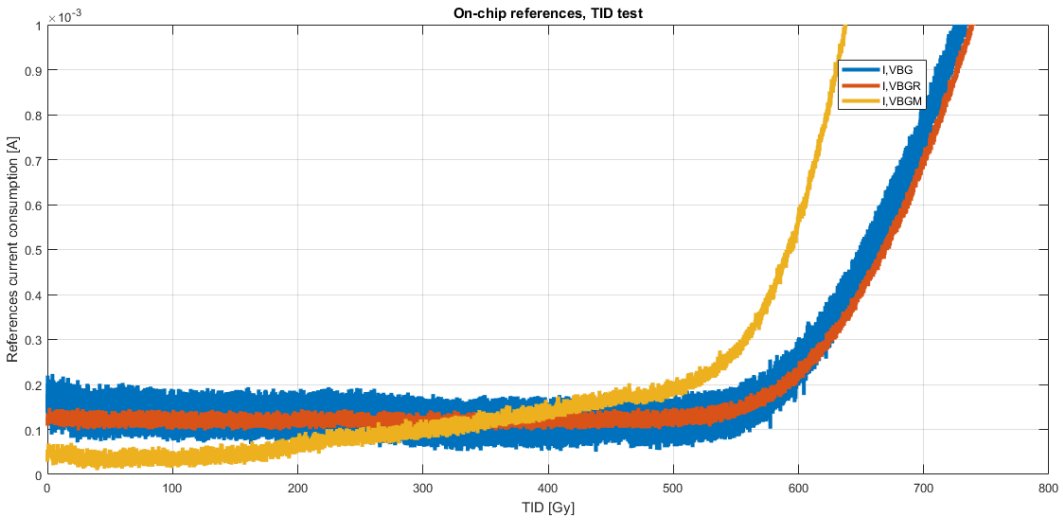

Figure 46. Detail on current measurements profile from **Figure 45**. Different TID effects are observed depending on the voltage reference circuit

Moreover, if current consumption curves were zoomed in to have more detail, as it is done in **Figure 46** another effect could be find out. VBGM reference showed different current slopes depending on the TID cumulated. Up to 100 Gy, it was stable and constant, and also it can be seen from **Figure 44**, how the regulated output voltage was stable up to this point. It means, that no relevant degradation was observed in the circuitry. However, from 100 Gy up to 500 Gy, a linear degradation of the current consumption was pointed out. This behaviour can be attributed to the V_{th} shift in the n-MOS transistors. Even using enclosed geometries it is not possible to stop the V_{th} due to the oxide and interface traps generated by the ionizing dose. Finally, the third slope appreciated was due to the ESD protection, starting from 500 Gy.

Instead, VBG and VBGR references were very stable in terms of current consumption up to 500 Gy, where the ESD protections degradation was observed. Both voltage references were not using n-MOS transistors as current mirrors. Only VBG reference was using n-MOS transistors as follower in a regulated node and both references n-MOS transistors in the start-up circuitry that did not play an important role when the circuit is biased and then working.

Results collected after testing TC971 against TID, presented important effects and behaviours from designed circuitries. VBGR demonstrated to be the best architecture and because of that the candidate to be used in the new FGDOS® complete version.

In addition, other effects were found out, as the ESD protections degradation. This effect is studied in more detail in another TC design and presented later in this work.

4.5.7. TC974, new FGDOS® complete version

This section focuses on new FGDOS® version design. The conception process followed is explained, and characterization results from radiation tests campaigns are presented and discussed. Designing the new FGDOS® complete version was the main task of this thesis. All TC designs presented earlier in this chapter were conceived to finally be included or used in this new design somehow. New FGDOS® complete version design would not have been possible, without first having followed a firm and well-organized work process. Hence, resulting of this, new functionalities and enhanced abilities of the sensor had been designed and tested with a positive outcome.

During this thesis, two different designs of TC974 were fabricated and tested. A first version designed and fabricated during the second year of the thesis and a final version produced, during its last year. Due to very limited access to tape outs and therefore to silicon in order to fabricate new prototypes, first version was designed to include already all possible improvements already known at that time. The second and last version included finally all major improvements and functionalities to obtain an entirely functional new FGDOS® version design.

In **Figure 47**, it can be seen the block diagram of the TC974. It is essentially, as previous FGDOS® version, but including all new functionalities discussed later in this section.

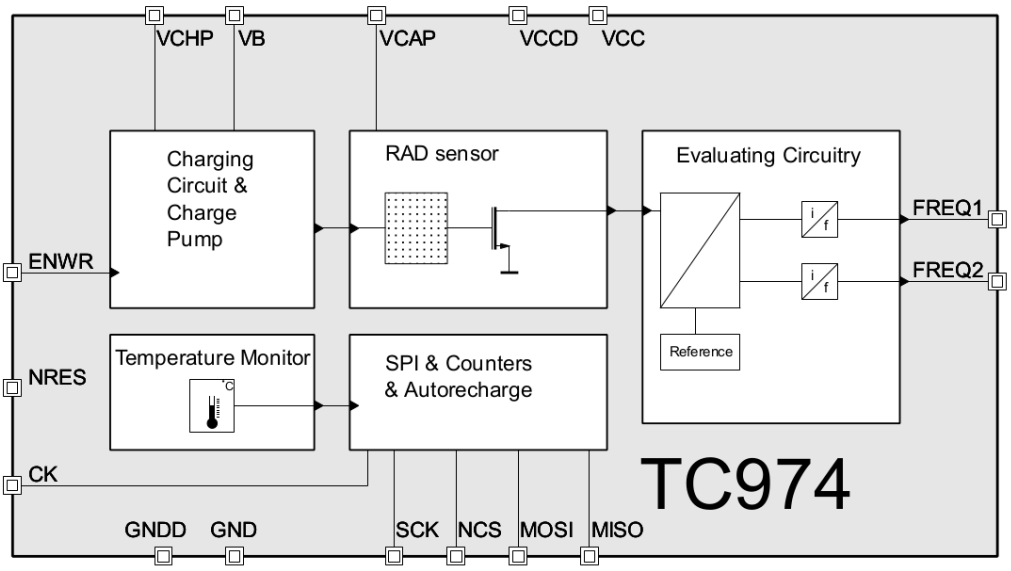

Figure 47. TC974 block diagram

First design included all analogue circuits made using RHBD techniques, i.e. reading n-MOS, references, temperature sensor, charge pump and input/output path circuits. Only the digital circuitry was not implemented using those techniques because the design flow and digital cells were not ready at this time, to include RHBD techniques. In addition, some new functionalities were already included, as for example the high voltage generation on-chip to carry out the recharge of the FG (done by the charge pump circuit), or the controlled discharge of the FG (via the VCAP pin) or sensor sensitivity increase (by modifying the reading n-MOS ratio).

Second (and last) design implemented already all circuits with a RHBD techniques based design. In this case, first, area constraints on the chip were considered. This came up, due to larger area needed to implement all RHBD circuits, and became more problematic with all digital circuits, where high number of devices are found on them. This way, the new design could still be embedded in the QFN 32-pin package, including two sensors each. Then, other aspects in the design were improved. These were, the charge pump circuit (different output voltage ranges compared to previous version and one more stage, to improve output voltage performance), or the inclusion of an ultra-low power mode (when NRES pin pulled to 0, the whole chip circuits lower the consumption, ≈ 10 μA). Moreover, an ID number was embedded (in order to identify each exact chip), or a dummy n-MOS was included next to the reading n-MOS (to compensate the loss of sensitivity of the sensor owing to TID effects in the

FG response) via pin, when the compensate mode is activated. Finally, by making the placement and route carefully in the whole layout, it was pretended to lower the noise of the sensor as much as possible.

Regarding to tests carried out on both versions, first version was tested to check its dose rate and TID lifetime response. In addition, a comparison between new FGDOS® and another dosimeter (RadFETs devices) was carried out at CHARM facility to compare their performance under a fast-pulsed mixed field environment. Finally, to crosscheck the source of other effects observed during the TID lifetime test, a thermographic test was carried out to find which are the hot spots in the chip, and in order to understand better weakest regions and circuits. To conclude this section, second version tests were focused in the sensitivity and TID lifetime. All these tests and results will be presented and discussed below. More experiments as thermographic test or at CHARM facility, are under preparation, but are out of this work due to time constraints.

The first experiment carried out was the dose rate experiment. This experiment was performed in the CC60 room under a 60-Co radiation source, using the TIDmon measuring system (see **Figure 48**).

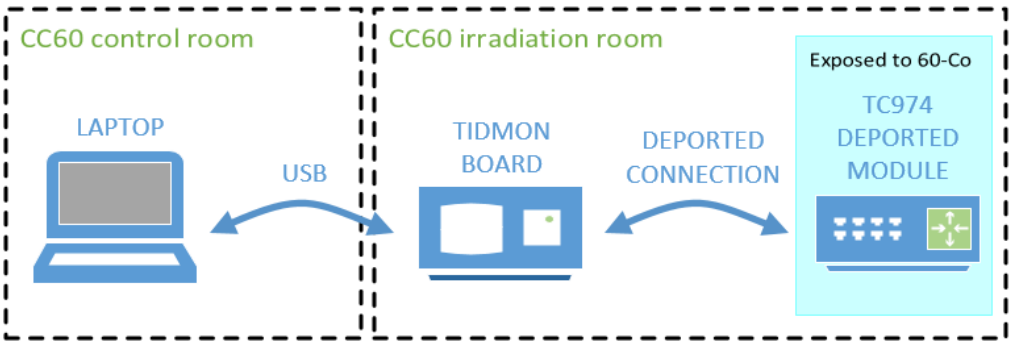

Figure 48. Measuring system used at CC60 room during TC974 radiation campaign

The dose rate experiment conducted in the first version revealed the dependence of the FGDOS® detection on different dose rates. Two different dose rates were tested in two chips (see **Table 10**). One run at low dose rate (LDR), 0,32 Gy/h and another run at high dose rate (HDR), 2,62 Gy/h.

Table 10. TC974 version one dose rate response, in two sensors

Dose rate	HDR Sensitivity [kHz/Gy]	LDR Sensitivity [kHz/Gy]	Variation [%]
Sensor 1	60.87	57.71	-5.2
Sensor 2	58.16	54.31	-6.6

As it is shown in **Figure 49**, the sensitivity decreases with lower dose rates. This effect was already reported at [3, 4]. This can be explained because carriers are able to move easier towards available holes and recombine in the FG when lower dose rates are applied, because less carriers are generated for the same amount of holes available. Moreover, the decrease of the sensitivity can be related to the calibration done with the ionizing chamber. When higher dose rates are calibrated, the errors are higher than in lower dose rates, where a variation on the position from the source affects less the dose rate calibration.

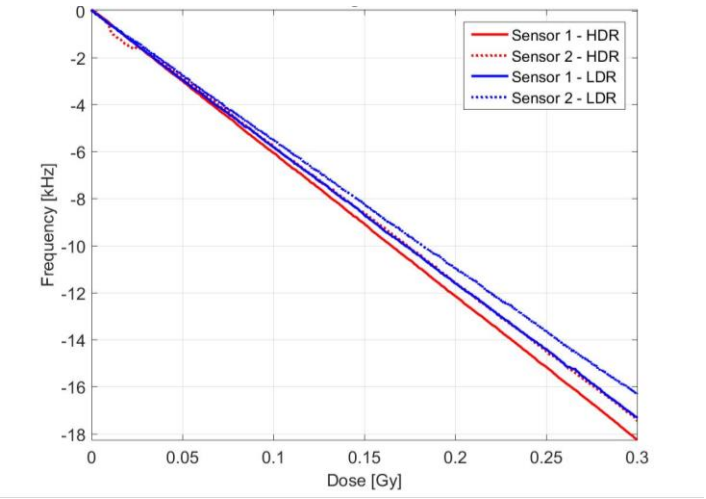

Figure 49. TC974 version 1, dose rate experiment in two different samples

In addition, from the dose rate experiment, it was obtained the sensitivity of the new FGDOS® and it practically doubled that of the previous version (≈ 60 kHz/Gy, instead of ≈ 30 kHz/Gy).

After having tested the dose rate and sensitivity of the first version, a TID lifetime test was carried out in order to foresee how much lasts the chip working properly when TID is cumulated. This test was performed in the CC60 room with two sensors as well at a dose rate of 24.61 Gy/h.

As it is shown in **Figure 50**, both sensors were still detecting radiation above 300 Gy of TID. Concretely, sensor 1 lasted up to 320 Gy and sensor 2 up to 310 Gy.

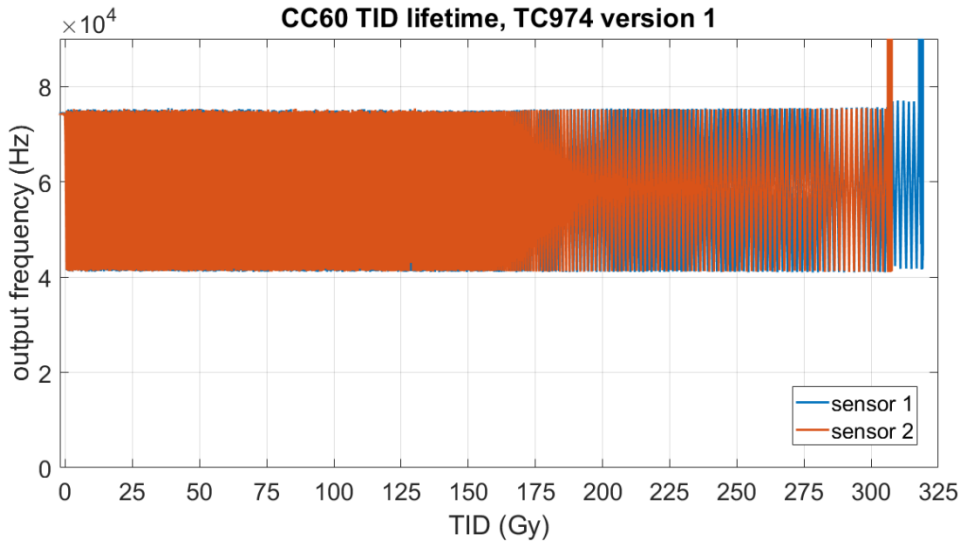

Figure 50. TC974 version 1, TID lifetime experiment, output frequency from sensor 1 and 2

However, both sensors experimented other secondary effects before its complete failure. A current consumption increase was observed (but not monitored) along the experiment starting from 100 Gy, probably owing to the circuitry with standard design (not using RHBD techniques). In addition, a variation of the sensitivity has been observed. Finally, a longer time needed during recharge process has been also noticed, probably due to TID effect in the charge pump circuitry, affecting directly to its output voltage. In **Figure 51** and **Figure 52**, details on TID lifetime experiment, at 0 Gy and 300 Gy regions are presented respectively. Both effects longer recharge time needed and sensitivity variation can be appreciated.

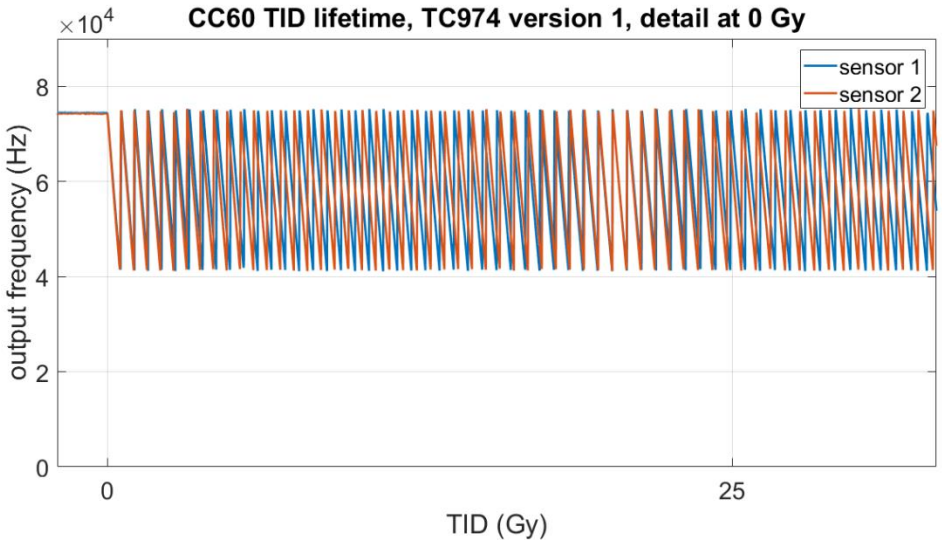

Figure 51. TC974 version 1, TID lifetime experiment detail, when 0 Gy were cumulated

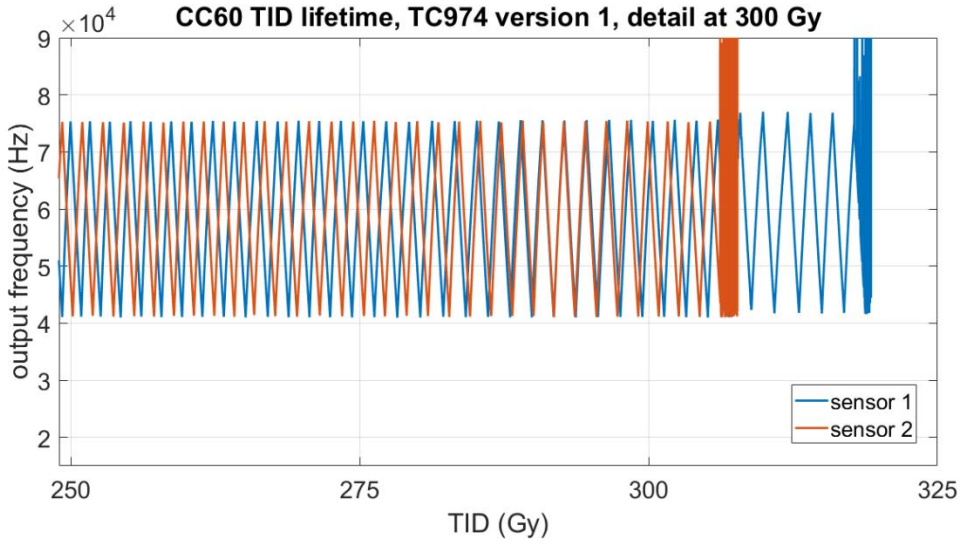

Figure 52. TC974 version 1, TID lifetime experiment detail, when 300 Gy were cumulated

Once TID lifetime experiment results were analysed, the first open question was why chip was still having a promptly failure (lifetime was enlarged only 50 Gy with respect to previous FGDOS® version). Thus, the source of this increase of current consumption and loss of functionality had to be find out. A way to do so would be to analyse the degradation of the chip, when TID is applied, by making a thermography on the chip [64, 65 and 66]. By doing this, it would be possible to see which zones of the chip demand more current when TID is being cumulated.

The experiment was conducted in a single chip of TC974 version 1 and radiation was exposed in different runs at CC60 room. First run, up to 100 Gy, and afterwards,

in steps of 50 Gy, up to a total cumulated TID of 300 Gy. In between, thermographic pictures were taken on the chip area. The dose rate used for the calibrated position was 6 Gy/h in run 1, and 53 Gy/h for all other runs, 2, 3, 4 and 5. The test setup was the one used in previous TC974 experiments (see **Figure 48**).

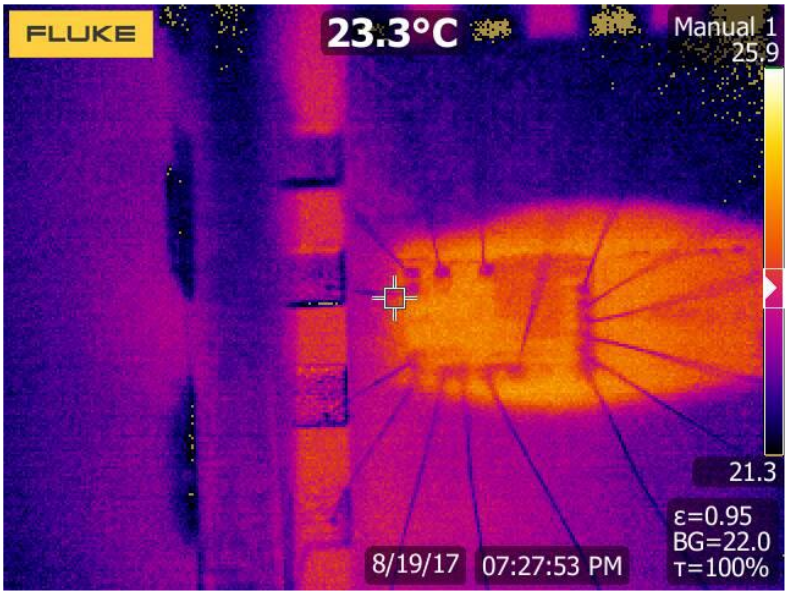

Figure 53. TC974 version 1, thermography experiment, 100 Gy of cumulated TID

After first run (as it is shown in **Figure 53**), a TID of 100 Gy is achieved. The surface temperature of the chip remains stable, at around 25 ºC.

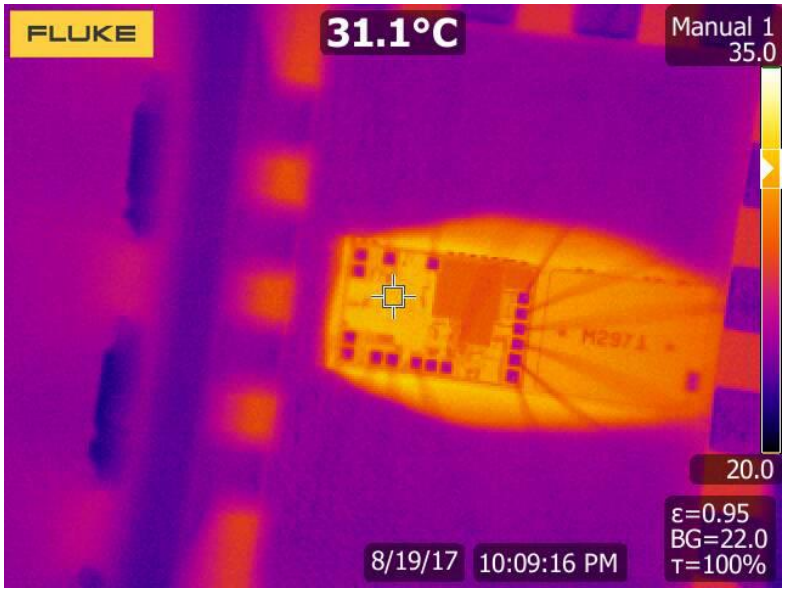

Figure 54. TC974 version 1, thermography experiment, 150 Gy of cumulated TID

When a TID of 150 Gy is achieved, after run 2 (see **Figure 54**), chip temperature slightly increased up to around 30ºC, and digital circuits start to show even a higher increase (around 33ºC).

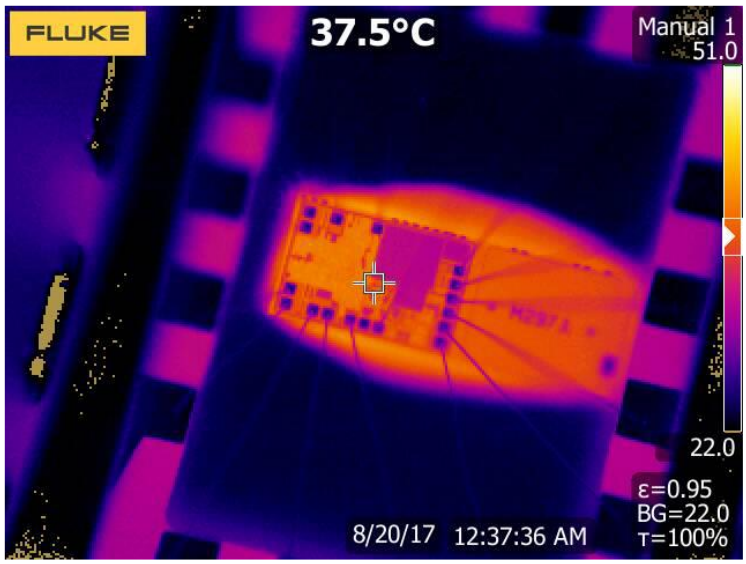

Figure 55. TC974 version 1, thermography experiment, 200 Gy of cumulated TID

As it is shown in **Figure 55**, it is when TID achieves 200 Gy, and digital circuits start to have a larger difference of temperature (45 ºC) compared with other circuits (around 35 ºC).

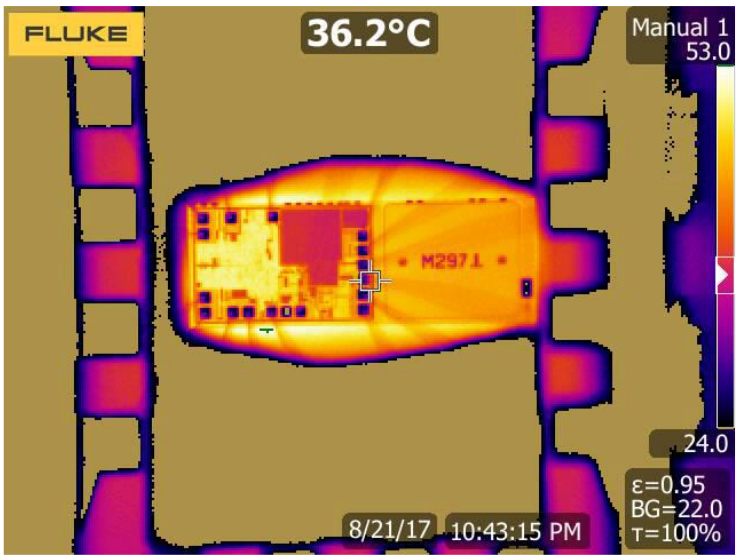

Figure 56. TC974 version 1, thermography experiment, 250 Gy of cumulated TID

Following thermography photos taken at 250 and 300 Gy, in **Figure 56** and **Figure 57**, respectively demonstrated, as digital circuits are the main reason of degradation of the chip, and probably the main source of final failure.

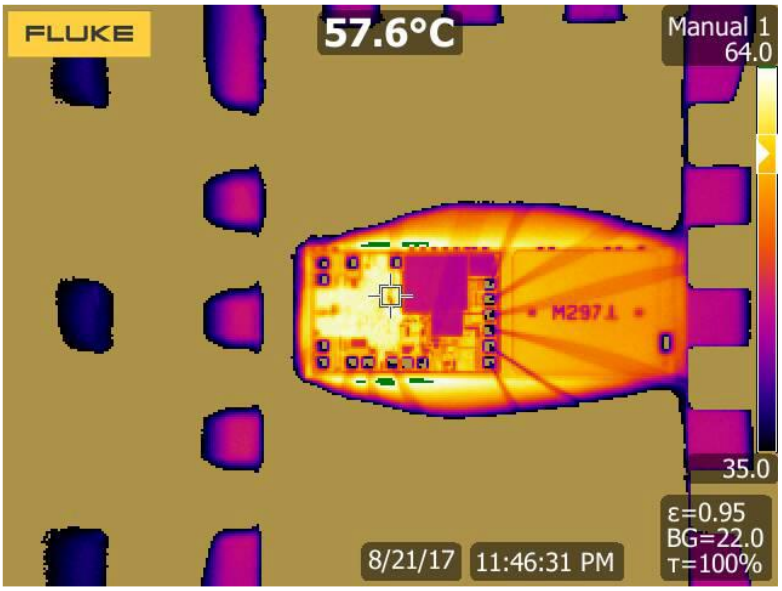

Figure 57. TC974 version 1, thermography experiment, 300 Gy of cumulated TID

The temperature of the chips increased up to 50 ºC and 65 ºC, respectively in last two runs. Clearly, the hottest spot in the chip was localized in the digital circuit zone. While other circuits showed an increase of the temperature (much lower) but probably produced for the very hot spot in the digital circuit that generates a temperature increase in all chip area.

Another experiment carried out on the TC974 version 1, was performed at CHARM facility under a fast-pulsed radiation environment. These measurements were compared with another kind of dosimeter that is in use to calibrate different positions inside the facility, a RadFET device.

The comparison of results between the new FGDOS® and RadFET sensor is one of the most important parts of this work. From these results, it is highlighted whether or not both types of sensor, under the same exact conditions behave in the same way. The results from the irradiation carried out at CHARM are presented in the following and showed in **Figure 58**, **Figure 59** and **Figure 60**. These Figures present the detection profile from the TC974 version 1, and a RadFET, and it is directly given in cumulated dose (in Gy), from a previous calibration carried out on both dosimeters in the CC60 room. The calibration factors were obtained from these calibration

measurements, using a calibrated ionizing chamber in parallel with each kind of sensor. By checking the data from the ionizing chamber and analysing the response of each sensor, can be extracted the calibration factor. From this calibration factor, it is possible to translate from Hertz or Volts to Greys.

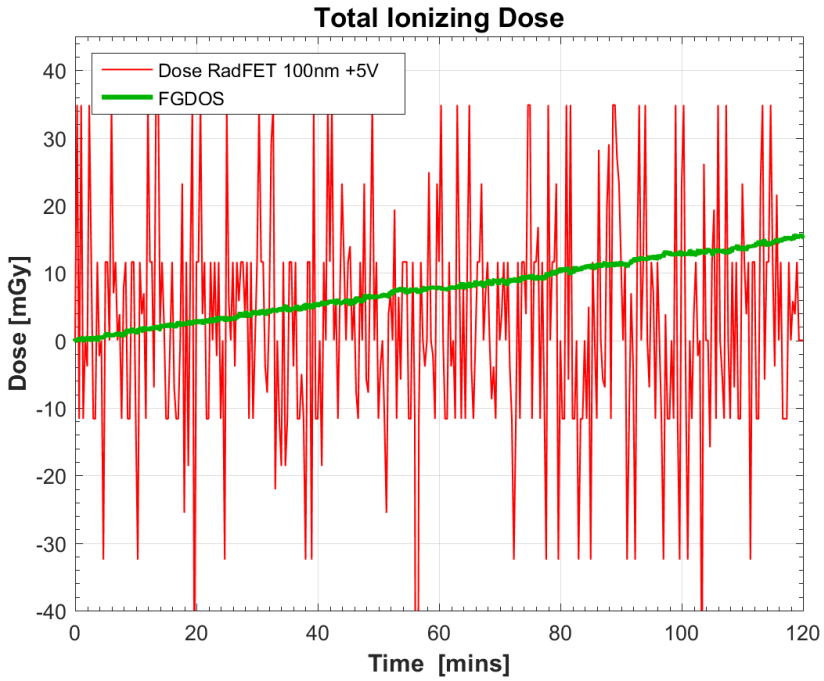

Figure 58. CHARM experiment, beam ON, target OUT, new FGDOS® version and 100 nm RadFET response

Figure 58 details the irradiation detection by both types of sensors when the beam is on and no target is in place. Under this condition, it is noted that the RadFET is not able to detect radiation, as the radiation generated is below its sensitivity and the readout records only noise. On the other hand, the new FGDOS® version is able to detect radiation because of its very high sensitivity and low noise.

In **Figure 59** it can be noticed that the RadFET starts to detect radiation when the target is in place (CuOOOO indicates copper target is in place and all shielding is off). The noise level, which is about ± 50 mGy for the RadFET measuring system, does not permit the measurements from the RadFET when the target is not in place.

Moreover, from this Figure can be seen how new FGDOS® version also detects radiation with the target in place but with a slightly lower sensitivity if compared to the RadFET. This difference comes from the calibration factor used on each type of

dosimeter. The lower sensitivity for the FGDOS® device in comparison to the RadFET comes up from the error obtained when both calibration factors are used. By using ideal calibration factors on both dosimeters the detecting slopes should be the same. This error arises from distinct sources of error coming from the calibration process (distance between the ionizing chamber and the DUT to the source, ionizing chamber measurement error, etc.).

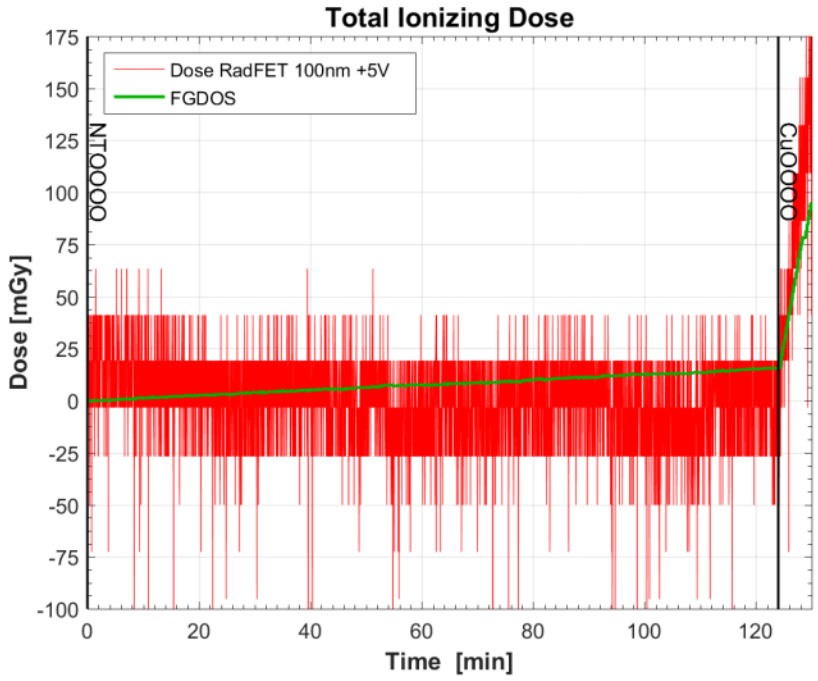

Figure 59. CHARM experiment, beam ON and detail of transition copper target OUT to IN, new FGDOS® version and 100 nm RadFET response

Finally, **Figure 60** presents an enlarged view of the RadFET and new FGDOS® version detection slopes. Regarding to the RadFET signal, the noise from the system is appreciated in the Figure whereas for the new FGDOS® version, it can be seen that the detection slope has small steps every few seconds. The steps are coming from the time structures of the beam that produces the steps in the radiation detected, so called spills. It is the beam profile delivered at CHARM. An accelerator that provides protons at GeV energy generates it. Therefore, the new FGDOS® is able to detect the precise moment when the fast-pulsed mixed field is generated at CHARM.

Nevertheless, the detection response is very similar on both detectors but the signal-to-noise (SNR) ratio response at the output is better for the new FGDOS®.

Thus, it permits the new FGDOS® detect the radiation at CHARM, even when target is not in place (target OUT).

Measurements conducted at CHARM facility report how the new FGDOS® has higher resolution and sensitivity with respect to the RadFET. Two factors have been found very attractive. First, the low output noise and the high sensitivity response (≈ 60 kHz/Gy) which permits the new FGDOS® to reach 150 µGy of resolution (compared to the 150 mGy in the RadFET). Second, the higher resolution, which allow detecting the profile of the beam (when target is in place) to be monitored.

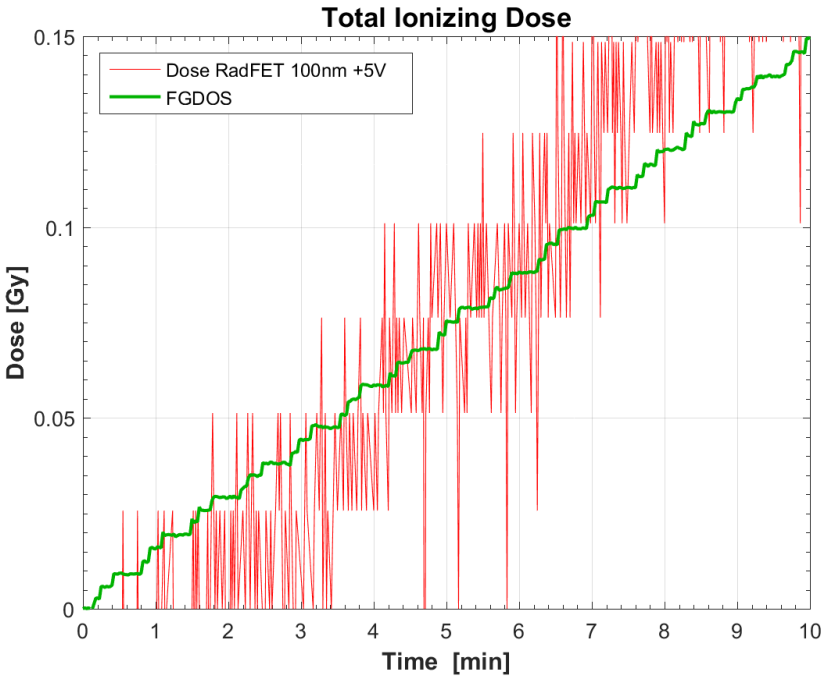

Figure 60. CHARM experiment, beam ON and target IN, new FGDOS® version and 100 nm RadFET, detail on spills detection

New FGDOS® version performed well for one week inside CHARM, without any single SEE detected, and detecting the TID generated from the cocktail of particles generated.

From those results above on the TC974 version 1 and other TC presented earlier in this chapter, TC974 version 2 design was performed trying to include all new features and design improvements to overcome all problems detected in previous versions and TCs. Once TC974 version 2 was fabricated, a TID lifetime experiment

was carried out. A single sample was exposed to gamma radiation (60-Co source), in CC60 room at a dose rate of 6.12 Gy/h.

In **Figure 61**, it is presented the complete run conducted. Spikes observed were produced for changes in the configuration done during the radiation, just for few minutes. These changes of configuration were carried out in order to check if the sensor was still working in terms of changing configurations. The sensor lasted more than 800 Gy keeping all its functionality. It means more than three times than previous FGDOS® version (≈ 250 Gy). At around 805 Gy, the sensor start to fail. First, not recharging when sensor output exceed the threshold value, and finally with a general failure, retrieving directly zeros at the output.

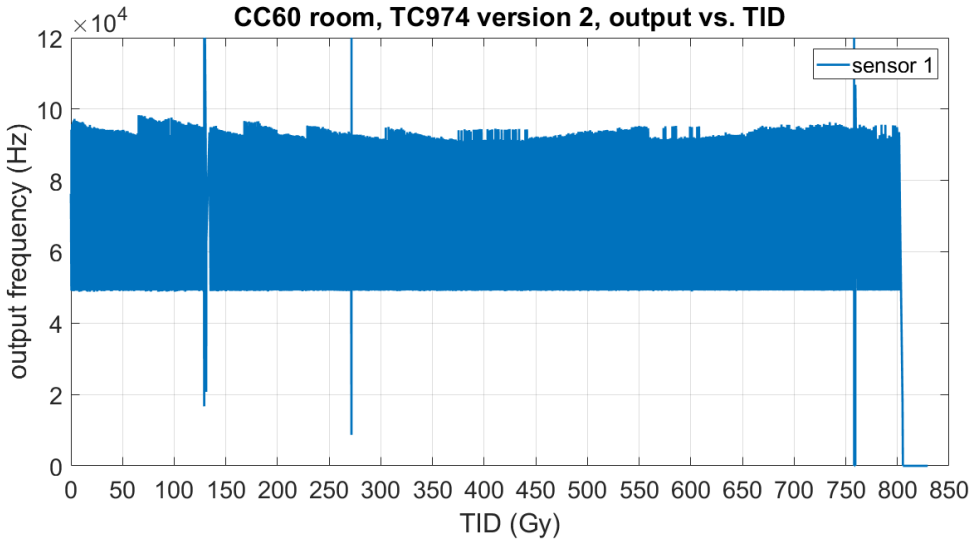

Figure 61. TC974 version 2, TID lifetime experiment, output frequency

One of the aspects to be tested was the performance of the recharge process during the TID lifetime test. From this point of view, the recharging process showed a much better performance than TC974 version 1.

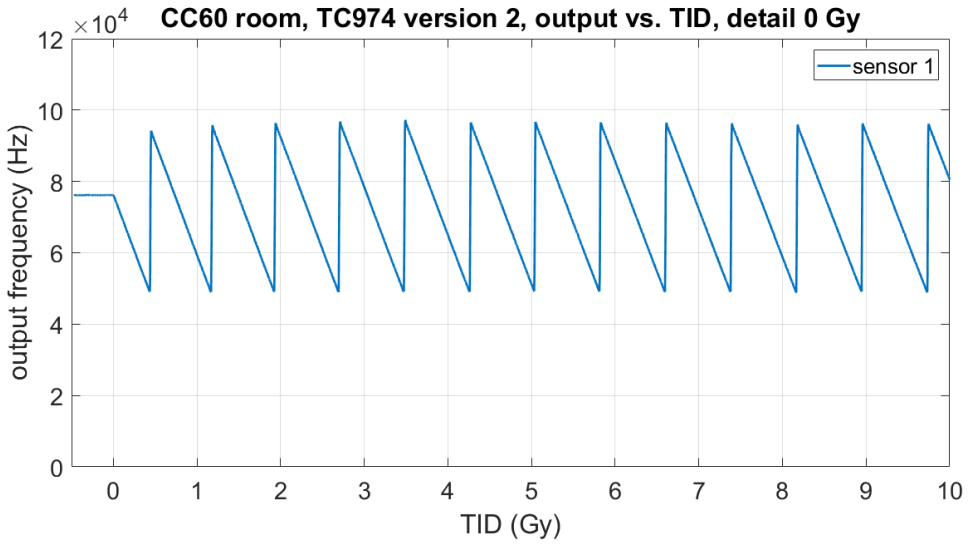

Figure 62. TC974 version 2, TID lifetime experiment detail, when 0 Gy were cumulated

This time, the recharge process was carried always within 2 to 5 samples (every 2 to 5 seconds, because during recharge the sensor output was sampled every second). As it is observed in **Figure 62** and **Figure 63**, recharge process was fast enough, in both, at the beginning and at the end of the TID lifetime experiment.

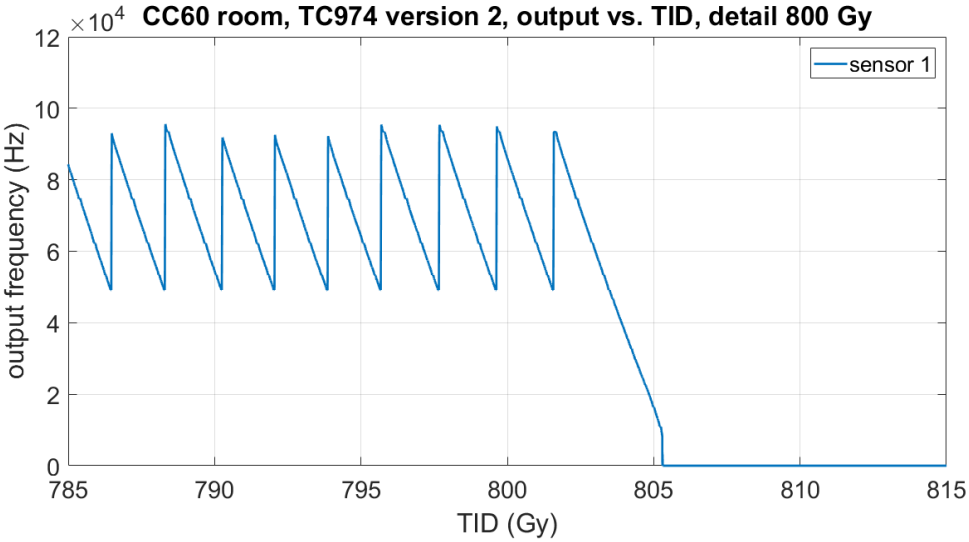

Figure 63. TC974 version 2, TID lifetime experiment detail, when 800 Gy were cumulated

Another important characteristic to be observed during the TID lifetime experiment was the sensitivity of the sensor along the experiment. In previous studies, was possible to monitor this effect [47]. Then in this test was important to analyse it and if a drastic loss of sensitivity from the sensor had been occurred. **Figure 64** presents the sensitivity variation when the sensor was exposed to TID.

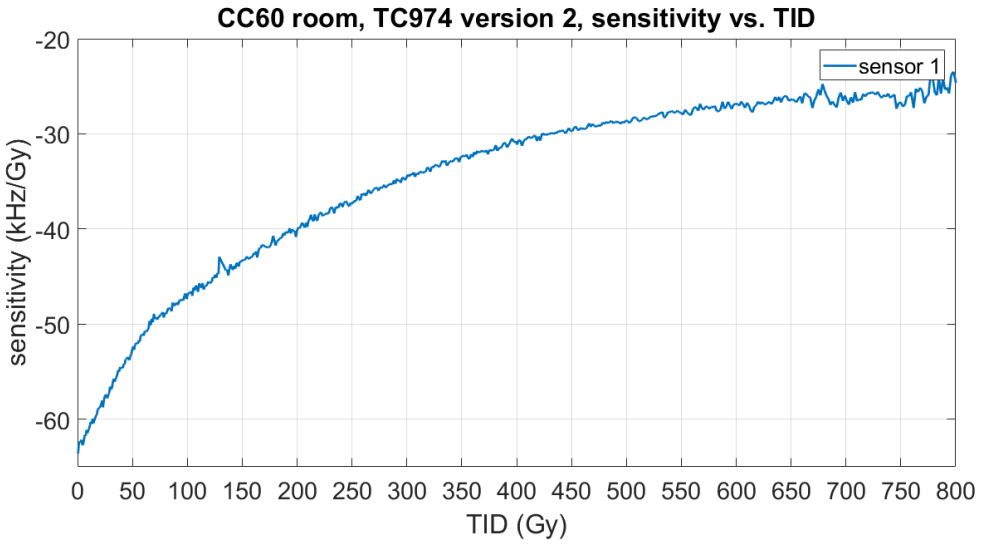

Figure 64. TC974 version 2, TID lifetime experiment, new FGDOS® sensitivity

The sensitivity at the beginning was around 63,61 kHz/Gy and at the end, 25,76 kHz/Gy, what signifies a 60 % loss of sensitivity. This effect was already described at [47]. Even so, the lowest sensitivity registered, is similar to the one from previous FGDOS® version.

TC974 version 2, even with all circuitry designed using RHBD techniques, exhibited an increase of the current consumption from 4 mA, up to 65 mA, when the sensor failed. Unfortunately, the current consumption was not logged during the experiment; thence it could not be plotted. However, the current consumption rise, takes associated an increase of the temperature in the chip. Thus, as the FGDOS® has a temperature sensor embedded on chip, it can be plotted (see **Figure 65**), and it can be foreseen how the TID effect damage is affecting the circuits on-chip.

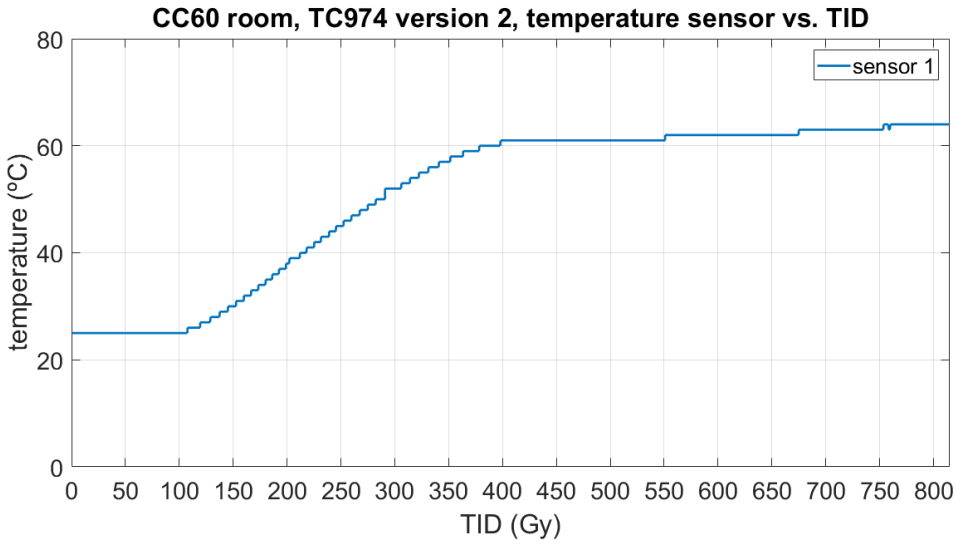

Figure 65. TC974 version 2, TID lifetime experiment, new FGDOS® temperature sensor

The effect associated to this rise in the current consumption it is expected to be the V_{th} shift on the n-MOS transistors from digital circuits. As digital circuitry implements hundreds of n-MOS transistors, even, few microamperes from each device, in total, implies an increase of the consumption of tens of mill amperes. Moreover, in some tests carried out in single n-MOS devices, with minimum size, demonstrated to be very sensitive to TID, from 100 Gy, with a sudden shift in the V_{th} of the transistor. In addition, a recover of the effect if TID is not applied after, is expected, due to annealing, and V_{th} shift recover. This must be investigated in future experiments.

In summary, TC974 demonstrated to be a big step ahead with respect to previous FGDOS® version. All extra functionalities and improvements in its sensitivity (≈ 60 kHz/Gy) and TID lifetime (≈ 800 Gy), made it a better dosimeter. Effects as the current consumption rise and loss of sensitivity must be further investigated and improved in future versions.

4.5.8. TC993, ESD radhard

The design of TC993 came up after data collected on TC971 radiation tests. ESD protections in these tests had become the main suspect of the current increase above 500 Gy when the ESD protection was in worse polarization case, i.e. +5 V. Thus, as

ESD protection structures are affected by TID effects [67, 68], it was of main interest to investigate them.

TC993 embedded radiation tolerant (proposed) and standard ESD structures. In addition, to validate the ESD protections supposed to be radiation tolerant, a complete input to output digital circuit had been included two times. One time used with standard ESD protections and the other with ESD protections radiation tolerant in order to compare. This way, it could be verified that a common circuit connected to pin with ESD protections, did not penalize the normal circuit functionality.

As it is shown in **Figure 66**, TC993 design has two times the same circuit but one time is using standard ESD protections and the other time radiation tolerant ESD protections.

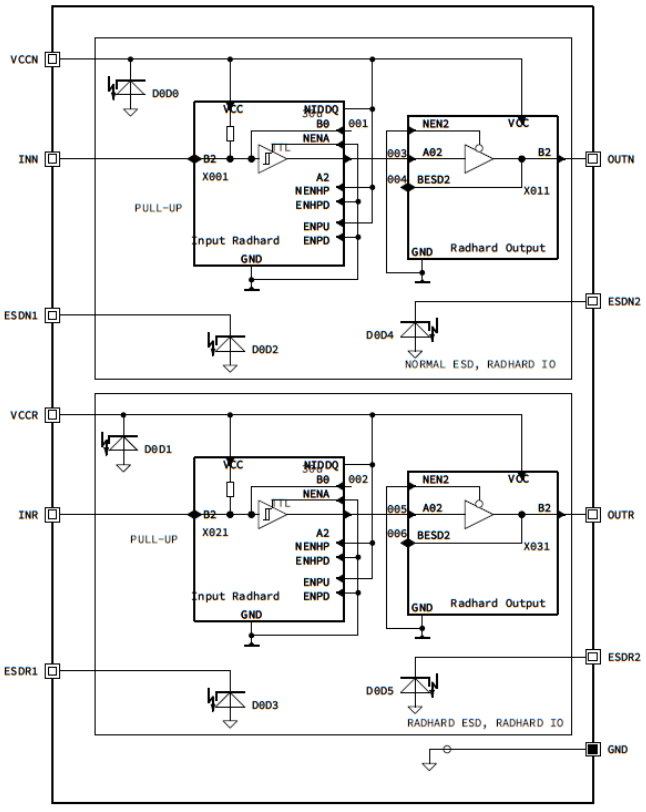

Figure 66. TC993 schematic

The standard ESD protection apart of the protection diode includes snapback protection functionality, and owing to this, it is not a structure radiation tolerant by design. New ESD protections proposed and designed in TC993 to withstand ionizing

radiation deleted the snapback and kept the protection diode. Thus, they should be radiation tolerant at least up to 1 kGy (TID goal of new FGDOS®).

The test was carried out at CC60 room in a position receiving a dose rate of 10 Gy/h. During the test a function generator was used to generate a 10 MHz square signal at both digital (INN and INR pins). Moreover, a four channels power supply was used to provide +5 V to all four lines, VCCN and VCCR power supplies of input/output digital circuits, and ESDN1 and ESDR1, standard and radiation tolerant ESD protections respectively. In addition, ESDN2 and ESDR2 were set to ground during the experiment. The measuring setup used can be seen in **Figure 67**.

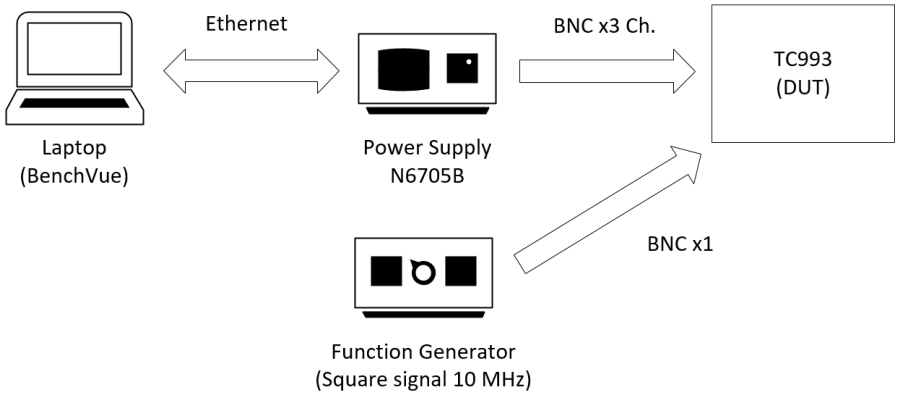

Figure 67. TC993 radiation test setup diagram

Data from all four channels of the power supply were logged via a computer using the BenchVue software.

The results obtained were used to validate the new ESD protections design. As it is shown in **Figure 68**, new ESD protections showed a good tolerance to ionizing radiation up to more than 1.3 kGy of TID.

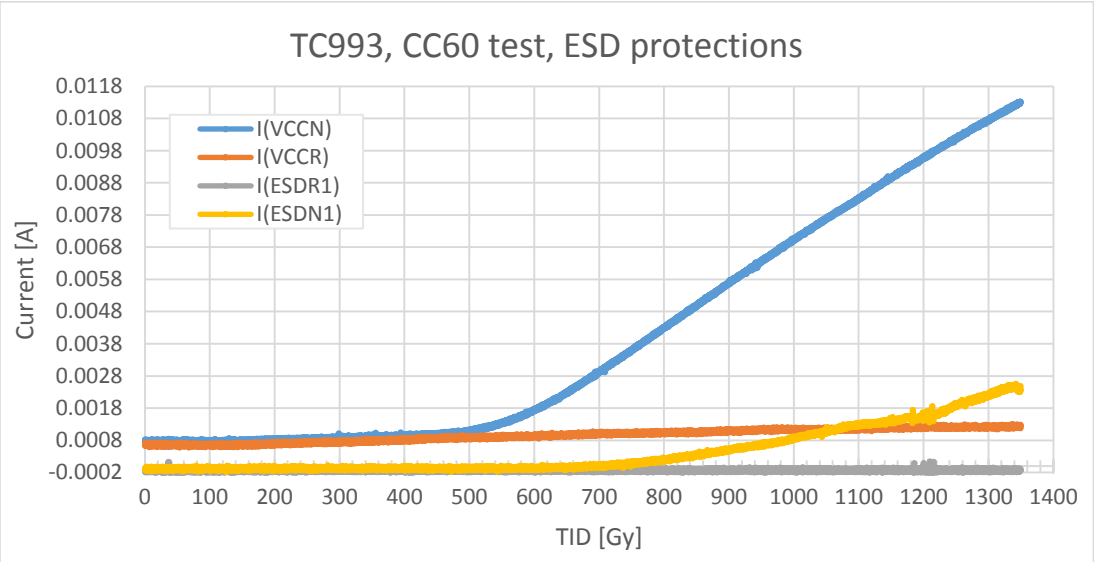

Figure 68. ESD protections current consumption when exposed to TID

Both channels from the power supply where standard ESD protections were connected (I(VCCN) and I(ESDN1)) had an increase of the current consumption above 500 Gy. I(VCCN) as was supplying the input to output digital circuit had a higher current consumption since the beginning (around 800 µA) when fed with a 10 MHz square signal at the input. In addition, the current slope increase was double compared with I(ESDN1) because in I(VCCN) channel two standard ESD protections were connected. One for VCCN and the other at OUTN pin, as an output, the power supply of the output driver comes also from VCCN pin.

In the other side, both channels with radiation tolerant ESD protection designs (I(VCCR) and I(ESDR1)) proved to be tolerant to ionizing radiation up to 1.3 kGy. The current consumption in the case of the single ESD protection (I(ESDR1)) was zero up to the end of the experiment. Instead, for the input to output circuitry, a linear increment of the current consumption was observed due to the V_{th} shift of the n-MOS transistors (≈ 500 µA current increase). This effect as observed in previous tests (e.g. in TC971 tests) started at 100 Gy of TID. The design of the input to output circuit includes some active pull-ups and pull-downs and current mirrors, therefore an increase of the current was measured.

Finally, when radiation stopped measurements on both input to output digital circuits were conducted at OUTN and OUTR pins. Only OUTR pin was switching at 10 MHz due to the input 10 MHz square signal coming from the function generator.

In addition, current measurements on I(ESDR2) and I(ESDN2) were carried out and no current conduction was measured up to +5 V polarization. This effect could be explained because both devices were not polarized during the radiation, thus the charge trapped generated in the field oxide was much lower than the ESD protections in worse polarization condition (+5 V) during the radiation test.

4.6. Summary

The new FGDOS® version design and conception has been a long process. In this chapter all different test structures, and test carried out have been presented and discussed. From all these test structures, many fruitful results have been obtained. Thanks to all of them, the new and current version of the FGDOS® have been possible. Nevertheless, many drawbacks and time constraints came out as the project progressed.

In order to improve even more the current design, more tests should be carried out, and some of them are already on the way. More tests regarding simple n-MOS transistor structures, to better understand the V_{th} shift, or another thermography test on the TC974 version 2 chip, or radiation tests in this version, at CHARM, or under heavy ions would make this thesis a better work and it will be keep as future work to be done.

In addition, the access to silicon deliveries (tape outs) very limited, usually once a year, did the development process more complex, due to time constraints between tests, results and new designs. Usually, half the time was dedicated to new FGDOS® version and TCs design, and the other half of the year to test, and obtaining results, for next versions design.

Despite all this, most of the TID effects regarding the technology used in the FGDOS® were understood in different kind of devices (MOS transistors, bipolars and ESD protections). Thus, it can be said that the FGDOS® cannot be 100 % immune to TID due to V_{th} shift in n-MOS transistors. However, other techniques and design methodologies can be experimented, in order to improve against its TID response (different n-MOS transistors sizes, disconnecting circuits when not used, etc.). Moreover, other technologies to implement FGDOS® should be tested. In concrete, technologies with smaller gate oxide thicknesses. By doing this, a priori V_{th} shift in

MOS devices should be a negligible effect (Nonetheless, other effects will arise, i.e. SEE).

As relevant RHBD techniques used, can be mentioned enclosed MOS transistors, guard rings between devices and avoid n-MOS transistors in the design. Bipolar devices and ESD protections equally have been designed using similar RHBD techniques.

FGDOS® fabrication technology showed a very good performance against SEE. No SEE have been appreciated during CHARM campaigns, where the very harsh environment is composed with particles that can generate SEE. As discussed earlier in this section, SEE should be considered if smaller gate oxides technologies are used for future FGDOS® versions design. Probably, it will become the predominant radiation effect to take into account.

Chapter 5. High Speed Floating Gate Dosimeter

This chapter presents a characterization study of a High-Speed Floating Gate based dosimeter system (Floating Gate TransImpedance Amplifier, FGTIA). Two chip prototypes compose the system: one embeds basic floating gate structures and the other is a multipurpose chip with configurable transimpedance amplifiers. The system allows improving two key measurements with respect to other floating gate based dosimeters, by measuring the discharge on the floating gate in real-time and high speed, and by providing an amplified signal out of the floating gate. In addition, the sensor includes a replica structure of the floating gate circuitry without the sensing capacitor, and thus, this can be used to compensate the effects of the temperature. Results are first presented on simulations and measurements without radiation to get an overview of the system performance. Later radiation measurements under two different sources are presented. Radiation characterization is carried out under a 60-Co source and finally measurements on a beam profile in a mixed-field environment are included to validate the measurements and simulations under different radiation conditions.

5.1. Working Principle

The FGDOS® highlighted to be a good candidate [1, 3, 4 and 8] for much different kind of applications. Nevertheless, the response of the FG sensor was converted to frequency and this lowered the dosimeter performance for fast-pulsed radiation environments [30, 69, 70 and 71].

The measurements of a radiation profile is a continuous requirement in accelerators driven facilities [72]. This chapter presents a new FG based dosimeter system that overcome some of the drawbacks of previous FGDOS® and more precisely improve the response under pulsed radiation conditions. The main objective of this new proposed system is its capability to be used in this application field, that is, in accelerators driven facilities.

The radiation generated in accelerators like those at CERN [30, 69] produces a characteristic radiation profile. The radiation intensity profile at each pulse is not constant along the time. Thus if the measurement of the exact profile and its time dependence can be carried out, then the radiation levels delivered during the experiments can be detected and measured with accuracy. The radiation dosimeter system presented in this work would be able to detect such a profiles and then extract a precise measurement of the radiation delivered during the spills generation.

The study starts with the characterization of the system under different configurations and working modes –which will be detailed later in this chapter- to foresee which is the best configuration to be used under real conditions of radiation. After this, measurements will be carried out under gamma source first and mixed field environment [31] later to validate the simulations and previous characterization measurements.

The system working principles consists of three stages as it is shown in **Figure 69**. Stage 1 is the FG sensor embedded inside the first chip, it is composed by the FG capacitor plus the reading MOS. This stage delivers a current proportional to the charge stored in the FG. When radiation is applied the pre-stored charge starts to be removed from the FG leading to a variation of the output current in the reading MOS. Moreover, Stage 1 has a replica reading MOS where its V_{GS} can be externally controlled (V_{GD}), to be used as a reference and polarized to the FG voltage as initial condition. Stage 2 is composed by the input adaptation front-end of the second chip and the TransImpedance Amplifier (TIA) [73]. This second stage is in charge of adapting the input by using cascode transistors and transforming from current to voltage and amplifying through the TIA circuit. This is done separately for each input, the one coming from the FG structure and the one from the replica structure. Stage 3 is the output from the second chip, and it is in charge of making the operations of addition (V_1+V_2) and subtraction (V_1-V_2) between the pair of inputs received from the first chip. This function is implemented by an iC-Malaga's chip developed for encoder positioning applications and reused here in the FGTIA system.

A voltage value proportional to the difference of currents between the FG and replica structures is given as a resulting output of the FG based dosimeter system. It makes the system very fast on response when radiation is applied. The only latency is the one coming from the two chips circuitry response, it means in the order of

microsecond. By using this system, it is expected to detect radiation pulses of few millisecond. In addition, as the measurement is carried out from two different channels (the FG and the replica) with a very similar polarization point, the temperature effects coming from the reading MOS are compensated.

The dosimeter system consists in two different chips, one with the sensing circuitry and another with the readout circuitry. As it is shown in **Figure 69**, the system interconnection allows up to two sensors working in parallel independently. Each one with its replica and its FG sensor.

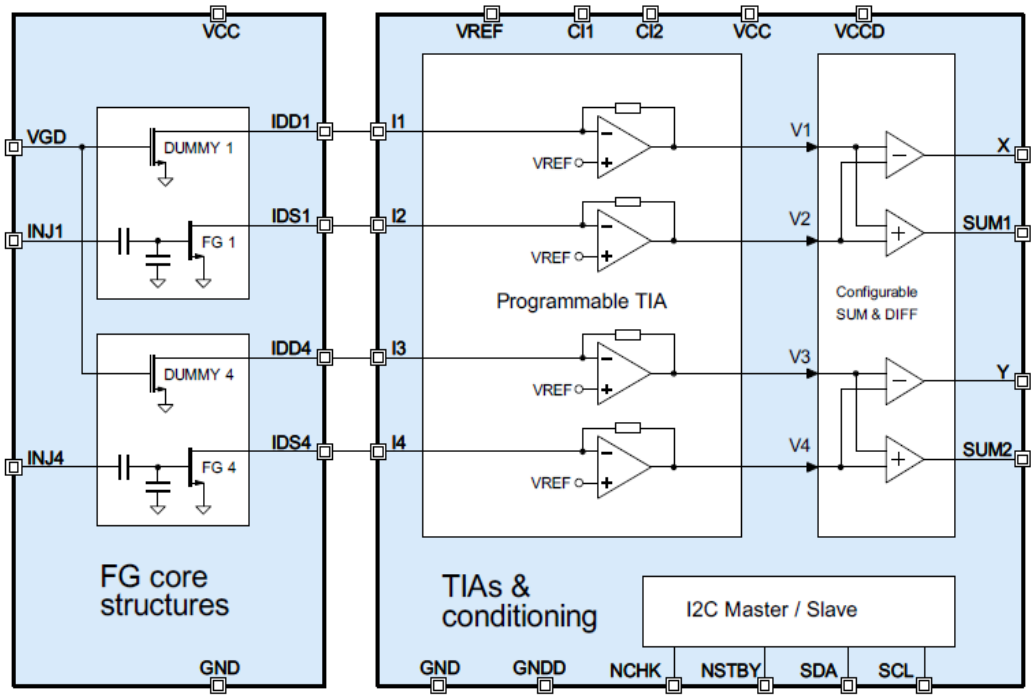

Figure 69. FGTIA system, block diagram

The sensing circuitry embedded in the first chip is composed of different FG basic structures (FG capacitor and reading MOS) and includes a replica reading MOS (the so-called dummy structure), for each of the FG basic structures.

The second chip is in charge of the amplification, and operation of the inputs coming from the sensing chip. This second chip is composed of the programmable TIAs (the amplification is configurable), the selectable addition and subtraction operations in pairs, and finally includes an inter-integrated circuit (I^2C) serial interface which permits the chip configuration.

In **Figure 69**, it can be seen two FG systems working at once. Here we will describe only one, the system with VGD, INJ1, IDD1, IDS1, X and SUM1 as input and outputs, working with channel 1 and 2 (replica and FG channels respectively).

First of all the FG sensor must be charged by injecting charge on it. To make it in a precise way, we set 1.5V at VGD pin, and we start the injection using INJ1 pin. When both the FG and replica channels are in the same polarization point, giving the same amount of current at the TIAs inputs (I1 and I2), then the output (X) must be set exactly at the TIA's reference value because the subtraction of both channels is zero (V_1-V_2).

Once the system is charged and equilibrated, then every discharge in the FG side will generate a difference between the FG and the replica channels and this change will be amplified (depending on the TIA gain setting) at X output.

Finally, when radiation generates a difference large enough to reach the saturation region where the output cannot follow the difference between both channels, a recharge by using the injector (pin INJ1) must be triggered until the system is equilibrated again to the reference voltage.

The readout given in the FG based dosimeter system consists on measuring a voltage variation at pin X (V_X), proportional to the FG discharge. In order to carry out this measurement a precision digital multimeter or a data acquisition system (DAQ) are used externally.

5.2. Test Setup

The setup used to carry out the measurements is composed of; the chip with the FG structures, the chip with the TIAs and readout stage and the board including both chips. The FG and replica structures were embedded in the TC994. This TC is a dedicated chip embedding four FG and replica structures. In this chapter, results from only one structure are presented. The structure used is similar to previous FGDOS® version because the aim of these measurements is to evaluate the reliability of the system in pulsed radiation environments.

In the other side, the TIA's chip is the TE162, a multipurpose and multiapplication chip prototype, designed at iC-Malaga and reused in this application. Its four channels connected in pairs are perfect to be used straight forward in this application.

The configuration set introduced in the whole system is described in this section. The main parameters configured are the TIA gain, the V_{DS}, V_{GS} polarizations from the sensing and replica parts and the TIA's reference and input adaptation. Because of that, two main system configurations have been considered:

- Configuration 1: This configuration sets a similar polarization of the one used by the previous FGDOS systems [4, 8] It means, V_{GS} = 1.5 V and V_{DS} = 0.5 V with an external 0.5 V reference.
- Configuration 2: This configuration uses the best settings for the TIA. It means. V_{GS} = 1.5 V and V_{DS} = 0.7 V given by input cascodes of the second chip with an internal 2.5 V reference in order to enlarge the output dynamic range.

Table 11. Proposed FGTIA configurations

Configurations	TIA Reference	Input Cascode
1	External, 0.5 V	Disabled
2	Internal, 2.5 V	Enabled

The gain of the TIAs is also set in principle to the maximum, but it is one of the parameters to be analysed in the results section because depending on the radiation environment and type of application it would be interesting more or less gain.

The board is supplied with +5 V. Moreover, the +0.5 V external reference and +1.5 V to VGD pin which is used as the replica reference must be provided as well. Only channels 1 and 2 are used and measured.

The measurement procedure under radiation applied consists in charging the FG up to the equilibrium point of the system for a given V_{GD} of 1.5 V. When radiation is applied then the discharge of the FG has to provide a variation at X output pin due to the disequilibrium between replica and FG channels.

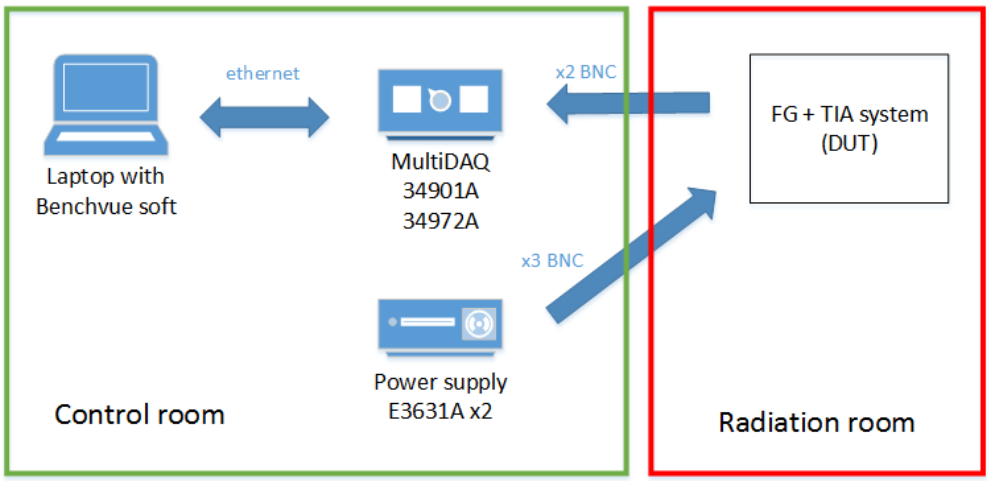

Figure 70. FGTIA CC60 radiation test setup diagram

The test setup at CC60 room is composed by the board and chips already described, three channels from a power supply (to provide VGD, VCC and INJ1 voltages), two channels from a multiDAQ, to measure X and SUM1 pins and the laptop to control the instruments and data logging. The multiDAQ measuring system can be used at CC60 room tests because the output variation will be slow, and able to be measured by the measuring system.

Instead, the test setup at CHARM needed as measuring system an oscilloscope (due to fast-pulsed radiation environment, this way it can be measured with accuracy enough), and data is logged from it directly. All the other components and equipment used at CHARM were the same than used during CC60 tests.

5.3. Test Results

Regarding the characterizations, simulations and measurements under radiation of the FGTIA system, their results are presented and discussed in this section. Firstly, the two configurations proposed previously have been analysed. Afterwards on one of them, a more detailed characterization changing different parameters is discussed. In addition, some simulation results are presented, and then radiation characterization measurements (at CC60 room at CERN) are introduced to finally present measurements in a pulsed mixed field radiation environment (CHARM test area at CERN). These results confirm that milliseconds spills can be measured by the system proposed in this chapter.

In **Figure 71** and **Figure 72** it can be seen the performance for both configurations.

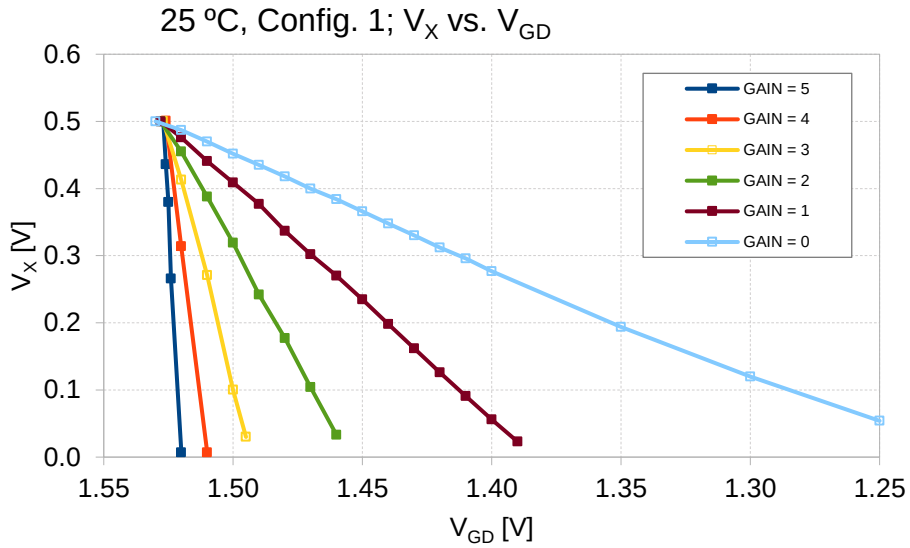

Figure 71. Measurements using Configuration 1 for different gain settings

The small output dynamic range owing to the low voltage reference (0.5 V) limits the performance when the system is in Configuration 1. By using this configuration, the system is limited in terms of gain amplitude, because higher gains saturate the output for few millivolt of variation in the FG (in the figure above V_{GD}). In addition, when the reference is in the lower side of the output full range of the system, the mismatch between the replica and the FG channels is wider due to different polarization conditions. It occur when real radiation is applied and the X output will move towards larger voltage values.

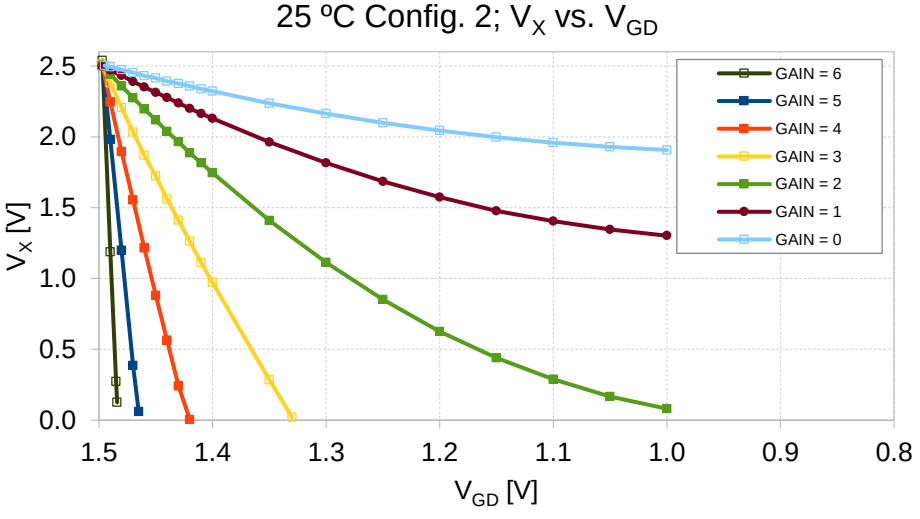

Figure 72. Measurements using Configuration 2 for different gain settings

Configuration 2 permits wider dynamic output range because the reference is set to 2.5 V. Moreover, in this case the reference is generated on-chip, so there is no need of an external voltage reference, which makes the system easier to implement saving one voltage reference. In addition, using Configuration 2 where the reference is centered in the middle of the dynamic output range, difference between replica and FG polarization voltages will be the minimum, even when real radiation impacts the system, where X output will move towards voltages that are more positive. Those are the reasons why Configuration 2 is used in the full characterization procedure.

Figure 73 to **Figure 75** show different gain configurations characterized under distinct temperatures.

When the system is configured with gain 6, it multiplies the output with respect to the V_{GD} variation up to 188.1. In addition, two effects are observed in all gain configurations with the temperature characterization.

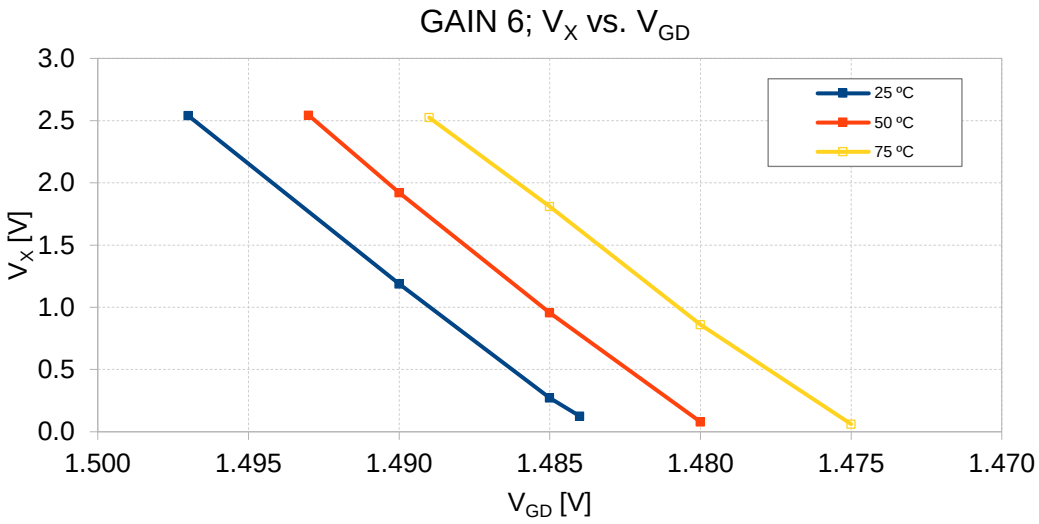

Figure 73. Temperature measurements using Configuration 2 for gain 6

First, for different temperatures the FG shifts its voltage for the same amount of charge stored on it (from 1.497 V to 1.489 V). It means, the FG itself has a temperature coefficient, it is shown in **Table 12**. Secondly, the gain has a temperature dependence in the range of -0.2 %/ºC to -0.3 %/ºC.

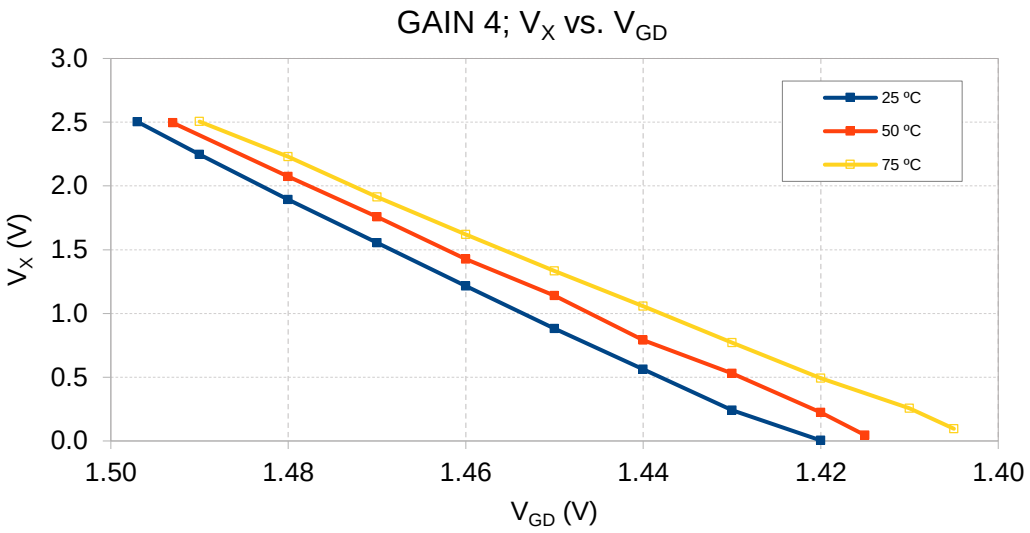

Figure 74. Temperature measurements using Configuration 2 for gain 4

Figure 74 and **Figure 75** show how the range of discharge allowed in V_{GD} is wider with respect to Configuration 1 before the system output saturates. By configuring gain 6, the V_{GD} range is 13 mV, using gain 4 is 77 mV and gain 0 does not saturates within the range between 1.5 V and 1 V at V_{GD}.

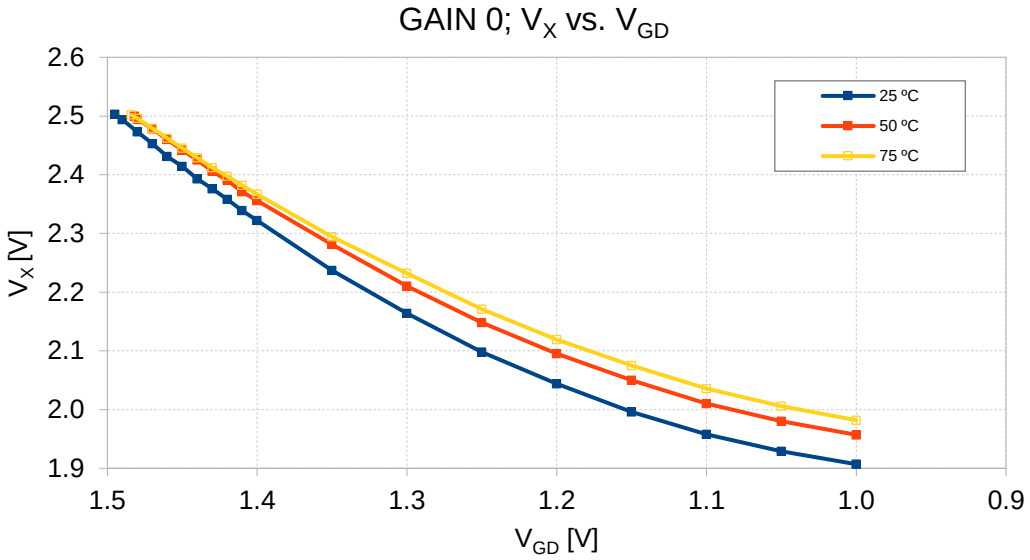

Figure 75. Temperature measurements using Configuration 2 for gain 0

The V_{GD} dynamic range to keep the system inside a linear response must be between 1.5 V and 1.4 V, in **Figure 75** it is appreciated how wider ranges start to make the system response non-linear due to the reading MOS polarization.

Table 12. Measured and simulated gains and temperature coefficient

Configured Gain	Simulated Gain at 25 ºC	Measured Gain at 25 ºC	Temperature Coefficient [ppm/ºC]
0	2.4	1.9	-220
4	31.8	31.6	-140
6	135.0	188.1	-160

Simulations were carried out (by using the analog circuits simulator from iC-Malaga) trying to foresee the expected behaviour of the system when the reference varies as it was done above during the pre-irradiation characterizations. **Figure 76** shows how the system should perform under these conditions, considering 1 mV variation per step in the V_{GD} pin, Configuration 2 and gain set to 5.

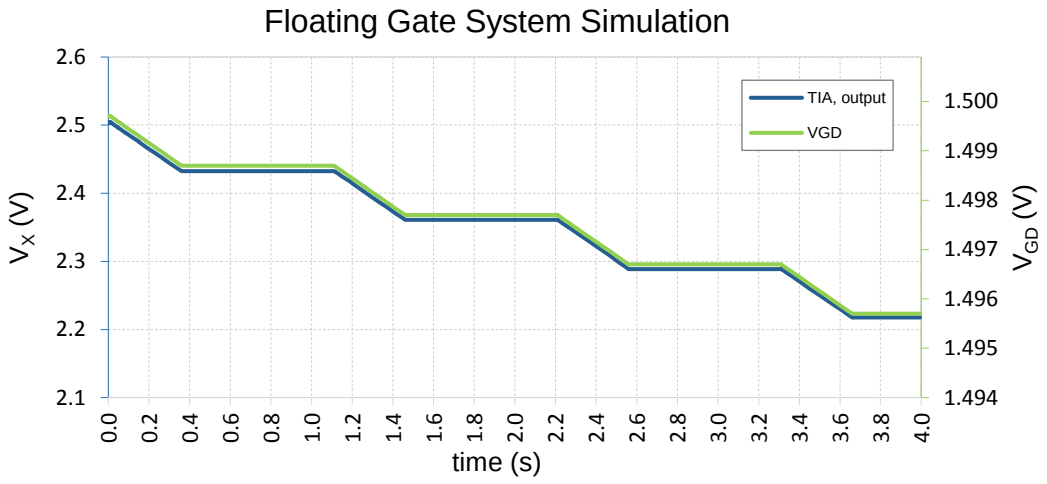

Figure 76. FGTIA system simulation, when reference varies, 1 mV variation per step, system with Configuration 2, gain 5

Once pre-characterizations and simulations were carried out, tests campaigns under radiation were conducted. Firstly, a characterization of the system under a 60-Co source at CC60 facility from CERN is presented and discussed. Then at last, beam profile measurements and simulations are presented and discussed for different positions at CHARM facility from CERN.

Figure 77 shows the response of the system for different gain configurations at CC60 facility when irradiated at 2.21 Gy/h. This permits to see the TID response of the system after few mGy accumulated.

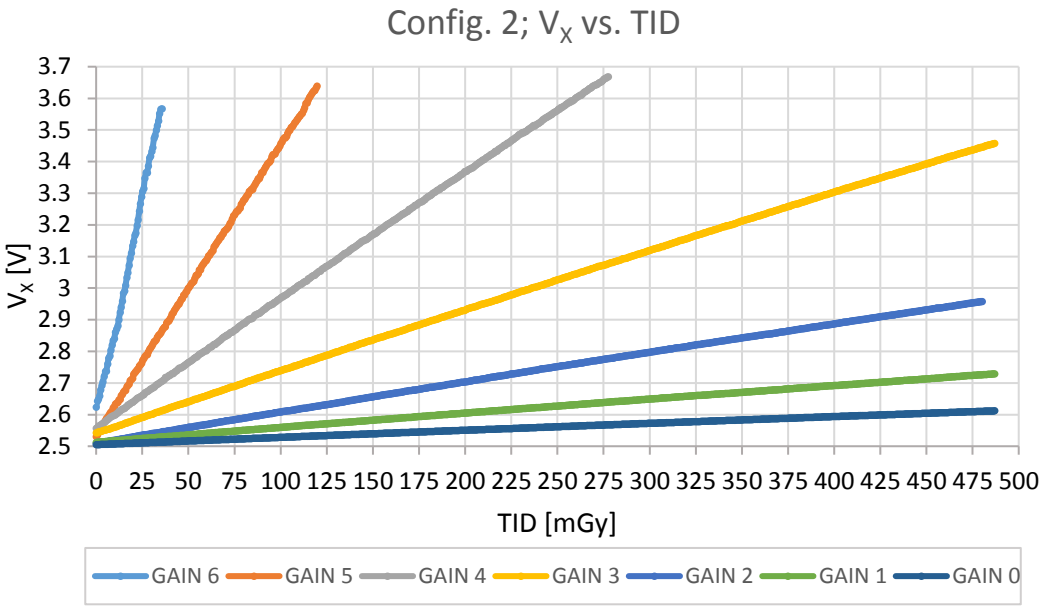

Figure 77. FGTIA system calibration using a 60-Co source for different gain configurations

The plots for different gains in **Figure 77** show the linearity of the system when exposed to TID. The dynamic range of the system varies considerably depending on the gain configuration. Obtained sensitivities (S, V/Gy) at X output are the expected for each gain configuration, compared with pre-characterization and simulations. Nevertheless, the noise of the system was larger than expected, probably due to long cables connections inherent in the test bench. Thus, the minimum detectable dose (MDD) for each gain was larger than expected, in the order of mGy.

Table *13* summarizes all parameters extracted from calibration measurements conducted in CC60 room.

Table 13. Results summary of CC60 room radiation campaign

Gain [n]	Noise [mV]	MDD [mGy]	S [V/Gy]
6	34.38	1.28	23.34
5	24.24	2.65	9.14
4	10.97	2.53	4.33
3	5.37	2.55	2.09
2	2.01	1.93	1.04
1	1.41	2.79	0.51
0	0.58	2.32	0.25

Once the calibration of the system had been carried out at CC60 room, measurements of a beam profile at CHARM facility were conducted.

CHARM facility as it is shown in **Figure 78**, receives a proton beam at 24 GeV/c from the Proton Synchrotron (PS) accelerator. Each spill coming from the beam impinges a copper target and generates a mixed field environment.

At CHARM, two different positions were tested. Position G0* (it has no calibration measurements per spill), next to G0 position and with a very low dose per spill, and R16 position, where the experiment is placed in an overhead conveyor and where more radiation per spill is expected than in G0* (as it is shown in **Table 14**).

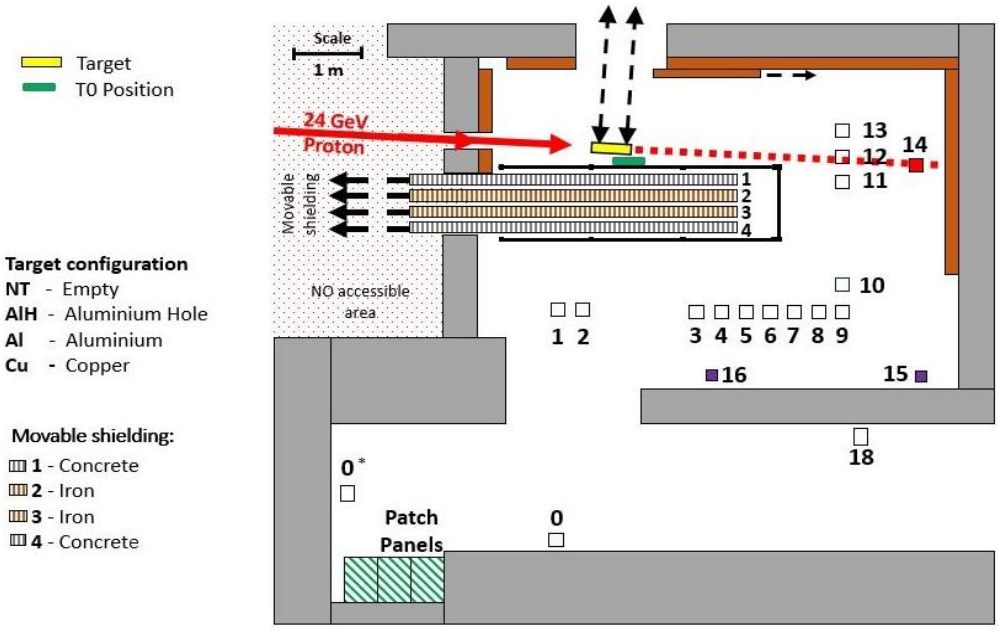

Figure 78. CHARM facility top view diagram with G0 (0), G0* (0*) and R16 (16) positions

Table 14 summarizes the expected radiation delivered per spill depending on CHARM positions.

Table 14. Radiation profile at different CHARM positions

Position	Min. dose per spill [mGy/spill]	Max. dose per spill [mGy/spill]
G0	0.63 ± 23%	1.05 ± 23%
R1	3.60 ± 23%	6.00 ± 23%
R10	7.23 ± 23%	12.10 ± 23%
R13	9.00 ± 23%	15.00 ± 23%
R16	2.30 ± 23%	3.83 ± 23%

In addition, simulations were carried out trying to foresee the expected behaviour of the system under fast-pulsed radiation in a mixed field environment with spills coming from the accelerator at CHARM [30]. **Figure 79** shows how the system should

perform under this fast-pulsed environment, considering 1 mV discharge per spill in the FG, Configuration 2 and gain set to 5.

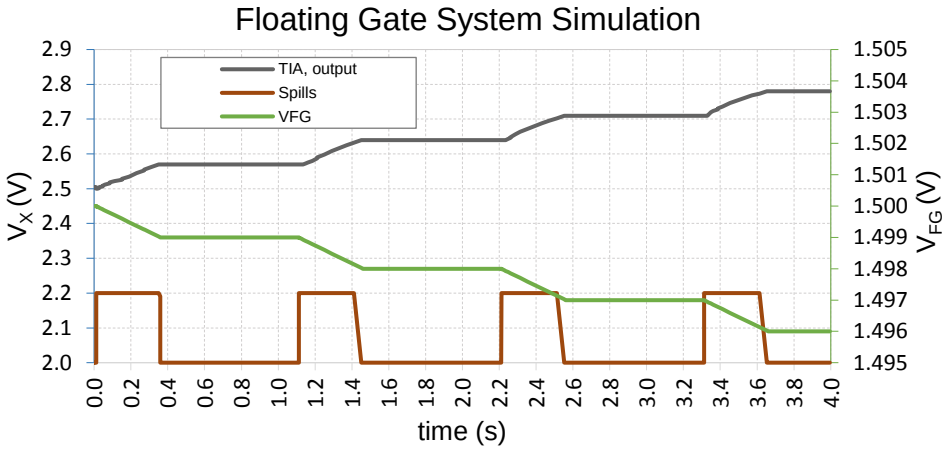

Figure 79. FGTIA system simulation, when spills are detected, 1 mV variation per spill, system with Configuration 2, gain 5

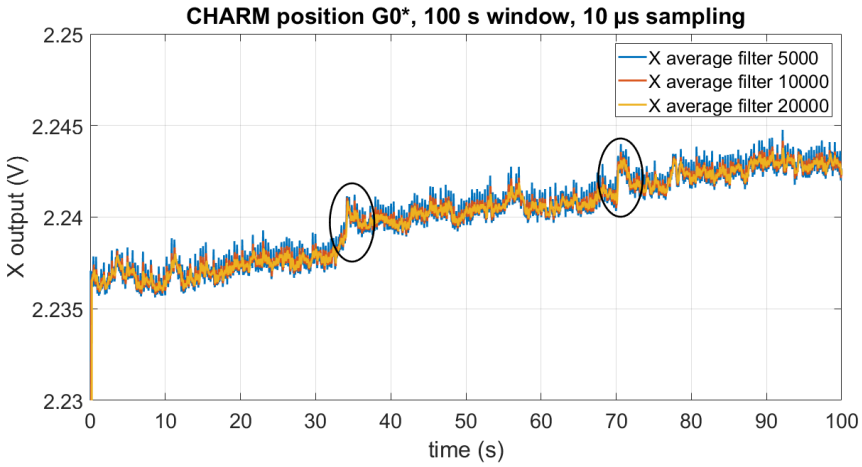

Figure 80. CHARM measurement at G0* position, using Configuration 2 for gain 4 and sampling every 10 µs

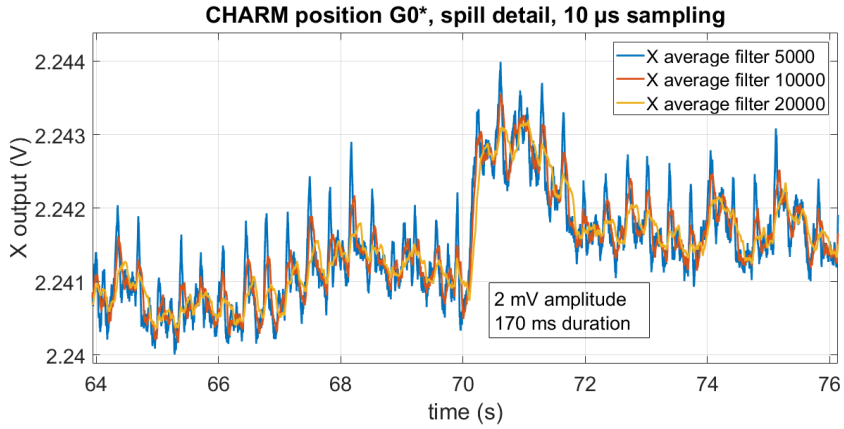

Figure 81. Spill detail of CHARM measurement at G0* position, using Configuration 2 for gain 4 and sampling every 10 µs

Measurements obtained in position G0* can be seen in **Figure 80** and **Figure 81** for a configured gain 4. Plots show data collected after applying three different window average filters. It is observed how the spill profile amplitude is near the system limit of detection, due to the level of noise. Moreover, from calibrations carried out at CC60 room, it can be seen how for this configured gain, 2 mV of amplitude of the spill corresponds to approximately 400 µGy/spill.

Figure 80 in addition, shows the carriers recombination (increasing slope) when no spill is detected, due to the large amount of recharges carried out on it. It is noticed owing to system small amplitude response to a single spill. The charge anneals from the FG as observed before in FG based systems [1].

More measurements were conducted using same gain configuration in a different position in order to have more dose per spill, and obtain larger amplitude response of the system per spill.

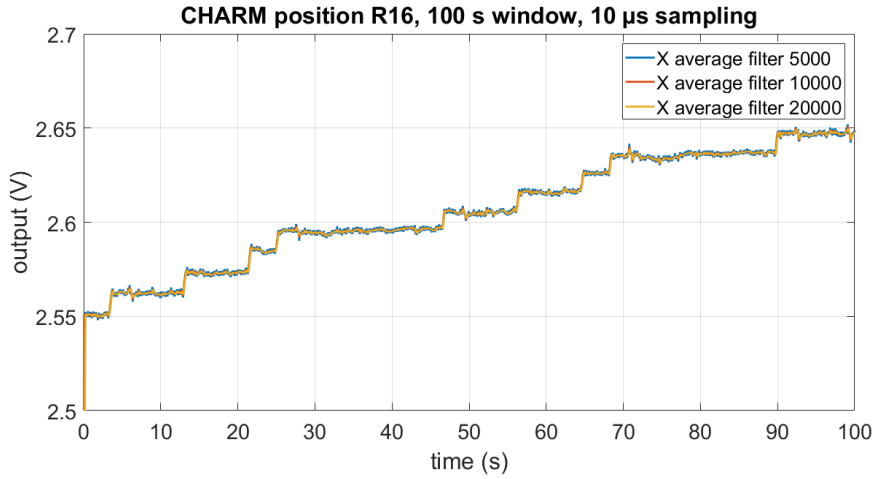

Figure 82. CHARM measurement at R16 position, using Configuration 2 for gain 4 and sampling every 10 µs

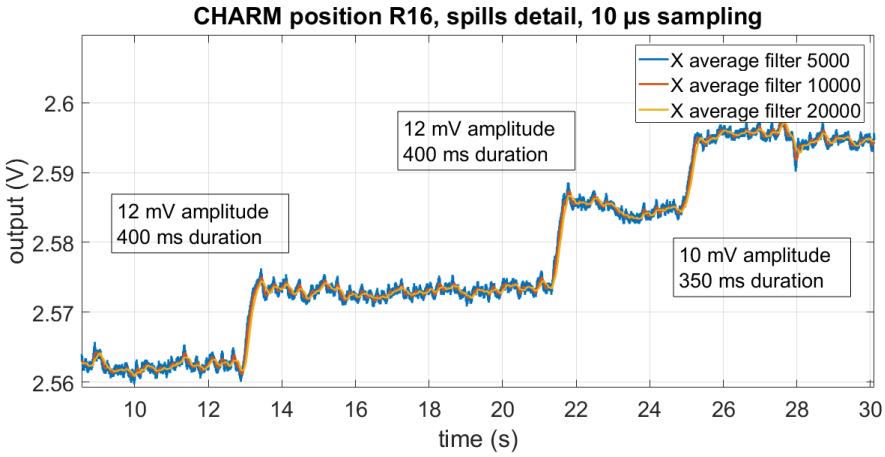

Figure 83. Spills detail of CHARM measurement at R16 position, using Configuration 2 for gain 4 and sampling every 10 µs

The amplitude of the spills detected in R16 were around 10 mV. Using the 60-Co calibration of the system, it corresponds to 2,04 mGy/spill. It is in agreement with expected radiation intensity in this position, as it is shown in **Table 14**. As it is depicted in **Figure 82** and **Figure 83**, spills at CHARM are not generated in a constant timing base but between spills the time can change from few seconds up to tens of seconds.

The system response in Configuration 2 and gain 4 was accurate enough to sample the beam profile along the time. However, looking in more detail to the shape of the spill it is appreciated how after applying the average filtering is not detailed enough using a 10 µs sampling rate. Hence, more measurements using different sampling rates have been presented in **Figure 84** and **Figure 85**.

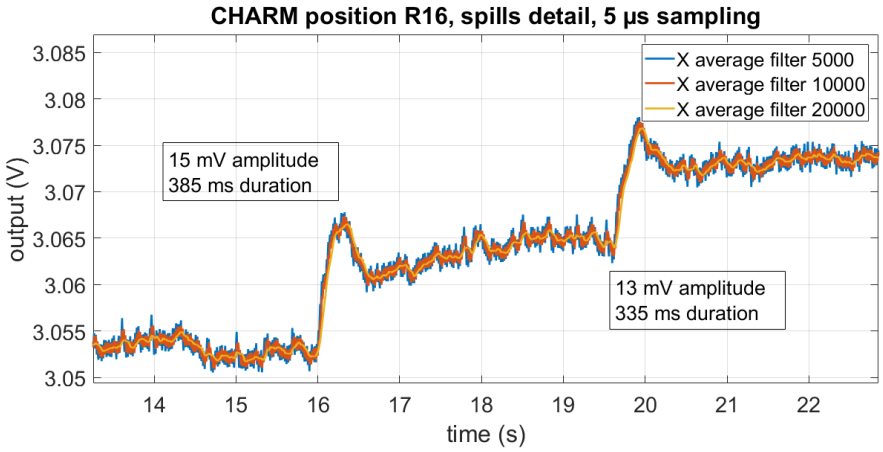

Figure 84. Spills detail of CHARM measurement at R16 position, using Configuration 2 for gain 4 and sampling every 5 µs

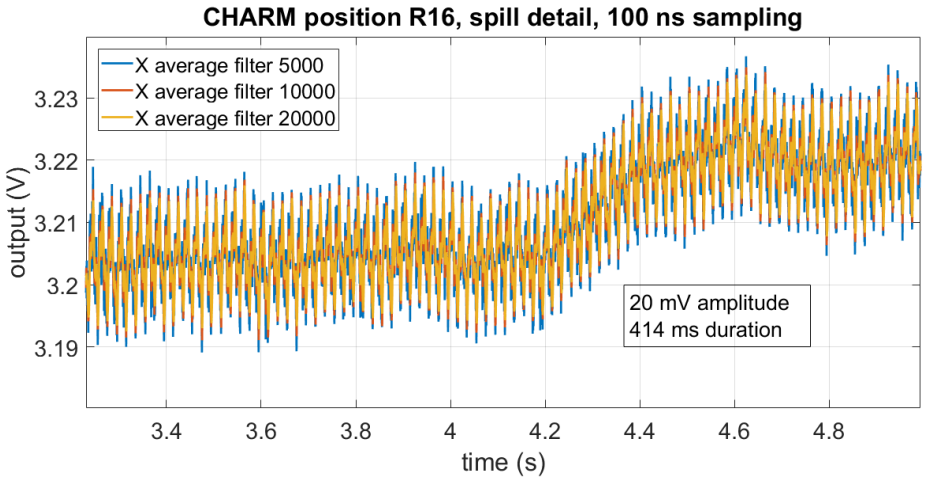

Figure 85. Spills detail of CHARM measurement at R16 position, using Configuration 2 for gain 4 and sampling every 100 ns

By increasing the sampling rate, the shape of the spill has been retrieved by the system with higher accuracy. However, the noise in the measurement is increased as well.

In conclusion, the system fast response to the radiation (it is able to measure millisecond radiation pulses), the output amplification (up to 188) of the FG discharge and the second channel with a replica MOS, which permits a good temperature compensation is a good improvement with respect to the already known FGDOS® dosimeter. The radiation campaigns conducted first under a 60-Co source and later under a mixed field environment demonstrated the system to be a good candidate

for detecting fast-pulsed radiation environments. Those are preliminary results for investigating the limitations of the system.

Parameters as the minimum detectable dose of the system have been extracted in the pre-calibration carried out under a 60-Co source. Future work will focus on the improvement of this, by understanding better the source of the noise measured. Thus, the detection of the spill shape would be even more accurate by reducing it.

Additional work will be focused in extracting the spill profile. Hence, the derivative of the time-based data would be extracted. Moreover, higher gain configurations (up to 6) will be tested to increase the amplitude response of the incoming spill detected. Finally, new measurements using a reference sensor, as for example a diamond detector [74, 75 and 76] must be carried out as future work. With this, it will be possible to compare the system presented herein with other commonly used systems in beam monitoring.

Chapter 6. Conclusions and Outlooks

This work is dedicated to the design and test of the new FGDOS® version, which is an upgrade of previous FGDOS® versions. It was conceived to fulfil the requirements to be used in the LHC and its injection lines, besides of many other applications. The main objectives during the new FGDOS® version design process were two; to enlarge the TID lifetime and to increase the sensitivity of the dosimeter.

This thesis details the commitment and all efforts made to enhance the radiation hardness and the sensitivity of the FGDOS®, aside of many other features. The radiation robustness of the device have been improved by using RHBD techniques after investigating TID effects in the technology that FGDOS® is fabricated. By contrast, the sensitivity has been enhanced by making an exhaustive and cautious study of the sensor core structure, from the theory to real implemented structures. This permitted to find out which is the most sensitive structure composed of FG and reading n-MOS to be duly embedded in the new FGDOS® version.

In order to enhance the radiation hardness of the new FGDOS® version a specific radiation testing strategy has been planned using TCs, which include either simple circuits or devices. As starting point, simple device structures were used in order to understand better TID effects in the technology. Afterwards, circuits that are more complex were designed to predict the behaviour under TID radiation, where effects can come out by interaction between devices depending on the circuit architecture.

The design of the most sensitive sensor core structure has taken into account many considerations. First, to understand the FG detection response to TID from the analysis of two theoretical studies found in the recent literature. Second, to understand the low frequency noise in n-MOS transistors. Finally, by understanding the relationship between the FG capacitance and other parasitic non-desired capacitances connected to it (injector and reading n-MOS). The resulting sensor core structure was tailored to all those aspects.

Furthermore, the improvement of all circuitries in the chip have been achieved. By keeping the same or similar functionalities of the circuits, but by increasing the

endurance to the TID radiation. For that purpose, many TCs have been designed and tested to bear out that new circuits designed attained these objectives.

Concerning all new features included in the new FGDOS® version, different circuits have been embedded or upgraded. Features as the option of discharging the FG in a controlled way, or a charge pump circuit to generate the high voltage needed to recharge the FG, or an ID number to have a tracking number of each device or the standby mode to have an ultra-lower power consumption by keeping the detection of the dosimeter have been incorporated.

New FGDOS® version design arose a better dosimeter in terms of functionality and easy to use dosimeter from user's point of view. It is a dosimeter developed for microcontroller-based applications (using an SPI interface), needing only a +5 volts power supply to fully work. Adding this, to its higher sensitivity to TID radiation with respect to previous FGDOS® version (60 kHz/Gy in front of 30 kHz/Gy in previous version) and radiation TID lifetime extended up to 800 Gy, more than three times larger than previous FGDOS® version (only 250 Gy), makes it a better dosimeter.

Despite all those new positives outcomes, many improvements can still been done by investigating further some structures or circuits. For instance, bipolar devices used in the design were directly developed using RHBD techniques but not tested in detail, concretely for enhanced low dose rate sensitivity (ELDRS) effects. Some bipolars devices depending on the technology used to fabricate them are sensitive to those kind of effects and further investigations should be conducted in this sense. Regarding the injector tests performed, more measurements should be carried out to try to find out the reproducibility of both injector structures investigated when repetitive 14 volts pulses (as occurs in the real application) are applied between terminals of the injector.

Furthermore, more radiation campaigns should be conducted in distinct facilities. Radiation tests under heavy ions, protons and neutrons must be arranged. By doing this, it will be possible to better understand if the new FGDOS® version has any failure or demonstrates a non-expected behaviour under these kinds of radiations. Not only TID effects but also Single Event Effects (SEE), or Displacement Damage (DD) must be considered.

The current technology used to fabricate and produce the new FGDOS® version demonstrated to be useful for applications up to around 1 kGy of cumulated TID and keeping the sensitivity in the sensor core structure to detect TID. Nevertheless, an increase of the current consumption have been observed even when RHBD techniques have been used in the new design. Hence, new approaches must be investigated to try to lower this effect in the current technology or a new technology process with smaller gate oxide thicknesses must be used. A new technology process has the problem that technologies with thinner gate oxides are more sensitive to SEE. In addition, it must be demonstrated that the sensor core still has good detection performance when implemented in this new technology process. A priori an advantage of a new technology process with thinner gate oxides should be the better radiation robustness of the dosimeter to TID, it would probably be possible to extend it up to tens of kGy or MGy.

Apart of the new FGDOS® version design, another important step ahead made in this thesis was the new FG-based architecture using TIAs (FGTIA) to better detect fast-pulsed radiation environments. The work presented is a first trial that open a road for future developments in this direction.

Future work regarding the FGTIA system design should focus in few different aspects. For example, the system should include all the design in one single chip to increase the SNR of the FGTIA system. In addition, current inputs from TIAs should be better adapted for the FG sensor core structure and all circuits designed following RHBD techniques. To conclude, more experiments shall be carried out to better understand the detection performance of the system for different gains and as well the fast-pulsed beam profile extracted (spill shape) from the time-based measurements of the FGTIA system.

To date, the new FGDOS® version is being produced in mass using a QFN 32-pin 5 mm x 5 mm package embedding two sensors each package for redundancy purposes. Finally, the current FGDOS® version is going to be included by CERN in many different detection systems to monitor the radiation within a detection system with other kind of detectors (i.e. to detect SEE or neutrons, using memory devices) that complement its detection of TID. These detection systems will be used at LHC and its injection lines at ground level but also will be embedded to fly in space missions for TID radiation monitoring during the flight.

The original contributions to the FGDOS® from the work done in this thesis are:

1- Sensitivity enhancement by studying the basic mechanisms that play a role in the FG performance when exposed to TID.

2- High-voltage for the recharge process generated on-chip.

3- Discharge of the FG in a controlled manner without radiation for debug purposes.

4- ID number permitting effective tracking of each chip.

5- Standby mode, for ultra-low power applications.

6- Design implemented using RHBD techniques, in order to improve its endurance to TID.

Bibliography

[1] E. García-Moreno, E. Isern, M. Roca, R. Picos, J. Font, J. Cesari and A. Pineda “Temperature Compensated Floating Gate MOS Radiation Sensor with Current Output”, IEEE Transactions on Nuclear Science, vol. 60, no. 5, pp. 4026 – 4030, September 2013.

[2] E. García-Moreno, E. Isern, M. Roca, R. Picos, J. Font, J. Cesari, A. Pineda “Floating Gate CMOS Dosimeter with Frequency Output”, IEEE Transactions on Nuclear Science, vol. 59, no. 2, pp. 373 – 378, February 2012.

[3] S. Danzeca, J. Cesari, M. Brugger, L. Dusseau, A. Masi, A. Pineda and G. Spieza “Characterization and Modeling of a Floating Gate Dosimeter with Gamma and Protons at Various Energies”, IEEE Transactions on Nuclear Science, vol. 61, no. 6, pp. 3451 – 3457, November 2014.

[4] M. Álvarez, C. Hernando, J. Cesari, A. Pineda, E. García-Moreno “Total Ionizing Dose Characterization of a Prototype Floating Gate MOSFET Dosimeter for Space Applications”, IEEE Transactions on Nuclear Science, vol. 60, no. 6, pp. 4281 – 4288, December 2013.

[5] K. Roeed, M. Brugger, G. Spiezia, "An overview of the radiation environment at the LHC in light of R2E irradiation test activities", CERN, September 2011.

[6] J. Mekki, M. Brugger, R. G. Alia, A. Thornton, N. C. Dos Santos Mota and S. Danzeca, "CHARM: A new mixed field facility at CERN for radiation test in ground atmospheric space and accelerator representative environments", Proc. 24th RADECS Conf., vol. H-2, 2015

[7] G. Spieza, P. Peronnard, A. Masi, M. Brugger, M. Brucoli, S. Danzeca, R. Garcia Alia, R. Losito, J. Mekki, P. Oser, R. Gaillard and L. Dusseau “A New RadMon Version for the LHC and its Injection Lines”, IEEE Transactions on Nuclear Science, vol. 61, no. 6, pp. 3424–3431, December 2014.

[8] J. Cesari, A. Barbancho, A. Pineda, G. Ruy, and H. Moser “Floating Gate Dosimeter Measurements at 4M Lunar Flyby Mission”, The Nuclear and Space Radiation Effects Conference (NSREC) Radiation Effects Data Workshop (REDW), Boston, July 2015.

[9] J. R. Srour, C. J. Marshall, and P. W. Marshall, “Review of displacement damage effects in silicon devices” *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 653–670, Jun. 2003.

[10] J. R. Srour and J. W. Palko, “Displacement damage effects in irradiated semiconductor devices” *IEEE Trans. Nucl. Sci.,* vol. 60, pp. 1740–1766, 2013.

[11] M. Moll, “Displacement Damage in Silicon Detectors for High Energy Physics” *IEEE Trans. Nucl. Sci.*, vol. 65, no. 8, pp. 1561–1582, August 2018.

[12] P. Fernández-Martínez, F.R. Palomo, S. Hidalgo, C. Fleta, F. Campabadal, D. Flores, “Analysis of displacement damage effects on MOS capacitors” *Nucl. Instr. Meth. Phys. Res A*., vol. 730, pp. 91, 2013.

[13] L. Ding, S. Gerardin, M. Bagatin, D. Bisello, S. Mattiazzo and A. Paccagnella, “Investigation of total ionizing dose effect and displacement damage 65 nm CMOS transistors exposed to 3 MeV protons” *Nucl. Instr. Meth. Phys. Res. A,* vol. 585, pp. 104-108, 2015.

[14] S. Duzellier, “Radiation effects on electronic devices in space”, *Aerospace Science and Technology*, 9 (2005) 93-99.

[15] R. Gaillard, “Chapter 2: Single Event Effects: Mechanisms and Classification”, *Soft Errors in Modern Electronic Systems*, Nicolaidis, M. (Ed.), 2011, XVII, 318 p., ISBN: 978-1-4419-6992-7.

[16] T. P. Ma, P. V. Dressendorfer, “Ionizing Radiation Effects in MOS Devices & Circuits”, 1989.

[17] H. J. Barnaby, “Total-ionizing-dose effects in modern CMOS technologies”, *IEEE Trans. Nucl. Sci.,* vol. 53 (2006) pp. 3103-3121.

[18] T.R. Oldham and F. B. McLean, “ Total ionizing dose effects in MOS oxides and devices”, *IEEE Transactions on Nuclear Science,* vol. 50, no. 3, pp. 483-499, 2003.

[19] I. S. Esqueda, H. J. Barnaby, M. L. Alles, “Two-dimensional methodology for modeling radiation-induced off-state leakage in CMOS technologies”, *IEEE Trans. Nucl. Sci.*, vol. 52 (2004) pp. 2259.

[20] H. J. Barnaby, M. Mclain and I. S. Esqueda, “Total-ionizing-dose effects on isolation oxides in modern CMOS technologies”, *Nucl. Instr. Meth. B*, 261 (2007) 1142-1145.

[21] M. Sajid, N.G. Chechenin, F. S. Torres, M. N. Hanif, U. A. Gulzari, S. Arslan and E. U. Khan, “Analysis of Total Ionizing Dose effects for highly scaled CMOS devices in Low Earth Orbit”, *Nucl. Inst. and Meth. B*, 428 (2018) 30-37.

[22] R.G. Forbes and J.H. B. Deane, “Reformulation of the standard theory of Fowler-Nordheim tunnelling and cold field electron emission”, Proceedings of the Royal Society of Mathematical, Physical and Engineering Sciences, vol. 464, no. 2100, pp. 3378-3378, 2008.

[23] N. M. Ravindra and J. Zhao, “Fowler-Nordheim tunnelling in thin SiO_2 films”, Smart Materials and Structures, vol. 1, no. 3, p. 197, 1992.

[24] M. Brucoli, S. Danzeca, M. Brugger, A. Masi, A. Pineda, J. Cesari and L. Dusseau, “A complete qualification of floating gate dosimeter for CERN applications”, Proceedings at 15th European Conference on Radiation and Its Effects on Components and Systems (RADECS). September 2016.

[25] R. Ferraro, S. Danzeca, M. Brucoli, A. Masi, M. Brugger, L. Dilillo, ”Design of a radiation tolerant system for total ionizing dose monitoring using floating gate and RadFET dosimeters”, *Journal of Instrumentation*, vol. 12, Topical Workshop of Electronics for Particle Physics (TWEPP 2016), April 2017.

[26] M. Brucoli, S. Danzeca, M. Brugger, A. Masi, A. Pineda, J. Cesari, L. Dusseau and F. Wrobel “Investigation on Passive and Autonomous Mode Operation of Floating Gate Dosimeters“, Proceedings at 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS). September 2018.

[27] F. Pozzi, R. G. Alia, M. Brugger, P. Carbonez, S. Danzeca, B. Gkotse, M. R. Jaekel, F. Ravotti, M. Silari and M. Tali, “CERN irradiation facilities”, *Radiation Protection Dosimetry* 1-5 (2017).

[28] A. Thorton, “CC60 Facility”, presentation at RADWG (April 2015), https://indico.cern.ch/event/381653/sessions/159361/attachments/760653/1043432/CC60_intro_radwg.pdf

[29] J. Mekki, M. Brugger, R. G. Alia, A. Thornton, N. C. Dos Santos Mota and S. Danzeca, “A mixed field facility at CERN for radiation test: CHARM”, *Proceedings,* RADECS, 2015.

[30] J. Mekki, M. Brugger, R. G. Alia, A. Thornton, N. C. Dos Santos Mota and S. Danzeca, “CHARM: A Mixed Field Facility at CERN for Radiation Tests in Ground, Atmospheric, Space and Accelerator Representative Environments”, *IEEE Transactions on Nuclear Science,* Vol. 63, no. 4, August 2016.

[31] CHARM facility website http://charm.web.cern.ch/CHARM/

[32] F. Xue, L. Ping, L. Wei, Z. Bin, X. Xiaodong, W. Gang, H. Bin and Z. Yahong, “Gate-enclosed NMOS transistors”, *Journal of Semiconductors*, vol. 32, no. 8, August 2011.

[33] M. Kuczynska, S. Gozdur, S. Burgiel, M. Firlej, T. Fiutowski, M. Idzik, S. Michelis, J. Moron, D. Przyborowski and K. Swientek, “Development of Radiation-hard Bandgap Reference and Temperature Sensor in CMOS 130 nm Technology”, *Proceedings of the 22nd International Conference of “Mixed Design of Integrated Circuits and Systems”*, June 2015.

[34] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Florian, A. Giraldo, E. Heijne, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira and W. Snoeys, “Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects”, *IEEE Transactions on Nuclear Science,* vol. 46, no. 6, December 1999.

[35] J. Cesari, A. Pineda, S. Danzeca, A. Masi, M. Brugger, M. Fernandez, E. Isern, M. Roca and E. García-Moreno “Analysis of two different charge injector candidates for an on-chip Floating Gate recharging system”, 12th International Conference on Design & Technology if Integrated Systems in Nanoscale Era (DTIS). April 2017.

[36] J. Cesari, D. Gomez, M. Roca, E. Isern, A. Pineda and E. García-Moreno “Floating Gate P-MOS Radiation Sensor Charging Cycles Characterization” The Nuclear and Space Radiation Effects Conference (NSREC) Radiation Effects Data Workshop (REDW), Paris, July 2014.

[37] J.S. Sanjeev Kumar Gupta and J. Akhtar, “Materials and processing for gate dielectrics on silicon carbide (SiC) surface, physics and technology of silicon carbide devices” in *Physics and Technology of Silicon Carbide Devices*, 2013, ISBN 978-9535109174.

[38] R. G. Forbes and J. H. B. Deane, “Reformulation of the standard theory of Fowler- Nordheim tunnelling and cold field electron emission”, Proceedings of the Royal Society of Mathematical, Physical and Engineering Sciences, vol. 464, no. 2100, pp. 3378-3378, 2008.

[39] N. M. Ravindra and J. Zhao, “Fowler-Nordheim tunnelling in thin SiO_2 films”, Smart Materials and Structures, vol. 1, no. 3, p. 197, 1992.

[40] A. Gehring and S. Selberherr, “Modeling of Tunneling Current and Gate Dielectric Reliability for Nonvolatile Memory Devices”, *IEEE Transactions on Device and Materials Reliability*, vol. 4, no. 3, September 2004.

[41] R. Entner, A. Gehring, H. Kosina, T. Grasser and S. Selberherr, “Impact of Multi-Trap Assisted Tunneling on Gate Leakage of CMOS Memory Devices”, *Proc. Nanotech*, vol. 3, pp. 45-48, 2005.

[42] J. Cesari, M. Brucoli, S. Danzeca, A. Pineda, A. Masi, M. Brugger, S. Gilardoni, E. Isern, M. Roca and E. García-Moreno “Study of Floating Gate MOS Structures to improve the noise and sensitivity as Radiation Dosimeter”, Proceedings at 16th European Conference on Radiation and Its Effects on Components and Systems (RADECS). September 2017.

[43] J. P. Mitchell, “Radiation-induced space-charge build-up in MOS structures”, *IEEE Transactions on Electron Devices,* vol. ED-14, pp. 764-774, 1967.

[44] S. Danzeca, “The new version of the Radiation Monitor system for the electronics at CERN. Electronic components radiation hardness assurance and sensor qualification”, pp. 142, 2015.

[45] S. Cristensson, I. Lundstrom and C. Svensson, “Low frequency noise in MOS transistors”, *Solid-State Electron*, vol. 11, pp. 797-812, 1968.

[46] E. Isern, M. Roca, E. García-Moreno, J.C. Font, J. Cesari and A. Pineda “Characterization of a floating-gate sensor for X-ray dose detection”, Proceedings at 14th European Conference on Radiation and Its Effects on Components and Systems (RADECS). September 2013.

[47] M. Brucoli, S. Danzeca, J. Cesari, M. Brugger, A. Masi, S. Gilardoni, A. Pineda, L. Dusseau and F. Wrobel “Investigation on the Sensitivity Degradation of Dosimeters based on Floating Gate Structure”, Proceedings at 16th European Conference on Radiation and Its Effects on Components and Systems (RADECS). September 2017.

[48] E. I. Starchenko, N. N. Prokopenko and P. S. Budyakov “The Radiation-Hardened Voltage Reference On Bipolar and JFET Transistors”, Proceedings at the 8th IEEE GCC Conference and Exhibition, Muscat, Oman, 1-4 February 2015.

[49] G. Traversi, F. de Canio, L. Gaioni, M. Manghisoni, S. Mattiazzo, L. Ratti, V. Re and E. Riceputi “Characterization of bandgap reference circuits designed for high energy physics applications”, *Journal of Nuclear Instrumentation and Methods in Physics Research*, A 824, 371-373, 2016.

[50] Daniel M. Fleetwood “Total Ionizing Dose Effects in MOS and Low-Dose-Rate-Sensitive Linear-Bipolar Devices”, *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, June 2013.

[51] D. A. Adams, H. A. Barnes, N. P. Goldstein, D. C. Harms, J. J. Horner, C. E. Sherman and C. Stodart “A Total Ionizing Dataset Dose Dataset for Vertical NPN Bipolar Transistors” IEEE Radiation Effects Data Workshop (REDW), Paris, France, July 2014.

[52] F. Toscano, A. Ouellet, F. Tilhac and T. Lagarrigue “Dose Rate Effects on Bipolar Components” IEEE Radiation Effects Data Workshop (REDW), San Francisco, CA, USA, 2013.

[53] K. F. Galloway, R. L. Pease, R. D. Schrimpf and D. W. Emily “From Displacement Damage to ELDRS: Fifty Years of Bipolar Transistor Radiation Effects at the NSREC”, *IEEE Transactions on Nuclear Science,* vol. 60, no. 3, June 2013.

[54] R. M. Chavez, B. G. Rax, L. Z. Scheick and H. Johnston “Total Ionizing Dose Effects in Bipolar and BiCMOS Devices” IEEE Radiation Effects Data Workshop (REDW), Seattle, WA, USA, 2005.

[55] M. F. Bernard, L. Dusseau, S. Buchner, D. McMorrow, R. Ecoffet, J. Boch, J. R. Vaillé, R. D. Schrimpf and K. LaBel “Impact of Total Ionizing Dose on the Analog Single Event Transient Sensitvity of a Linear Bipolar Integrated Circuit”, *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, December 2007.

[56] L. T. Clark, K. E. Nielsen and K. E. Holbert “Radiation Hardened By Design Digital I/O for High SEE and TID Immunity”, *IEEE Transactions on Nuclear Science*, vol. 56, no. 6, December 2009.

[57] Y. Cao, P. Leroux and M. Steyaert “Radiation-Tolerant Delta-Sigma Time-to-Digital Converters”, ACSP- Analog Circuits And Signal Processing, ISBN 978-3-319-11841-3, Springer, 2015.

[58] R. R. Harrison “The MOS Transistor in Weak Inversion”, EE 5720/University of Utah.

[59] V. Gromov, A. J. Annema, R. Kluit, J. L. Visschers and P. Timmer “A Radiation Hard Bandgap Reference Circuit in a Standard 0.13 µm CMOS Technology”, *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, December 2007.

[60] S. S. Chouhan and K. Halonen “A Simple All MOS Voltage Reference for RFID Applications”, IEEE NORCHIP Conference, November 2013.

[61] E. Vilella, A. Diéguez “Design of a Bandgap Reference Circuit with Trimming for Operation at Multiple Voltages and Tolerant to Radiation in 90nm CMOS Technology”, IEEE Annual Symposium on VLSI, 2010.

[62] K. J. Shetler, N. M. Atkinson, W. T. Holman, J. S. Kauppila, T. D. Loveless, A. F. Witulski, B. L. Bhuva, E. X. Zhang and L. W. Massengill “Radiation Hardening of Voltage References Using Chopper Stabilization”, *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, December 2015.

[63] Y. Piccin, H. Lapuyade, Y. Deval, C. Morche, J. Y. Seyler and F. Goutti “Radiation-Hardening Technique for Voltage Reference Circuit in a Standard 130 nm CMOS Technology”, *IEEE Transactions on Nuclear Science*, vol. 61, no. 2, April 2014.

[64] A. Stoynova, B. Bonev and N. Brayanov “Thermographic Approach for Reliability Estimation of PCB”, 41st International Spring Seminar on Electronics Technology (ISSE), 2018.

[65] M. Vellvehi, X. Perpiña, D. Sanchez, P. Fernandez-Martinez, D. Flores and X. Jorda, “Failure Analysis in Power Devices using Lock-in Infrared Thermography”, 19th International Conference on Thermal, Mechanical and Multi-Physucs Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), 2018

[66] M. Vellvehi, X. Perpiña, J. Leon, D. Sanchez, X. Jorda and J. Millan, “Lock-in Infrared Thermography: a tool to locate and analyse failures in power devices”, Spanish Conference on Electron Devices (CDE), 2017.

[67] W. Liang, K. Alexandrou, M. Klebanov, C. Kuo, I. Kymissis, B. Sundaram and J. Liou, “Characterization of ESD Protection Devices under Total Ionizing Dose Irradiation”, IEEE 24th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), 2017.

[68] Q. Shi, Q. Xiao, Y. Liu and Y. En, “Measurement of ESD protection structure irradiation degradation using TLP method”, International Conference on Quality, Reliability, Risk, Maintenance and Safety Engineering (QR2MSE), 2013.

[69] B. Gkotse, M. Glaser, M. Moll and F. Ravotti “IRRAD: The New 24 GeV/c Proton Irradiation Facility at CERN”, AccApp’15, Nov. 2015.

[70] M. McCarthy, D. Anderson, I. Campisi, F. Casagrande, R. Cutler, G. Dodson, K. Kasemir, S. Kim, D. Gurd, J. Galambos, Y. Kang, H. Ma, M. Riemer, J. Schubert and M. Stockli “Spallation Neutron Source (SNS) high pulse repetition rate considerations” PAC Conference, June 2007.

[71] J. Alonso “The Spallation Neutron Source Project”, Proceedings of PAC Conference, New York, 1999.

[72] M. Glaser, F. Ravotti and M. Moll “Dosimetry Assessments in the Irradiation Facilities at the CERN-PS Accelerator”, RADECS Conference, September 2005.

[73] G. Royo, M. Garcia-Bosque, C. Sánchez-Azqueta, C. Aldea, S. Celma and C. Gimeno “Transimpedance amplifier with programmable gain and bandwith for capacitive MEMS accelerometers”, I2MTC Conference, May 2017.

[74] J. Bok et al. “Beam-monitors for TESLA based on diamond-strip-detectors”, IEEE Nuclear Science Symposium, Conference Record, 2003.

[75] P. Dong et al. “Beam Condition Monitoring with Diamonds at CDF”, *IEEE Trans. On Nucl. Sci.,* vol. 55, no.1, pp. 328-332, February 2008.

[76] M. Girolami et al. “Diamond Detectors for UV and X-Ray Source Imaging”, *IEEE Electron Device Letters*, vol. 22, no. 2, pp. 224-226, December 2011.