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**SINGLE EVENT TRANSIENT PROPAGATION
AND CAPTURE IN NANOMETER CMOS ICs:
ANALYSIS AND MODELING**

Xavier Gili Pérez



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Doctoral Programme of Electronic Engineering

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Resum

Durant les últimes dècades la tecnologia CMOS ha sofert un escalat constant que ha permès l'augment de la freqüència d'operació i de la densitat d'integració. Aquestes fites, a priori beneficioses, han comportat l'aparició de fenòmens adversos en el funcionament dels circuits electrònics. Uns d'aquests efectes són els anomenats Single-Event Effects (SEE) causats per la col·lecció de càrrega deguda a l'impacte d'una partícula energètica en un node sensible del circuit. Els SEEs es poden dividir en Single-Event Upsets (SEU) si canvien l'estat d'un element de memòria i en Single-Event Transients (SET) si generen un pols de tensió en un circuit combinacional. Un SET pot esdevenir un SEU si és capaç de propagar-se per un circuit combinacional, arribar a un element de memòria i ésser capturat, guardant un valor erroni.

Aquesta tesi s'ha centrat en l'estudi de la propagació dels SETs. Per això s'ha desenvolupat un model analític que prediu les característiques del SET propagat. El model es pot utilitzar per observar com evolucionen aquestes característiques quan el SET es propaga a través d'un camí dins un circuit, així com per avaluar la sensibilitat dels nodes d'un circuit als SETs.

El model s'ha validat mitjançant resultats experimentals. La tècnica utilitzada per generar els SETs ha estat la del làser polsat, que s'utilitza per emular la deposició de càrrega que genera la radiació.

També s'ha estudiat l'estabilitat de les cel·les SRAM, proporcionant un model per calcular la càrrega crítica, que consisteix en la càrrega mínima necessària per generar un SEU, i que és la mètrica més comú per mesurar l'estabilitat de les cel·les SRAM.

L'estudi s'ha completat amb el desenvolupament d'un model per calcular la probabilitat de captura d'un SET per part d'un element de memòria, incloent la dependència tant de la durada com de l'alçada del SET.

Resumen

Durante las últimas décadas la tecnología CMOS ha sufrido un escalado constante permitiendo el aumento de la frecuencia de operación y de la densidad de integración. Estos logros, a priori beneficiosos, han implicado la aparición de fenómenos adversos para el correcto funcionamiento de los circuitos electrónicos. Unos de estos efectos son los llamados Single-Event Effects (SEE) causados por la colección de carga debida al impacto de una partícula energética en un nodo sensible del circuito. Los SEEs se pueden dividir en Single-Event Upsets (SEU) si cambian el estado de un elemento de memoria y en Single-Event Transients (SET) si generan un pulso de tensión en un circuito combinacional. Un SET puede dar lugar a un SEU si es capaz de propagarse por un circuito combinacional, llegar a un elemento de memoria y ser capturado, guardando un valor erróneo.

Esta tesis se ha centrado en el estudio de la propagación de los SETs. Para ello se ha desarrollado un modelo analítico que predice las características del SET propagado. El modelo se puede utilizar para observar cómo evolucionan estas características cuando el SET se propaga a través de un camino dentro de un circuito, así como para evaluar la sensibilidad de los nodos de un circuito a los SETs.

El modelo se ha validado mediante resultados experimentales. La técnica utilizada para generar los SETs ha sido la del laser pulsado, que se utiliza para emular la deposición de carga que genera la radiación.

También se ha estudiado la estabilidad de las celdas SRAM, proporcionando un modelo para calcular la carga crítica, que es la carga mínima necesaria para generar un SEU, y que es la métrica más común para medir la estabilidad de las celdas SRAM.

El estudio se ha completado con el desarrollo de un modelo para calcular la probabilidad de captura de un SET por un elemento de memoria, incluyendo la dependencia tanto en duración como en altura del SET.

Abstract

In the last decades CMOS technology have experienced a constant scaling allowing an increasing operating frequency and integration density. These achievements imply adverse effects to the proper operation of electronic circuits. One of these effects are the Single-Event Effects (SEE) caused by the charge collection due to the impact of an energetic particle in a sensitive circuit node. The SEES can be divided into Single-Event Upsets (SEU) if there is a change of the state of a memory element and Single-Event Transients (SET) if they generate a voltage pulse in a combinational circuit. An SET may become an SEU if it is able to propagate through a combinational circuit, reaching a memory element and being captured, storing a wrong value.

This thesis has focused on the study of SET propagation. In this way we have developed an analytical model which predicts the characteristics of the propagated SET. The model can be used to observe how these characteristics evolve as the SET propagates through a path in a circuit, and to assess the sensitivity of the nodes of a circuit to SETs.

The model has been validated through experimental results. The technique used to generate SETs is the pulsed laser, which is used to emulate the charge deposition that radiation generates.

We also studied the stability SRAM cells, providing a model to calculate the critical charge, consisting in the minimum charge required to generate an SEU, that is the most common metric to measure the stability of the SRAM cell.

The study is completed with the development of a model to compute the SET capture probability by a memory element, including the dependence on the SET length and height.

List of publications

X. Gili, S. Barceló, S. Bota, J. Segura, “Analytical modeling of glitch propagation in nanometer ICs”, SPIE Microtechnologies. Prague, Czech Republic, 2011.

X. Gili, S. Barceló, S. Bota, J. Segura, “Analytical Modeling of Single Event Transients Propagation in Combinational Logic Gates”, Radiation Effects on Components and Systems (RADECS 11). Sevilla, Spain 2011.

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S. Barceló, X. Gili, S. Bota, J. Segura, “Automatic SET propagation Tool based on analytical model”, Design Automation Conference (DAC) Work-In-Progress, San Diego, 2011.

S. Barceló, X. Gili, S. Bota, J. Segura, “An efficient and scalable STA tool with direct path estimation and exhaustive sensitization vector exploration for optimal delay computation”, Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, 2011.

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Abbreviated terms

CAD	Computed Aided Design
ECC	Error-Correcting Code
EDA	Electronic Design Automation
FF	Flip flop
FPGA	Field Programmable Gate Array
FWHM	Full Width Half Maximum
FWHR	Full Width Half Rail
ISCAS	International Symposium on Circuits and Systems
LET	Linear Energy Transfer
LUT	Look Up Table
MBU	Multiple-Bit Upset
MCU	Multiple-Cell Upset
Q_c	Critical charge
SEB	Single-Event Burnout
SEE	Single-Event Effect
SEFI	Single-Event Functional Interrupt
SEGR	Single-Event Gate Rupture
SEL	Single-Event Latchup
SER	Soft Error Rate
SET	Single-Event Transient
SEU	Single-Event Upset
SPA	Single Photon Absorption
TID	Total Ionizing Dose
TPA	Two Photon Absorption

Chapter 1

Introduction

Since the rise of modern electronics, specially with the development of the transistor in 1948 and later the integrated circuits in 1959, this discipline has evolved astonishingly until the present day. This constant evolution consisting in the reduction of transistor size and the improvements in the manufacturing process led to the scaling integration in chips from *small-scale integration* (SSI) to *medium-scale integration* (MSI), *large-scale integration* (LSI) and *very large-scale integration* (VLSI) following the self-fulfilling [Wes05] Moore's Law [Moo65]. The huge transistor densities reached have favored the massive use of electronic devices in our nowadays lives. Personal computers, smartphones tablets, and what is known as consumer electronics are the paradigm of this trend. One of the most important application fields is within the space environment, where devices are subjected to extremely high levels of radiation compared to the ground level, representing one of the most harsh environment domains for spacecraft hardware as experienced since the very early stages of space exploration. In fact, space exploration and electronics have evolved hand by hand. For instance, in 1958 the Van Allen belts were discovered thanks to the

saturation of a Geiger counter aboard the artificial satellite Explorer I [Vic60]. Another example of radiation effect is the telecommunication satellite Telstar, launched in 1962, whose electronic components (diodes) degraded due to the extremely high radiation. It became the first satellite lost as a consequence of radiation effects. And yet a more recent satellite, devoted to Space Exposure Experiments, was launched on May 2005. And failed after 15.6 days in Earth orbit due to an ion induced latch-up in a bulk SRAM.

1.1 Motivation and objectives

The technology scaling making possible the VLSI circuits also implies a supply voltage reduction and a decrease of the parasitic node capacitances. Both trends favor the generation and critical impact of Single-Event Effects or SEEs (named single-event because they are caused by a single particle). One of these effects is the Single-Event Transient (SET), being a voltage perturbation generated by the impact of a particle within a combinational circuit, that can eventually propagate and get captured at a memory element providing erroneous data. In addition to the voltage and capacitances reduction, the SET impact is also aggravated by the increasing clock frequency because a higher frequency implies a higher probability of an SET being captured by a clocked memory element. The increasing impact of SETs, together with the increase of circuit complexity, demands an extensive study on the SET propagation to determine the SET sensitivity within a circuit. Accurate SET propagation description is key to determine if an SET can be captured or not since there can be paths filtering wide SETs while other paths propagate narrow SETs. In this way, a model to efficiently compute the SET propagation is mandatory and is the main focus of the work being presented. Such model is based on analytical functions making it suitable for efficient CAD implementation.

In the study of SETs, experimental data is crucial. Previous studies on SETs provide experimental data obtained from tests with heavy-ions, protons, neutrons and pulsed lasers. In this work, experimental results obtained using

a pulsed laser impacting various logic chains constructed with standard gates are shown. These results are used to validate the SET propagation model.

Another SEE magnified by technology scaling is the Single-Event Upset (SEU) consisting in the change of the state of a memory element due to a particle strike directly on the memory element. Regarding SEUs, a static metric to measure the robustness of a latch against radiation is developed. For dynamic situations a model to compute the critical charge is proposed.

1.2 Document organization

Chapter 2 provides an overview of the radiation effects on integrated circuits describing the main sources of radiation, the physical mechanisms of interaction with silicon, the effects caused and mitigation techniques.

Chapter 3 describes in detail the Single-Event Transient (SET), reviewing the main previous works. A model to compute the propagation of SETs through combinational circuits is presented and validated through simulations at gate and circuit levels.

Chapter 4 presents the experimental setup of the pulsed laser and the results of the generated SETs, as well as a validation of the model presented in chapter 3.

Chapter 5 is dedicated to study the latch stability providing two methods to compute it. A static method (Line Switch Contour) and a dynamic method (critical charge). A study of the probability of a latch to capture an SET is also included in this chapter.

Finally, chapter 6 sums up the conclusions of the work.

Chapter 2

Radiation effects on ICs

This chapter is dedicated to review the main sources of radiation, describe the physical mechanisms of interaction with silicon, the possible effects and the main techniques available to mitigate them.

2.1 Radiation sources

- Solar wind: The solar wind is a flow from the Sun's corona of charged particles, primarily electrons and protons (with energies up to several keV) at speeds of about 400 km/s.
- Coronal mass ejections: are ejections of huge plasma bubble from the upper solar atmosphere or solar corona. They propagate at

high speeds (several hundred km/s) and collides with the solar wind forming a shock wave that accelerates particles of the environment at high energies. Behind the shock the coronal mass ejection can propagate and interact with the environment near the Earth.

- Solar flares: are sudden and intense variation in brightness. This phenomenon occurs when magnetic energy from the solar atmosphere is released, leading to radiation emission across the entire electromagnetic spectrum.
- Galactic cosmic rays: are charged particles originated outside the solar system representing a background of ions at a very high energy (can reach several hundreds of GeV). Their composition is approximately 89% protons, 10% ^4He and 1% heavy ions.

2.2 Radiation environments

Focusing on the Earth and its vicinity there are basically three radiation environments: radiation belts, atmospheric neutrons and terrestrial radiation sources. The radiation belts consist in charged particles, mainly protons and electrons, trapped by the magnetic field. There is an inner belt that extends from 100 km to 10000 km above the Earth's surface and an outer belt from 13000 to 65000 km. The energy of the particles ranges from 1 keV to 7 MeV for electrons and from 1 keV to 300 MeV for protons.

Cosmic rays interact with the Earth's atmosphere generating neutrons, secondary protons, muons and neutrinos. Regarding SEEs, neutrons are the most important source of radiation [Gai11]. Neutron flux varies with altitude and latitude but its energy spectrum is considered independent of altitude. Neutrons cannot cause errors in integrated circuits directly, but can generate secondary particles that can cause errors, as discussed below.

At ground level, there is still another source of radiation. Some materials

used in packaging or welding, like uranium and thorium, emit radiation. In the case of integrated circuits the major responsible for SEE are alpha particles. Even with very low energies (~ 9 MeV or less) can cause errors due to the proximity of the source [Yan79].

2.3 Interaction of radiation with ICs

Radiation can interact with matter in many different ways depending on the type of radiation, its energy and the target material, but for SEE generation, only charged particles and neutrons interactions are considered. In this section the charge deposition after a particle strike and how this charge is collected to generate an SEE are explained.

2.3.1 Charge deposition

The main resulting effect of an ionizing particle hitting a semiconductor device is the deposition of charge. There are two mechanisms by which ionizing radiation deposits charge in a semiconductor device [Dod05]: direct ionization caused by the incident particle, and indirect ionization due to secondary particles created by nuclear reactions between the incident particle and the target material. Each mechanism is described in more detail:

Direct ionization: when an energetic charged particle strikes the device, it frees electron-hole pairs along the covered path by means of coulombic interactions [Gai11] until it stops when all the energy is lost. Direct ionization is the primary charge deposition mechanism for heavy ions ($Z \geq 2$) and only an exceptional case for protons [Bou07]. The deposited charge is related to the Linear Energy Transfer (LET) of a particle. The LET is explained in more detail in section 2.4.1.1.

Indirect ionization: direct ionization by light particles does not always produce enough charge to cause upsets, but protons and neutrons can interact with nucleus in the semiconductor lattice through inelastic collisions. Many nuclear reactions can take place such as the emission of alpha particles or gamma rays and the recoil of a daughter nucleus (e.g., Si emits an alpha particle and a recoiling Mg nucleus), or a spallation reaction, in which the target nucleus is broken into two fragments (e.g., Si breaks into C and O ions). These reaction products can then deposit energy along their paths by direct ionization. Because these particles are much heavier than the original proton or neutron, they deposit a higher amount of charge as they travel, and therefore may be capable of causing an SEE [Dod05].

2.3.2 Charge collection

After the strike of a particle, a high charge density region, approximately cylindrical [Mes82], is generated beneath the struck surface. The most sensitive regions for this mechanism are reverse-biased p-n junctions due to the high field present in the depletion region capable of collecting the generated charge [Dod05]. An important effect is funneling [Hsi81]. When the generated carriers cross the depletion region around a p-n junction with a high electric field, the presence of the carriers distorts the field and expands it along the track into the substrate (Fig. 2.1). The charge collection inside the funnel is carried out through the drift mechanism. After this process more charge can be collected by diffusion of electrons to the depletion region. Fig. 2.2 shows current pulse induced by this process.

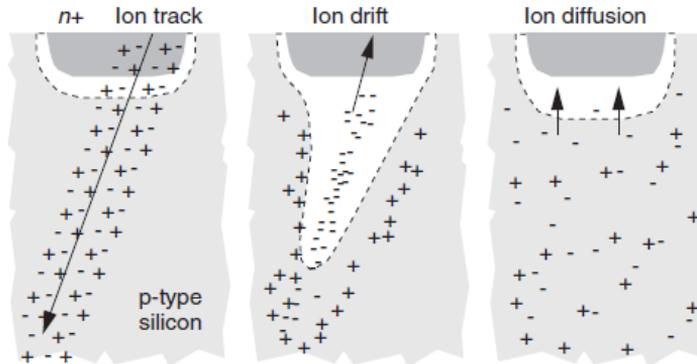


Fig. 2.1. Charge collection in a silicon junction after an ion strike.

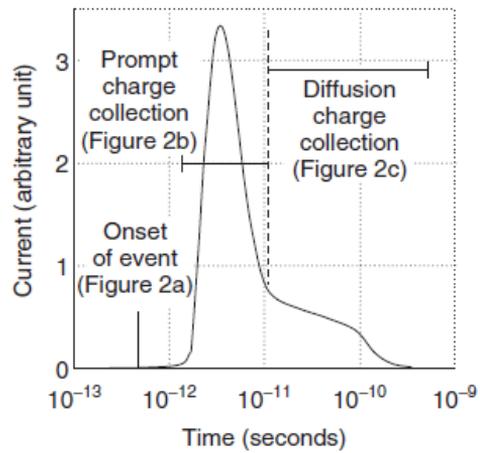


Fig. 2.2. Current induced.

2.4 Radiation effects

2.4.1 Concepts

2.4.1.1 Linear energy transfer

When a particle interacts with the matter it passes through, it transfers its energy to the medium. The charge deposition capacity, through ionization, is described in terms of Linear Energy Transfer (LET) which corresponds to the energy deposition by length unit and depends on the material density, ρ :

$$LET = \frac{1}{\rho} \cdot \frac{\Delta E}{\Delta x} \quad (2.1)$$

When $\Delta E > E_c$ (critical energy), a single event phenomenon may occur. The LET threshold (LET_{th}) is thus defined by this characteristic LET as the minimum LET required for a particle to create a single event. Consequently, components having a high LET_{th} have a good immunity to single events.

2.4.1.2 Cross section

The cross section, σ , is a measure of the sensitivity of a device to a given particle LET or energy. It is defined by the ratio between the number of single events observed on the device and the particle fluence (particles per cm^2) received by the component under test. Thus, the cross section can be interpreted as the probability that a striking particle provokes a single event and is given by the following equation:

$$\sigma = \frac{\text{number of events}}{\text{fluence}} \quad (2.2)$$

The cross section is usually presented graphically. The obtained curve is basically characterized by two parameters (Fig. 2.3). The first is the LET threshold, which is the lowest LET required to trigger an event in the device. The second is the saturation cross section, that indicates the maximum value of the device cross section and therefore is an approximated value of the total sensitive area of the device.

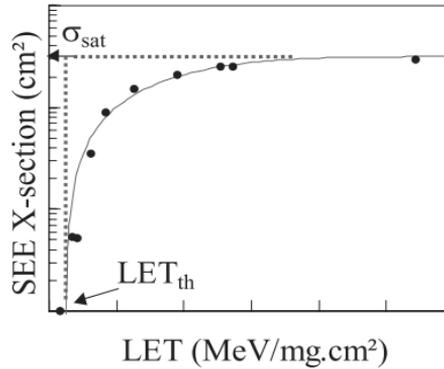


Fig. 2.3. Cross section curve.

The heavy ion cross section can be fit using a Weibull distribution [Pet92] with width (W) and shape (S) parameters. The curve shape equation is the following:

$$\sigma = \sigma_{sat} \left[1 - \exp \left\{ - \left(\frac{LET - LET_{th}}{W} \right)^S \right\} \right] \quad (2.3)$$

2.4.2 SER

The SER (Soft Error Rate) is the rate at which soft errors appear in a device for a given environment. The SER is given in FIT (Failure In Time). A FIT is equal to a failure in 10^9 hours. The SER can be calculated using

the cross-section. If with a fluence of N neutrons/cm² n errors are obtained, then the cross-section is $\sigma = n/N$. With a particle flux in the real Φ environment, expressed in n/cm²/h the FIT value is:

$$FIT\ value = (n/N) \cdot \Phi \cdot 10^9 \quad (2.4)$$

Advanced processors can have an SER exceeding 50000 FIT, being equivalent to about one failure every two years.

2.4.2.1 Critical charge

The critical charge Q_{crit} is a parameter describing the sensitivity of memory circuits to transient effects. It is defined as the minimum charge disturbance needed to change the logic level of a node in a memory circuit. An initial approach to compute this parameter consists in the critical charge as the product of the total capacity C_i at a given node by the power supply voltage V_{dd} : $Q_{crit} = C_i \times V_{dd}$. With this approach a rough estimation of the critical charge is obtained although it provides a wrong value when carrier collection is due to diffusion.

A more precise approach to obtain the critical charge uses a circuit simulator and describes the collected charge by a double exponential current generator of short duration applied at the sensitive node [Mav07]:

$$I = \frac{Q_{tot}}{\tau_f - \tau_r} (e^{-t/\tau_f} - e^{-t/\tau_r}) \quad (2.5)$$

The curves obtained using this approach are shown in Fig. 2.4. The charge is computed as the integral of the current pulse. In this approach, the peak amplitude dependence with the node voltage is not considered. A more precise approach consists in using a 3D device simulator of the whole device or a mixed mode simulator that describes the struck transistor with a device simulator and the rest of the transistors with a circuit simulator. With this

approach more precise current curves are obtained. Although better results are obtained using a device simulator, this option is more complex and time consuming. Therefore the double exponential approach is used in many works found in the literature.

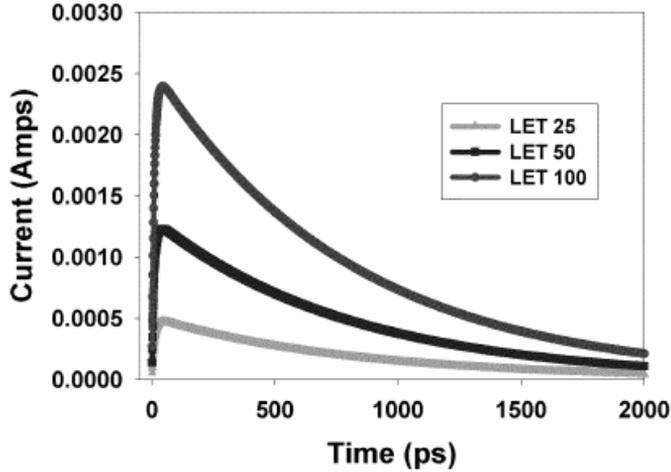


Fig. 2.4. Current pulses obtained using a double exponential [Gad04].

2.4.2.2 Mean time to failure (MTTF)

Is the expected time during which the circuit will operate correctly. It can be computed as:

$$\int_0^{\infty} R(t) dt \quad (2.6)$$

where $R(t)$ is the system reliability, or the probability that it operates correctly in a given time interval.

2.4.2.3 Mean time between failures (MTBF)

Is the mean time between two system failures. It can be computed as the ratio of a given time interval to the number of failures occurred in that interval.

2.4.2.4 Mean time to repair (MTTR)

The MTTR can be computed as:

$$\frac{\sum_i^N t_i}{N} \quad (2.7)$$

where t_i is the time required to repair i^{th} failure and N is the total occurred failures.

2.4.3 Cumulative effects

A constant exposure to radiation produces stable and long term changes in device's characteristics that may result in parametric degradation and functional failures. Cumulative effects can be divided in two categories: Total Ionizing Dose (TID) and displacement damage.

2.4.3.1 Total ionizing dose

This effect is due to ionizing particles, mainly protons and electrons, and provokes cumulative long term damages. It primarily affects insulating layers, which may trap charge or produce interface changes. In MOS devices,

trapped charges can lead to a shift in the gate threshold voltages, increasing significantly the leakage currents. Ultimately, TID provokes permanent functional failures of the device [Sch08].

2.4.3.2 Displacement damage

Non-ionizing energy loss results in displacement damage and defects in both insulator and semiconductor regions. This energy deposited by striking particles displaces atoms and creates electrically active defects. The overall effect of displacement damage is a change in the minority carrier lifetimes of semiconductors.

2.4.4 Single-Event effects

Single-Event Effects (SEE) occur within combinational and sequential circuits caused by the impact of a single particle on a sensitive area of the circuit. The consequences of SEEs vary from transitory effects to a permanent damage. The main SEEs are described in this section.

2.4.4.1 Single-Event Upset (SEU)

Is a temporary event that impacts memory circuits. An SEU occurs when an event changes the state of a memory element. After the event the affected devices still operate correctly.

An SEU occurs when a particle strikes a memory element and it deposits a charge amount larger than the critical charge. The memory state is inverted and maintained until a new value is written. SEU mechanisms differ depending on the class of memory elements [Dod03].

2.4.4.2 Single-Event Transient (SET)

Is a temporary event that impacts combinational circuits consisting of a spurious signal caused by a particle strike in a sensitive node, that can propagate through the circuit and eventually reach a memory element causing an SEU.

2.4.4.3 Multiple-Bit Upset (MBU) and Multiple-Cell Upset (MCU)

Are multiple transitory failures caused by a single event. Multiple errors can be created in devices when a particle crosses the sensitive zones of various cells or when the free carriers of the ion track can be collected by different junctions of transistors. As the transistors density is increasing with each new technology generation, the probability that a single particle generates a transitory failure in many memory elements is increasing. If various bits of the same word are affected, the failure is called MBU, whereas an MCU takes place when the affected cells do not belong to the same word.

2.4.4.4 Single-Event Functional Interrupt (SEFI)

Is a soft error that causes a component to reset, lock-up or other detectable temporal malfunction [Kog97], its effects are not destructive and the system fully recovers its functionality after a reset. An SEFI is often associated to an upset in a control bit or register.

2.4.4.5 Single-Event Latch-up (SEL)

Occurs in single-well CMOS technologies when the charge generated by the ionizing particle activates parasitic bipolar transistors formed between the

substrate and doped regions of the transistors, establishing an open path between supply and ground causing a short-circuit. It is necessary to cut the supply off to eliminate this failure. SELs can represent a serious problem because large currents can be generated which can damage permanently the circuit.

2.4.4.6 Single-Event Burnout (SEB)

The SEB occurs mainly in power MOSFETs when the parasitic bipolar junction transistor (BJT), inherent to the MOSFET structure, turns on and becomes conductive due to a particle strike. If the current induced at the emitter-base junction of the BJT is high enough it may provoke a local overheating able to destroy the device [Har07], [Sex03], [Tit13].

2.4.4.7 Single-Event Gate Rupture (SEGR)

The carriers generated by a particle can accumulate beneath the gate oxide, increasing the electric field across the gate dielectric. This reduces the recombination causing an increasing number of trapped carriers in the oxide, increased leakage and the breakdown of the oxide [Sex03].

2.5 Mitigation

This section is devoted to list the mitigation techniques applied at different levels (process, layout and circuit) used to reduce radiation effects.

2.5.1 Mitigation at process level

The techniques adopted at process level consist in modifying the standard manufacturing processes and can be achieved by several means such as modifications of doping profiles in devices and substrates, optimization of deposition processes for insulators and use of specific materials.

2.5.1.1 Epitaxial layers

An epitaxial layer is a lightly doped layer structure grown over the highly doped substrate [Dod94]. The lower substrate resistance reduces the formation of PNPN paths and therefore the risk of SEL. Such a structure also favors a rapid recombination of the charge generated in the substrate [Roc05] which limits the collected charge due to particle strikes. Fig. 2.5 shows the difference in charge collection between epi and bulk structures.

2.5.1.2 Silicon on insulator (SOI)

SOI technology comes from the idea of separating the active layer from the silicon bulk. It is accomplished by constructing the transistors on a silicon layer, called buried oxide (BOX), over the silicon substrate [Sch03]. SOI provides SEL immunity because the parasitic thyristor cannot be formed due to the isolation of the wells. SOI has also less charge collection volume compared to bulk technology, being less likely to experience currents capable of changing the logical value of a node.

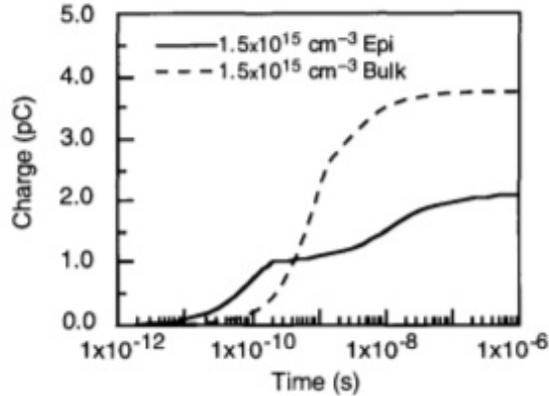


Fig. 2.5. Integrated charge collection in epi and bulk structures [Dod94].

2.5.1.3 Triple wells

Extra doping layers can be introduced to reduce charge collection at critical nodes. Thus, in a single-well process an n-well in a p-type substrate is used to build a PMOS transistor. The twin-well process uses a lightly doped substrate that is either p-type with p-wells for NMOS transistors or n-type with n-wells for PMOS transistors. In the triple well process, assuming a p-type substrate, the PMOS transistors are constructed in an n-well, however the p-well of the NMOS devices is constructed within a deep N-well. This means that both device types are isolated from the substrate by a reversed biased junction. Triple wells reduce the SER sensitivity as the electrons generated deep inside the substrate are more efficiently collected by the extended n buried zone and then better evacuated through n-well ties.

2.5.1.4 Buried layers

Buried layers are, generally highly doped zones buried inside the well or substrate placed beneath sensitive nodes, like storage nodes. They collect or repel excess charge deposited by particles, diverting it from the devices on

the surface. Buried layers are effective for eliminating SEL and for reducing diffusion current components responsible for MBUs in SRAMs. It will also prevent SRAM critical nodes from collecting diffusion currents from strikes at distant positions [Mav07].

2.5.2 Mitigation at the layout level

In this section the mitigation techniques with respect to the effects of radiation that can be applied at integrated-circuit layout are presented. They are based on modifying the transistor's shapes and inserting protection elements.

2.5.2.1 Enclosed layout transistor (ELT)

Standard transistor layout does not prevent the occurrence of the TID leakage currents. ELT is a special layout style with an inner diffusion surrounded by the transistor gate and an outer diffusion (Fig. 2.6). ELT provides the elimination of the parasitic paths because the drain is placed inside the gate.

2.5.2.2 Guard rings

Guard rings consist in surrounding n-channel devices with a p+ guard ring and p-channel devices with a n+ guard ring. It prevents leakage between adjacent devices and protects from SEL because the gains of parasitic NPN and PNP transistors are significantly decreased by p+ and n+ rings respectively.

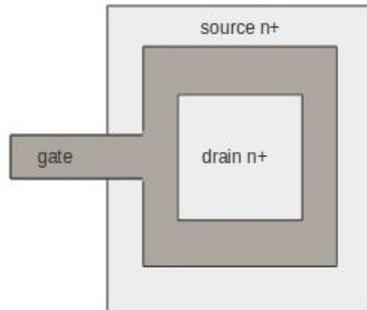


Fig. 2.6. Layout of ELT

2.5.3 Mitigation at the circuit level

At this level, the mitigation techniques consist in adding or modifying elements of the circuit or system.

2.5.3.1 Spatial redundancy

These techniques consist in replicating logical blocks performing the same task such that if one of the blocks fails, it is possible to detect and correct it. The most used technique is to replicate N times the block to be hardened and perform a majority voting to get the correct output. This technique doesn't detect failures but just mask them and is therefore called a passive technique. Active techniques detect failures and then recover the system. These techniques assume a non-correct operation while the circuit is reconfigured. An example of this technique consists in duplicating a block. The two blocks work in parallel and their outputs are compared. If the outputs are different an error message is generated. To correct the failure a spare block is used. The spare blocks can work in parallel or be inactive until the failure is detected, obtaining a less consumption.

2.5.3.2 Temporal redundancy

These techniques require extra hardware elements. There are two ways of implementing temporal redundancy. The first one is to repeat the calculations at different times and then compare the results (Fig. 2.7). If the values computed at different times match up then there is no failure.

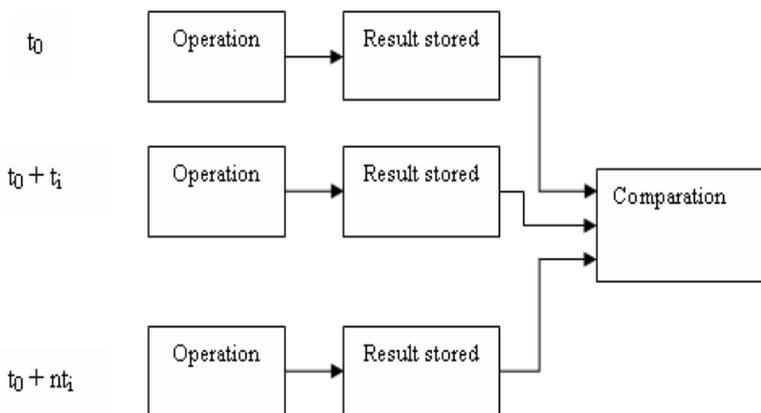


Fig. 2.7. Temporal redundancy computing data at different instants.

The second consists in storing data at different times (Fig. 2.8). In this technique data is stored at instants with a given delay, Δt , and only pulses shorter than Δt can be detected. For any pulse shorter than Δt only one of the three bistables will present a wrong value and therefore the correct value is shown at the output of the voter.

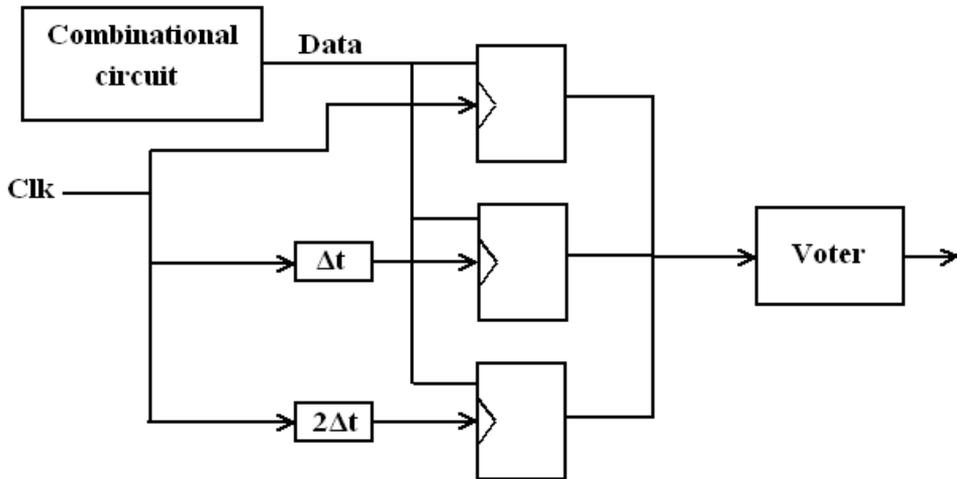


Fig. 2.8. Temporal redundancy storing data at different instants.

2.5.3.3 Information redundancy

It is possible that a part of the information in a circuit suffers a failure, for example the change in a bit value. This information can be considered valid although it contains wrong data. Therefore a mechanism that detects if the information is valid is necessary. The used mechanisms add redundant information using error detection codes (EDC) or error correcting codes (ECC). These techniques can be based on their Minimum Hamming distance. The Hamming distance between two data strings with the same length is the number of different bits between two data.

2.6 Radiation emulation

Determining the sensitivity of an electronic circuit to a specific radiation type requires exposing it to the specific radiation of interest, or emulating its effects through alternative techniques. In the first case, it can be done through either what is called real-life test or by accelerated test, while

radiation emulation is typically done by using a pulsed laser.

2.6.1 Real-time test

Real-time measurement is an experimental technique to determine the SER by monitoring a device subjected to the natural radiation environment and operating under nominal conditions. These tests can be performed at scientific satellites [Dye96], stratospheric balloons, or at ground level without any limitation due to weight or power consumption. This technique provides the most accurate results since the circuit is exposed to the real conditions of radiation. However, the experiments in real conditions require exposure times extremely large because of the low fluencies in the real environment, involving a high cost. These important limitations make other techniques preferred.

2.6.2 Accelerated test

Accelerated test methods consist in replicating the effect of the particles on a circuit assuming that normally it is not possible to obtain identical radiation characteristics, such as energy and LET, that the circuit will be actually exposed to. These methods are performed at facilities such as synchrotrons or linear accelerators that provide high fluencies of particles and, therefore, require a lower time effort compared to natural conditions. With the accelerated methods, it is not possible to obtain particles with identical energy and LET than in the real environment, hence it is necessary to calibrate and characterize the radiation sources used to provide particles with similar characteristics than the particles in the real environment.

2.6.3 Laser emulation

Another way to emulate the effects of energetic particles generating single event effects in ICs consists in using a pulsed laser. The main advantages of using a laser are the spatial and temporal resolution as it allows focusing and synchronizing the laser pulse and it has no radiation constraints such total dose ionization or displacement damage, and it also has a high penetration depth (hundreds of μm). If the laser energy can be controlled, then it is also possible to emulate a wide range of heavy ion LET values. The relationship between the laser parameters and the heavy ion characteristics is not straightforward but the studies in several works have obtained the optimal laser characteristics to emulate radiation effects [Mcm99], [Pou01], [Fou04], [Lop09], [Lop11], [Chu11], [Pal09a], [Pal09b], [Pal12].

The light absorption by a semiconductor is given by the following equation [Buc13]:

$$\frac{dI(r, z)}{dz} = -\alpha(\lambda)I(r, z) - \sigma_{ex}NI(r, z) - \beta(\lambda)I^2(r, z) \quad (2.8)$$

With r and z being the radial and longitudinal positions, respectively, $I(r, z)$ the irradiance of the laser pulse, $\alpha(\lambda)$ and $\beta(\lambda)$ are the one-photon and two-photon absorption coefficients, respectively, σ_{ex} the cross-section for photon absorption by free electrons, and N is the free carrier density. The term related to the absorption by free electrons is often neglected.

If the laser energy is larger than the bandgap of the silicon, photons are absorbed directly generating e-h pairs (SPA or single photon absorption). A laser energy larger than the bandgap implies a wavelength lower than a certain value. In the case of silicon, $\lambda < 1107$ nm is the condition for SPA. In that situation the first term of equation (2.8) is the dominant, obtaining the solution:

$$I(z) = I_0 \exp(-az) \quad (2.9)$$

The linear absorption coefficient α depends on the wavelength. It is larger for smaller wavelengths. Equation (2.9) implies that the maximum charge deposition takes place at the surface. If the laser impacts the circuit on the front side, the light may be reflected or absorbed by the metal layers, which in current technologies represent a significant barrier. The solution requires performing the laser test from the backside but it doesn't assure that the laser reaches the sensitive zones because of the substrate thickness. An alternative to this approach is a backside attack with substrate thinning. Another alternative is to use the two-photon absorption (TPA).

For energies lower than the bandgap, the non-linear term is dominant and, neglecting the free carrier absorption, the solution to (2.8) is:

$$I(z) = \frac{I_0}{1 + \beta(\lambda) I_0 z} \quad (2.10)$$

Equation (2.10) shows that the absorption depends on both the material and the laser intensity. For large intensities, e-h pairs can be generated by two-photon absorption (TPA). The maximum absorption takes place at a certain distance from the surface depending on the confocal distance where the irradiance is high [Mcm02], [Fou07], [Buc13]. It means that using this technique the charge can be injected at any depth depending on the focusing depth of the beam.

Fig. 2.9 compares SPA to TPA charge generation. With the SPA technique the beam is focused at the surface while with the TPA the beam is focused at about 20 μm from the surface.

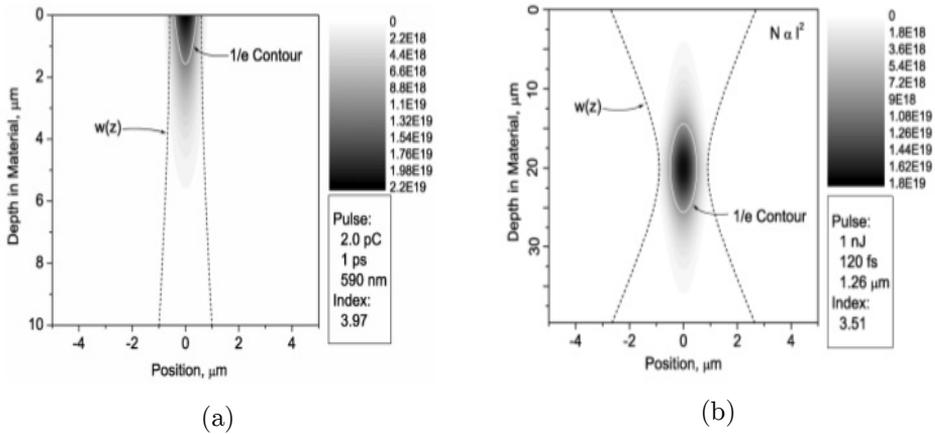


Fig. 2.9. Comparison between the charge generation zones for SPA (a) and TPA (b) [Mcm02].

In general, the charge track generated by TPA is more similar to the track generated by a heavy ion than the track generated by SPA and offers more experimental options. Nevertheless, depending on the experiment to be developed, such as a direct impact on the surface without metal layers, SPA is a valid technique to generate soft errors. For instance in [Sch11a] the charge generated at SOI diodes with the substrate removed using SPA shows a correlation with the charge collected using TPA. And in [Sch11b] SRAMs with the back substrates removed show a reasonable quantitative agreement in the charge collection from TPA and SPA for equivalent deduced heavy-ion LET.

The basic laser characteristics required to emulate the effects of a specific radiation type are the pulse duration, the impact diameter, the pulse energy and the wavelength [Lop11].

2.6.3.1 Pulse duration

To emulate the effect of a particle, the time that the laser takes to generate a certain amount of charge has to be similar to the time that the particle

travels through the sensitive volume. This time is of the order of femtosecond or picoseconds. It implies the use of pulsed lasers.

2.6.4 Pulse radius

It determines the zone of charge generation. The photon density follows a Gaussian distribution, and the radius is defined as half the width of this function at $1/e^2$ of its maximum. The radius is minimum at the focal point and diverges for points before and after this location. There is a relation between the ion energy and the radius of the laser beam:

$$E(\text{MeV}) = A(\text{amu}) \left(\frac{W_0(\mu\text{m})}{0.3} \right)^{\frac{1}{0.427}} \quad (\text{Single photon}) \quad (2.11)$$

$$E(\text{MeV}) = A(\text{amu}) \left(\frac{W_0(\mu\text{m})}{0.43} \right)^{\frac{1}{0.427}} \quad (\text{Two photons}) \quad (2.12)$$

2.6.4.1 Pulse energy

The pulse energy determines the number of e-h pairs generated in a given volume and, therefore, the generated charge. Knowing the deposited charge by an ion, the pulse energy to generate the same amount of charge with the laser can be obtained.

2.6.4.2 Wavelength

The wavelength determines the energy of the photon and, therefore, the capability to generate e-h pairs. If the photon energy is larger than the bandgap the photon generates an e-h pair. If the energy is below the

bandgap an e-h pair can also be generated if the electron absorbs two photons.

Regarding the generation of SEUs and SETs, several previous works used the laser technique. In [Buc93] a laser pulse synchronized with the clock signal was used to generate SEUs in a GaAs circuit. In [Buc97] SEUs and SETs were observed obtaining the interesting result that at low frequencies most errors were due to SEUs while when frequency was increased SETs became important due to the increasing capture probability. In [Mcm99] SEUs were obtained using a laser for circuits fabricated in 0.8 μm , 0.5 μm and 0.25 μm technologies, obtaining a correlation with heavy ion results. In [Kob08] SETs with a width of about 0.6 ns were obtained using a laser on a 0.2 μm FDSOI inverters. In [Fer07], [Fer08], [Fer09] a laser was used to generate SETs in chains of inverters observing the pulse broadening effect. More recently [Zha14] the threshold laser energy required to generate an SET in a chain of 100 0.18 μm PDSOI CMOS inverters has been measured.

Chapter 3

Single-Event Transients

When a particle strikes a combinational logic block, the collected charge may induce a voltage transient at the struck node. This is called a Single-Event transient (SET) and implies a temporal change of the logic state. An SET pulse itself doesn't represent a problem unless it is capable of propagating through a circuit output reaching a memory element. In this case the SET becomes an SEU. Four criteria must be met for an SET to produce an SEU:

1. The generated SET pulse must have specific conditions to propagate electrically through the circuit. If these conditions don't meet, the pulse is masked electrically. Electrical masking occurs for transients with a small duration or small height since they will be then attenuated.
2. There must be at least one open logic path arriving to a memory element.

If this condition doesn't meet, the pulse is logically masked. Logical masking occurs when a particle strikes a part of a combinational circuit that cannot affect the output due to a subsequent gate having a dominant logic value at any of its other inputs. For example, if there is a strike impacting an input of a NAND gate having any other zero then the strike will be completely masked and the output will be unchanged. Therefore the particle strike will not cause a soft error.

3. The width and amplitude of the SET pulse after traveling the circuit must be sufficient to change the state of a memory element.
4. The SET must reach a memory element when it is transparent. If the pulse doesn't reach the memory element while it is capturing an input, it is said that the particle is filtered due to temporal masking.

The first part of this chapter is aimed to detail the most important aspects regarding the study of SETs such as generation and propagation going through the different approaches published in the literature. In the second part the SET propagation model developed in this work is presented along with relevant results. The model is validated against electrical simulations.

3.1 Overview

SETs were predicted [Die84] and observed [Fri85], [Kog87] 30 years ago in the arithmetic logic unit of a microprocessor. In the 90's various experiments detected SETs in several technologies but the sensitivity of circuits to SET was difficult to simulate due the extensive computer resources required. At that point, new SET modeling and simulating works appeared and new experimental techniques were developed. The most relevant are described in this chapter. These new techniques applied to every new CMOS technology have revealed that SETs are becoming a major concern regarding radiation effects in ICs with technology scaling. First, a decrease of the node capacitances causes an increase of the resulting SETs width thus making its

generation more probable. Second, faster gates imply that narrower pulses may traverse the logic elements making SET propagation also more probable. And finally, higher frequencies increase the probability that an SET reaches a memory element when it is transparent, becoming the most important source of errors as frequency increases (Fig. 3.1).

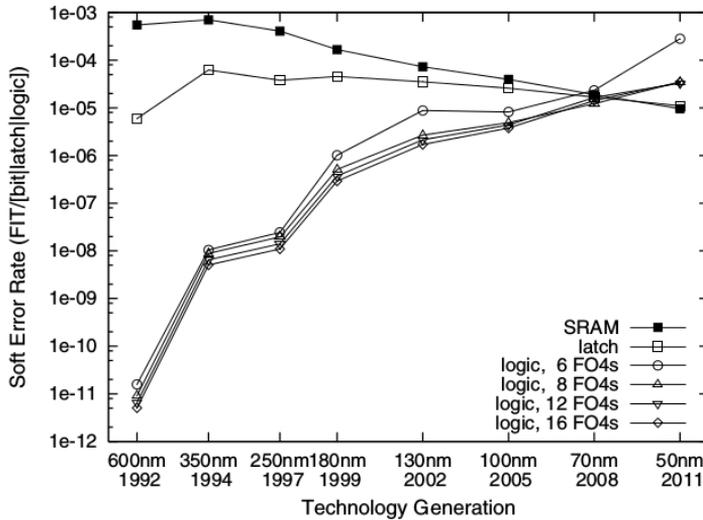


Fig. 3.1. Relative impact of SET (logic) vs. SEU (latch,SRAM) [Shi02].

3.1.1 SET generation

Understanding the SET generation mechanisms is key to estimate the range of possible voltages and widths. Simulation/modeling and experimental approaches can be performed to analyze this process. Simulation consists in computing numerically 3-D equations for charge transport based on drain-diffusion models. This is only done for the struck device while the rest of the circuit is simulated within the circuit domain [Dod04], [Fer06], [Ful07], [Kob07], [Mak09]. This approach is called Mixed-Mode 3D device simulation and was used to observe the SET shape for several LET values in [Dod04] for both bulk and SOI 0.18 μm CMOS inverters. It is important in this

approach to not simulate the struck transistor alone connected directly to V_{dd} but to include it in an inverter because the current generated is different for each case as shown in Fig. 3.2. Using Mixed-Mode 3D device simulations in [Tru08] the SET production was studied regarding temperature and strike position obtaining wider SETs at higher temperatures.

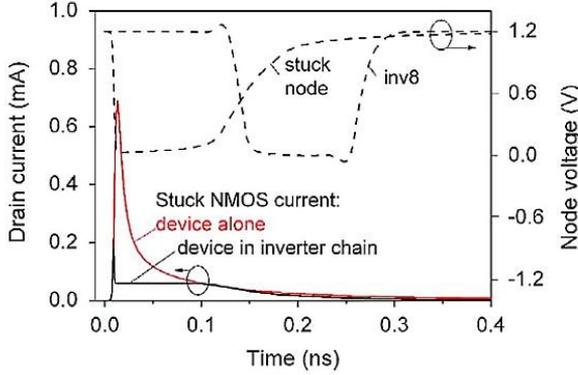


Fig. 3.2. Current at the struck transistor simulated alone and integrated in an inverter chain [Fer06].

Another way of studying the SET generation consists in modeling the impact of a particle through a current source connected at the impacted node. In [Wir05], [Wir06] and [Wir07] a particle strike at the drain junction of the p-transistor of an inverter is modeled as a simple RC circuit. The current due to the collection of the released charge was modeled with a double exponential current pulse source $I_p(t) = I_0(e^{-t/\tau_a} - e^{-t/\tau_\beta})$ where I_0 is the maximum charge collection current, τ_a the collection time constant and τ_β the ion-track establishment time constant. The parameters that determine this current source characteristics depend on the simulated particle and on the technology, and must be determined. Solving the RC circuit expressions for the voltage, the width and critical charge of the generated SET are obtained.

In [Ros09] a simplified RC model was used to calculate the critical charge Q_{SET} required necessary to produce a voltage glitch with an amplitude exceeding the fan-out logic threshold. A rectangular current source was used

to simulate the pulse induced by a particle strike. The resultant expression for Q_{crit} depends on the transistor conductance and on the total node capacitance. Then assuming that both conductance and capacitance can be expressed in terms of the transistors channel widths, a linear dependence of Q_{SET} on transistors widths was obtained.

In [Dhi07] Spice simulations were performed in order to calculate the width of the generated transient. A trapezoid current waveform was used and parameters such as delays, V_{dd} , V_{th} and load capacitances were varied to construct look up tables for the width of the generated transient.

Sub circuit models are also used to model a particle impact. In [Mav07], [Mak08], [Kau09] different models are developed using SPICE components.

The SET pulse widths observed experimentally vary depending on the type of radiation, the LET and the technology. SETs caused by heavy ions with pulses values from 200 ps to more than 1 ns have been measured in [Eat04] for a 0.18 μm technology. In [Ben05] similar results were obtained for the same technology: 344 ps to 1.5 ns. In [Fer06] pulses of 65-235 ps were measured for a 0.25 μm SOI technology. SETs in more recent technologies have been measured in [Nar07]: 400-700 ps for a 130 nm technology and 500-900 ps for 90 nm.

Neutrons have also been used to produce SETs. In [Nar08a] widths ranging from 300 ps to 1.4 ns were measured for a 90nm technology. In [Nak10] widths up to 600 ps were obtained for a 90nm technology and in [Nak12] SETs of 63-109 ps for a 90 nm technology and 38-150 ps for a 40nm technology were measured.

SETs generated by protons impact have been also measured too. In [Can09] widths up to 132 ps were obtained for NAND and NOR gates from a 90 nm library.

Irradiation with alpha particles also generates SETs as in [Nar08a] where pulse widths up to 1.1 ns were measured in a 90 nm inverter chain and in [Gad11] widths of less than 75 ps were detected for a 65 nm bulk inverter chain.

Pulsed lasers are typically used to emulate radiation. In [Kob08] a width of about 400 ps was found for a 0.2 μm FDSOI single inverter. In [Gou08] SETs of 800 ps were measured for a 0.18 μm FDSOI inverter chain while in [Fer07] SETs ranging from 200 ps to 2 ns were obtained due to pulse

broadening in a 0.13 μm SOI inverter chain.

Given the reduced dimensions achieved in current technologies it is likely that a single particle impact generates charge collection at multiple nodes of the device. A multi-node charge collection was observed in [Amu06], [Nar08b] showing that charge collection increases as the distance between nodes decreases. In [Nar08b] two devices were simulated on a 90-nm technology. A heavy-ion strike on the primary device was simulated but due to charge collection on both primary and secondary devices an SET may be generated at both. These two SETs may converge on a node and a wider SET may be created. Such SETs are called extended SETs (E-SET). Another effect of charge sharing was studied in [Ahl09]. In a chain of inverters a particle strike can generate an SET at an inverter that will be quenched at the next inverter due to charge sharing. For example, if the input of the first inverter is high, a particle impact at the off pMOS transistor of the first inverter generates a high SET at the output that is also the input of the second inverter. It appears as a low SET at the output of the second inverter. When the input of the second inverter is high, charge can be collected at the off pMOS of this gate driving the output of the second inverter high and truncating the SET. Therefore, the SET observed at the output is shorter than the generated SET. This study is extended in [Hua14], the transistor of one more inverter in the chain is added to the charge collection. The effect at the third inverter is the broadening of the SET obtaining a wider SET at the output than the one generated two gates behind.

3.1.2 SET propagation

The propagation of a pulse through a combinational circuit depends on the capability of the pulse to propagate through each logic gate within the path. At gate level, the propagation depends on both the pulse characteristics and the gate physical parameters. A minimum pulse duration and height are required for an SET to propagate through a logic gate. The minimum pulse duration is related to the gate delay. If the pulse is shorter than the time

that the gate needs to complete a transition, then the pulse will not propagate. The SET minimum voltage is related to the logic gate threshold voltage, that depends on the transistors thresholds and drive strengths. The node capacitance also plays a significant role in SET propagation. Lower capacitances imply faster gate response and, therefore, shorter pulses are capable of propagate. Another relevant parameter is the supply voltage, either for SET propagation or generation. [Ben06], [Gad07] observed experimentally increasing SET cross-sections and widths with decreasing supply voltage. Fig. 3.3 shows the mentioned cases.

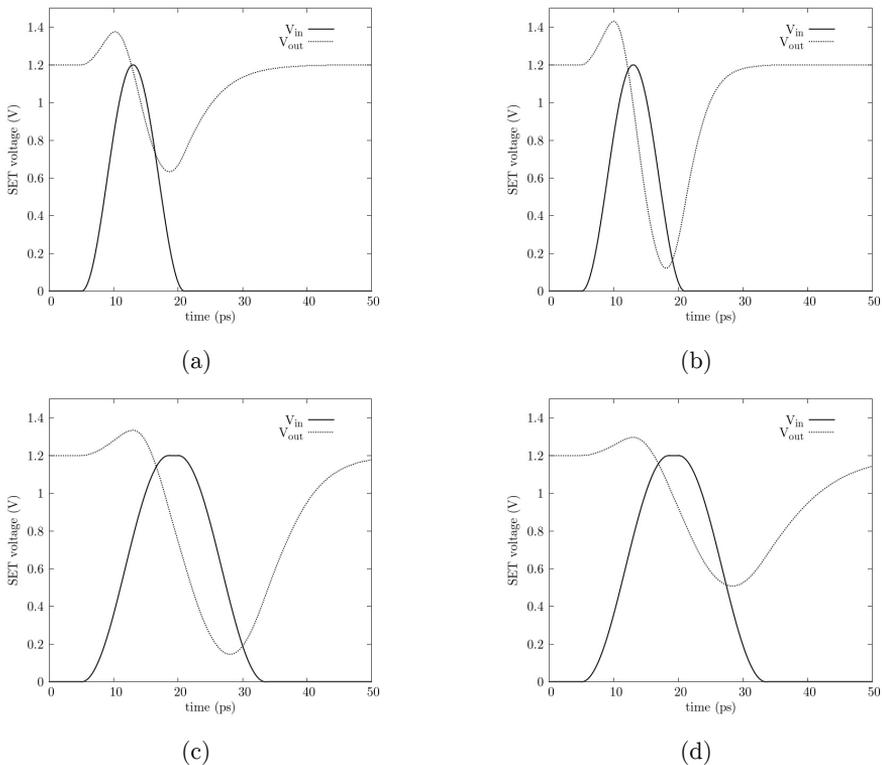


Fig. 3.3. Gate response to an SET for different cases.

In (a) an SET shorter than the delay of the gate is injected and is not propagated. In (b) the same pulse is injected at a faster gate with a shorter delay time and is propagated. In (c) a wider pulse is injected in the same

gate than in (a) and is propagated. And (d) shows the same situation than (c) but with a larger output load, obtaining an attenuated output pulse.

The ideal scenario for a rigorous and feasible SET propagation study would consist in having a closed-form equation describing the output waveform as a function of the input. This approach has not been achieved given the non-linearity of the equations governing the transistors operation processes. However, there are some analytical approximations describing the transient response of the inverter to an input transition [Kay92], [Bis98], [Wan09]. The complexity of equations increases with complex gates different from inverters. Therefore the most common approach is to model the response of gates to an SET instead of trying to solve equations for the currents to obtain the SET waveform. In [Kau91] an approximate set of closed-form equations was obtained to compute the output voltage response of a gate to an exponential input voltage. Different equations were obtained for different values of the input voltage. Realistic pulses were then fitted to this exponential input voltage and the output pulse was obtained. This operation was repeated for each gate of the path. In [Mol92] the penetration of a spurious signal with given height and width in a chain of identical CMOS inverters was investigated. At each k -level penetration (k being the number of inverters that the spurious signal is able to propagate) a critical curve was constructed. The critical curve represents the relationship between height and width of the pulses that produce a signal with an amplitude equal to the threshold voltage at the k th stage. For the case $k=1$ an analytical expression was obtained using Sah equations. This expression was divided in three regions depending on the height of the input pulse. The study was extended to any value of k using numerical methods to solve Sah equations. In [Dod04] the propagation as a function of the LET was studied by simulation in a chain of ten $0.18\ \mu\text{m}$ bulk CMOS inverters. For a LET of $3\ \text{MeV}\cdot\text{cm}^2/\text{mg}$ the produced SET did not propagate through all the inverters of the chain, and it was completely attenuated after the fourth inverter. For a LET of $7\ \text{MeV}\cdot\text{cm}^2/\text{mg}$ the SET propagated through all the chain without attenuation. An estimation of the critical transient width was also given. The critical width is the minimum width for unattenuated propagation. The critical LET (minimum LET for unattenuated propagation) is estimated as well for both bulk and SOI technologies. A decrease of the critical LET with

technology scaling is observed in both cases and for the 100 nm bulk technology a critical LET below $2 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ was found. This means that it is sensible to alpha particles, one of the most abundant reaction products for proton and neutron interactions in Si.

In [Dhi07] the propagation was computed as a result of two processes: logical and electrical masking. In the logical masking the probability of a path between two gates to be sensitized was computed. In the electrical masking the propagation through a gate was given by the following expressions:

$$\begin{aligned} w_0 &= 0 \text{ if } w_i < d \\ w_0 &= 2(w_i - d) \text{ if } d < w_i < 2d \\ w_0 &= w_i \text{ if } w_i > d \end{aligned}$$

where d is the delay time of the gate. The method used requires computing sample values of the output width for several input widths that are used to compute the actual output width by interpolation. The method combines the expressions shown above with the interpolation of the sample values to determine the width of the propagated SET at an output of the circuit.

In [Mas08] SET propagation through a chain of inverters was studied. At

each node the equation $\frac{dV_o}{dt} = i_p - i_n$ has to be solved, where i_p and i_n are

substituted by the Schokley's equations for the pmos and nmos transistors respectively. The equation is normalized so that it does not depend on the technology, only on the circuit characteristics. The differential equations obtained are solved numerically at each node and the pulse characteristics are obtained.

In [Wir05], [Wir06] and [Wir07] the SET propagation was computed by the propagation through every gate in the circuit. The width at the output of a gate is computed as a function of the width at the input and then the output of a gate taken as the input of the next gate in the circuit. The width at the output of a gate was computed with analytical expressions divided in regions depending on the input width:

$$\begin{aligned}
\tau_{n+1} &= 0 \text{ if } \tau_n < k \cdot tp \\
\tau_{n+1} &= (k+1)tp \left(1 - e^{-(\tau_n/tp)}\right) \text{ if } k \cdot tp < \tau_n < (k+1) \cdot tp \\
\tau_{n+1} &= \frac{\tau_n^2 - tp^2}{\tau_n} \text{ if } (k+1) \cdot tp < \tau_n < (k+3) \cdot tp \\
\tau_{n+1} &= \tau_n \text{ if } \tau_n > (k+3) \cdot tp
\end{aligned}$$

where τ_n and τ_{n+1} are the input and output widths, tp is the delay time of the gate and k is a parameter that depends on technology and has to be determined.

In [Fir10] analytical equations relating output to input pulse fall and rise times are obtained. The output pulse width and height are given as a function these fall and rise times. Non-realistic squared and trapezoidal input pulses are used.

3.1.3 SET broadening

In the study of SET propagation the phenomenon of pulse broadening has been observed [Fer07], [Mass08], [Wir08]. Pulse broadening is an effect observed in inverter chains that consists of an increase of the width of the pulse as it travels through the chain. Two mechanisms have been identified as a source of broadening effect. The first one is load asymmetry: if the response of a gate to the first pulse transition is fast, but the response to the second transition is slow, then the output pulse will be larger than the input pulse. On the contrary, if the response of the second transition is faster than the first one, the pulse at the output will be shorter.

The second mechanism is the asymmetry due to threshold hysteresis. This effect has been observed in SOI circuits [Suh94], [Wei96] showing that the transient characteristics of SOI transistors may be affected by its recent history. The body-source voltage (V_{BS}) is modulated by the charge state in the body, which is affected by slow time constants and thermal generation and recombination lifetimes in the floating body region. Quiescent conditions govern this charge state. It affects V_{BS} , which in turn modulates

the threshold voltage. A different threshold for rising and falling transitions may lead to a pulse broadening. Since dynamic switching conditions are faster than the time constants associated with the body charge, broadening effects are expected to decrease at high frequencies. This was proved in [Wei96].

Examples of broadening were provided by [Fer07]. A chain of 800 0.13 μm PDSOI inverters was used. SETs generated close to the chain output were about 200 ps wide, whereas 1.8 ns wide SETs generated far away from the output were measured. The broadening factor is only 2 ps per gate. In [Wir08], [Fer07], in order to have a significant broadening, an inverter chain with different fan-out at odd and even nodes is used. Therefore significant pulse broadening can be observed but under very specific conditions as load asymmetry and very long chains, which are not typical real situations in actual logic circuits.

Another mechanism to obtain pulse broadening is the convergence. In [Nar08b] and [Hua14] has been observed that a single particle strike can generate charge collection in two close nodes resulting in two SETs. If the nodes correspond to paths that converge to a node, the two SETs can arrive at this node at a similar instant and be added to generate an extended SET. In [Hua14], moreover, the effect of narrowing after broadening was observed for impacts generating charge collection at three nodes of three consecutive inverters.

3.1.4 SET characterization

The simplest approach to SET characterization consists in measuring the number of SETs produced. The basic idea is to capture the SETs generated in combinational components with a latch. The test structure in [Ben04] consists in a chain of synchronous DICE latch shift registers separated by non inverting buffers (0, 1, 2, or 4) and a latched output. Since the DICE latch is immune to SEU, all the captured events are due to SETs. A similar structure is used in [Ahl08] where the combinational parts are removed from the propagation path between latches so that the logic depth of the

combinational parts don't imply a reduction of the clock frequency.

A more detailed analysis implies measuring the duration of SETs. On-chip and external measurements can be performed. Regarding on-chip measurement several approaches are possible. The first one consists in connecting each output of a chain of logic gates (usually inverters) to a latch. Then the number of affected latches is a measure of the SET width [Nic03], [Nar06], [Yan06]. Fig. 3.4 shows the schematic presented in [Nar06] where a propagating SET affects n inverters at a given instant. For n inverters affected, the SET width is between $(n-0.5)x$ stage delay and $(n+0.5)x$ stage delay. Therefore if the number of affected inverters is known, an estimation of the SET width is obtained. The output of one of the inverters is used as a trigger signal when an SET is detected and this signal is used to trigger the latches to hold the inverters states. This method has been used in many other works [Gou08], [Bal08], [Gad11].

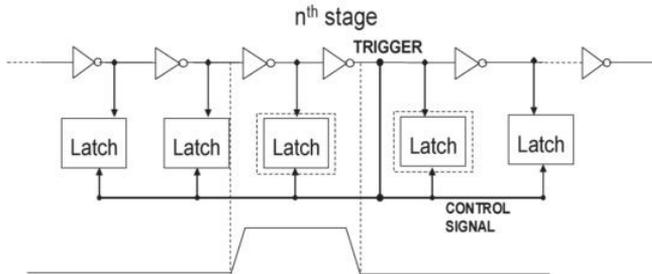


Fig. 3.4. Structure used in [Nar06].

In [Har10] two on-chip measurement techniques are presented. The first one uses a chain of delay elements with different delay values. Each element filters the pulses smaller than its propagation delay. A 1-bit counter is connected to each delay element output. The delays of the last toggled counter and the first not toggled counter establish an upper and lower limit for the width of the SET. The second one uses the Vernier Delay Line (VDL) composed by two buffer chains with different delays and a D-type latch chain. Step signals are sourced at each buffer chain with a given delay. The VDL measures this delay. To measure the width of an SET, two FFs are inserted between the target circuit and the VDL, one capturing the rising

edge of the SET and the other capturing the falling edge.

Another on-chip technique is used in [Eat04] and [Ben05]. A structure with three delay paths and a 3-input majority voter is used. The first path has no added delay, the second has a delay of Δt and the delay of the third path is $2\Delta t$. If the SET width $< \Delta t$ the output of the majority voter is 0, and if the SET width $> \Delta t$ the output of the majority voter is 1 meaning that the SET is detected. Adjusting Δt , the pulse width of the generated SET can be measured.

Regarding external measurements several techniques have been used. The main advantage of these techniques is that the SET waveform can be observed. [Fer08] uses a balanced buffer at the end of the inverter chain. The buffer is designed with large transistors to drive a high-impedance output without modifying the transient signal. The buffer output voltage is measured using a high-impedance probe. This buffer measurement technique can detect signals down to 150 ps. In [Fer09] a detection inverter is placed at the target chain output. The transient supply current is measured through a bias-T with a 50- Ω oscilloscope measurement head. A 010 input voltage pulse results in a 101 pulse at the inverter output. This 101 output pulse applied at the output capacitor induces a derivative current response with first a negative peak on the falling first edge, and a positive peak on the rising second edge. This capacitive current goes through the PMOS transistor and is then read on the oscilloscope measurement head. The distance between peaks is the width of the pulse. Another technique is presented in [Kob08]. The monitoring transistor (MT) technique is based on a structure consisting in only two MOS transistors, one n-type and one p-type, connected to the target output. The drain terminal of each MT is connected to a 50- Ω input of an oscilloscope to monitor the current curves. From these curves the original SET can be obtained.

3.2 SET propagation model

One of the main contributions of this work is the development of a model to describe the propagation of an SET within combinational logic blocks of a circuit. Differently to previous works, the approach presented here is not based on determining the propagated pulse waveform and it is not computed by solving equations describing the currents of the involved transistors. The logic gate is considered in this work as the basic propagation element and, therefore, the model is developed at this level. The SET propagation through a logic gate is analyzed in terms of the relationship between pulse input and output characteristics. Voltage and width are considered as the main pulse characteristic parameters defining the propagation and an analytical relationship is established for each one. Each function describes the gate response to one of these parameters as the pulse propagates through the gate. The response of one parameter depends on the value of the other, thus, the voltage propagation is described as a function of the input voltage and width $V_{out} = f(w_{in}, V_{in})$, and the width propagation as $w_{out} = f(w_{in}, V_{in})$. Fig. 3.5 describes the basic procedure of the model. Each box represents a logic gate and the propagation through it is described with a set of functions $f_k(w_{in}, V_{in})$ that provide the propagated pulse output characteristics. The propagation through a path is computed taking the output characteristics of the pulse for a gate as the input characteristics for the next gate.

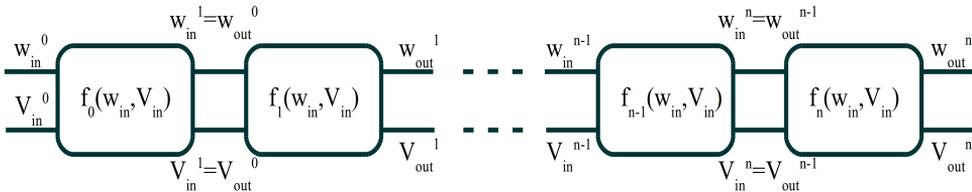


Fig. 3.5. Model scheme.

Two conditions are imposed for these functions to make the model more suitable for CAD environments: analyticity and fully continuous. The choice

of these analytical and continuous functions is based on the observation of the pulses propagation behavior with various characteristics. An expression is then proposed for voltage and width containing parameters that must be determined for each gate. This is done by fitting data obtained from electrical simulations to the proposed functions. The scheme used in the simulation process is shown in Fig. 3.6. A pulse is injected at the input of the gate using a source that is described next, while a load inverter (the minimum sized inverter of the library), fixed for all the library gates, is connected at the gate output. The number of load inverters is changed to account for the output load effect.

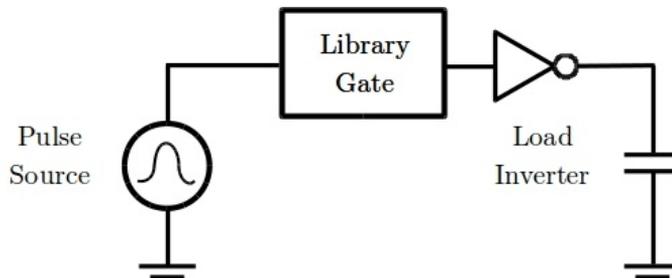


Fig. 3.6. Simulation circuit.

The extraction process is carried by fitting simulated data to the analytical expression using a method based on the Marquardt–Levenberg algorithm [Gre05]. Such algorithm provides a numerical solution to the problem of minimizing a function. In curve fitting, the function that has to be minimal is the sum of the squares of the deviations. The algorithm reduces the problem of minimizing a function onto a set of linear equations. The solutions are the set of parameters to be determined by linearization of the function variation with respect to the parameters.

3.2.1 SET pulse description

The propagation of an SET through a CMOS logic gate depends on both the gate and the SET properties once the logic path is established. In this

work an SET pulse is characterized using two parameters that describe the pulse width and height at each circuit node. The SET height (denoted as V) corresponds to the maximum voltage variation caused by the perturbation at the given node. The SET width (w) is taken as the time interval between the instants when the pulse crosses half the height value (Fig. 3.7). This is known as FWHM (Full Width Half Maximum). Another approach, known as FWHR (Full Width Half Rail), measures the width at $V_{dd}/2$ [Roy08], [Lov12]. Computing the width at FWHR may be a source of error because a pulse with a voltage lower than $V_{dd}/2$ is not considered although under certain conditions, such as fast gates or low loads, it is possible than a pulse that doesn't reach $V_{dd}/2$ traverses a gate. In other works, this is aggravated by considering only pulses that reach V_{dd} , thus neglecting a wide range of pulses that could propagate. On the contrary, with FWHM all pulses are considered independently of their height. Several pulse shapes have been proposed to emulate an SET. A squared pulse is used in [Dhi06], [Mas08], a Weibull cumulative distribution function is used in [Wat12]. Another option is to inject a double exponential current pulse [Wir05], [Moh05], [Wir06], [Wir07]. Since the induced current at the impacted node is asymmetric, a generated SET with an asymmetric shape is also expected, as observed in [Dod04], [Kob07], [Kob08]. Nevertheless, this behavior is restricted to the pulse generated at the impacted node because as the generated pulse propagates through the first logic gate it becomes symmetric due to the symmetric design of the standard cells.

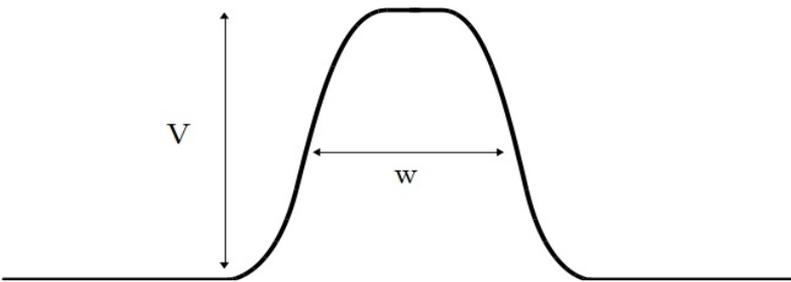


Fig. 3.7. Pulse characterization.

The pulse shape proposed in this work is sinusoidal considering two cases: a

pulse reaching V_{dd} and a non-full V_{dd} . For a full V_{dd} pulse a sinusoidal rise and fall ramp are used while for a non-full V_{dd} the whole pulse is simulated with sinusoidal cycle. For the full V_{dd} pulse a fixed rise and fall times are used and for a non-full V_{dd} pulse the rising and falling times depend on the duration of the pulse as shown in Fig. 3.8. The wider the SET the slower the rising and falling. The pulse is mathematically defined as:

$$V_{in}(t) = \begin{cases} 0 & t \leq t_0 \\ \frac{A}{2} \left(1 + \sin \left[2\pi f \left(t - t_0 \right) - \frac{\pi}{2} \right] \right) & t_0 \leq t \leq t_1 \\ V_{dd} & t_1 \leq t \leq t_2 \\ \frac{A}{2} \left(1 + \sin \left[2\pi f \left(t - t_2 \right) + \frac{\pi}{2} \right] \right) & t_2 \leq t \leq t_3 \\ 0 & t_3 \leq t \end{cases} \quad (3.1)$$

where A is the maximum amplitude, t_0 is the initial time of the pulse and parameters t_1 , t_2 , t_3 and f determine the rising and falling times. With this expression a realistic and totally characterized pulse can be injected at any node.

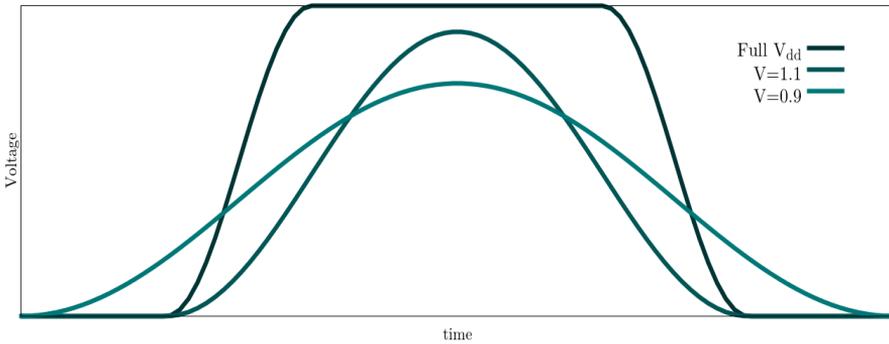


Fig. 3.8. Pulse shapes for full and non-full V_{dd} .

The pulse shape selection is of utmost importance for non-full V_{dd} pulses

because for the same characteristic V_{in} and w_{in} , a squared pulse remains at a high voltage value for more time than a sinusoidal pulse. It means that a square pulse provokes wider propagated pulses.

3.2.2 Height propagation

If the SET voltage is lower than the transistors threshold, then the perturbation is not capable of turning the transistors onto conduction. Therefore such a voltage pulse doesn't provoke a pulse at the gate output and does not propagate. Larger voltage SETs are capable of creating a perturbation at the gate output depending on the input SET actual voltage. Assume a pulse with a given input voltage V_{in} and a long duration w_{in} that propagates through the gate. The output voltage is expected to be also affected by the pulse duration because for shorter pulses the time during which the gate is conducting is shorter and consequently is the time for the output SET to be established.

Fig. 3.9 shows the dependence of the output voltage perturbation (V_{out}) with the input perturbation height (V_{in}) and width (w_{in}) obtained for a 65 nm commercial CMOS technology library inverter. As expected, it is shown that for a given input SET voltage, the output voltage perturbation is higher for wider pulses, specially when the input voltage perturbation is beyond $V_{dd}/2$. The height propagation is described by the model as a transfer function $V_{out}(V_{in})$ for a fixed value of w_{in} . Fig. 3.10 shows transfer functions for three values of w_{in} , as the pulse width decreases, the slope of $V_{out}(V_{in})$ decreases too and the function is displaced to larger values of V_{in} .

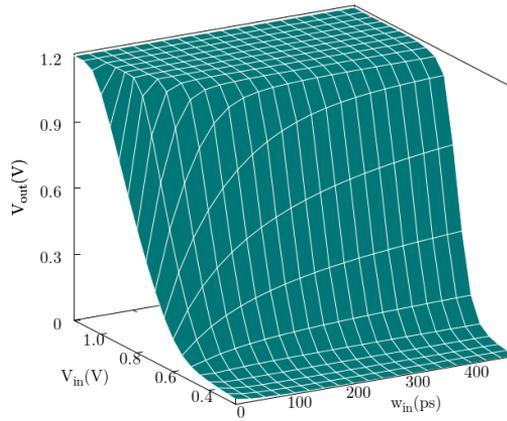


Fig. 3.9. Output perturbation voltage (V_{out}) depending on the input perturbation height (V_{in}) and width (w_{in}) obtained for a 65nm commercial CMOS technology library inverter.

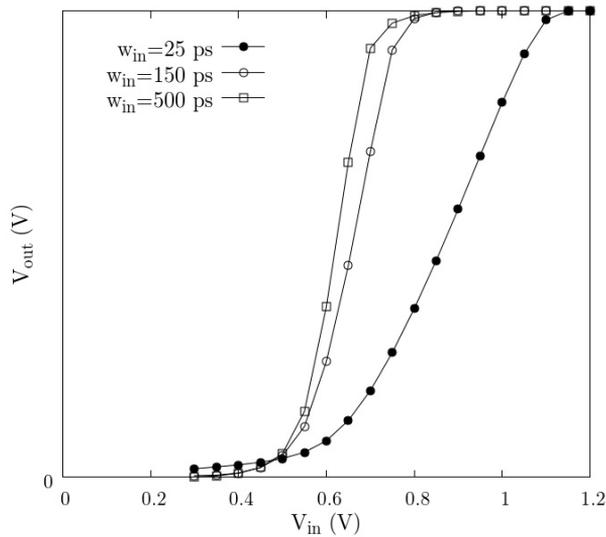


Fig. 3.10. V_{out} vs. V_{in} curves for pulse widths of 25, 150 and 500 ps.

The behavior of transfer function $V_{out}(V_{in})$ is shown in Fig. 3.10. There is a central V_{in} value for which V_{out} is $V_{dd}/2$. For larger V_{in} values, V_{out} tends to

V_{dd} , while for smaller values V_{out} tends to 0. Such a behavior is typical of a sigmoid-like function, described mathematically as:

$$s(x) = \frac{1}{1 + e^{-x}} \quad (3.2)$$

This function is centered at $x=0$, tends to 1 for positive x values and to 0 for negative values of x .

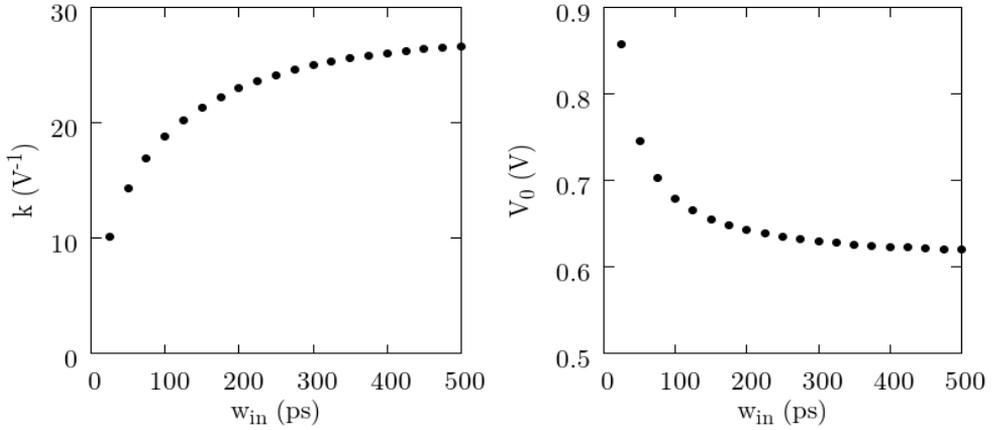
The magnitude to be described with a sigmoid function is:

$$\sigma_V = \frac{V_{out}}{V_{dd}} \quad (3.3)$$

And the function used is:

$$\sigma_V = \frac{1}{1 + e^{-k(V_{in} - V_0)}} \quad (3.4)$$

Function (3.4) is a variation of (3.2). Two additional parameters are introduced to determine the central point (V_0) and the slope (k). Parameter V_0 has units of volts being the amplitude of the incoming pulse that results in a $V_{dd}/2$ voltage at the output. For a balanced gate (i.e.: nMOS and pMOS transistor nets having equal transconductances) $V_0 \sim 0.6V$ for a $V_{dd} = 1.2V$ technology. Parameter $k[V^{-1}]$ is a measure of the function slope at $V_{in} = V_0$. The larger the k value, the higher the curve slope. A large value of k indicates that a small perturbation of V_{in} around $V_{in} = V_0$ results in a large change of V_{out} toward V_{dd} or GND . The values of both V_0 and k parameters are obtained by fitting the simulated data to (3.4). It is assumed that (3.4) is valid for any w_{in} and the dependence of σ_V on w_{in} is contained in parameters k and V_0 . Fig. 3.11 shows the dependence of parameters k and V_0 with w_{in} .

Fig. 3.11. Variation of parameters k and V_0 with w_{in} .

Similarly to the σ_V transfer function, k and V_0 can be described by analytical functions. The following expressions are used:

$$k = \frac{w_{in}}{c + \frac{w_{in}}{k_s}} \quad (3.5)$$

$$V_0 = V_{DC} \left(1 + \left(\frac{td}{w_{in}} \right)^a \right) \quad (3.6)$$

where c , k_s and a are fitting parameters; td is the delay time of the gate, and V_{DC} is the voltage at which the gate input and its output take the same voltage value in the gate DC transfer curve. Parameter c accounts for the behavior of parameter k for small w_{in} values and has units of $V \cdot ps$. Parameter k_s has units of V^{-1} and is the constant value of k for large w_{in} pulses. Then, to determine the height transfer function of a gate these five parameters must be extracted.

There is a set of curves of interest in the study of the voltage propagation shown in Fig. 3.12. These curves divide the (w_{in}, V_{in}) space in three main regions depending on the logic effect of each pulse. One region, called the

Pass Region (PR), is composed by the input perturbations for which the output voltage goes beyond 90% V_{dd} . These pulses are considered to pass the gate without getting filtered. A second region, called the *Filtering Region* (FR), is composed by the input pulses for which the output perturbation voltage value becomes lower than 10% V_{dd} . These pulses will get filtered out since their voltage height is in the noise margin. The third region, called the *Transition Region* (TR), comprises the input pulses for which the perturbation output voltage ranges between 10% V_{dd} and 90% V_{dd} . Pulses in the TR may get filtered or not depending on the electrical characteristics of the following gate in the path. Differently to many previous works, this approach does not determine if a given pulse will get filtered by the gate being traversed through comparison of its output voltage to a fixed value. Instead, the pulse propagation is determined by the relationship between the driver and load gates TR (that depends on both gate electrical characteristics and their respective output loads). In this sense, the TR is of high interest as it represents the logic gate signature when propagating an SET waveform through the circuit. It allows determining quickly which pulses will get filtered out and which will most likely traverse the gate. It also represents a valid gate signature metric to compare the predicted model vs. simulations.

The TR curves represent the projection of the intersection between the surface of $V_{out}(V_{in}, w_{in})$, like the one shown in Fig. 3.9, with horizontal planes at 10%, 50% and 90 % of V_{dd} . Given the sigmoid-like shape of the surface, such projections provide a clear idea of the output pulse voltage transition zone between GND and V_{dd} , depending on the input SET characteristics. These curves will be also used to quantify the model accuracy.

The TR graph is useful to predict if a given pulse will get filtered or amplified. As an example, take a $w_{in} = 200$ ps pulse injected at the gate input with a voltage height of $V_{in} = 0,8V$. This pulse will convert to an output pulse whose output voltage would be beyond $1.08V$ (90% of $V_{dd} = 1.2V$), thus experiencing amplification as reported in [Wir08]. However, if the input pulse height is equal to $V_{dd}/2$, then it will get dismissed, since its output voltage would be below $V_{dd}/2$.

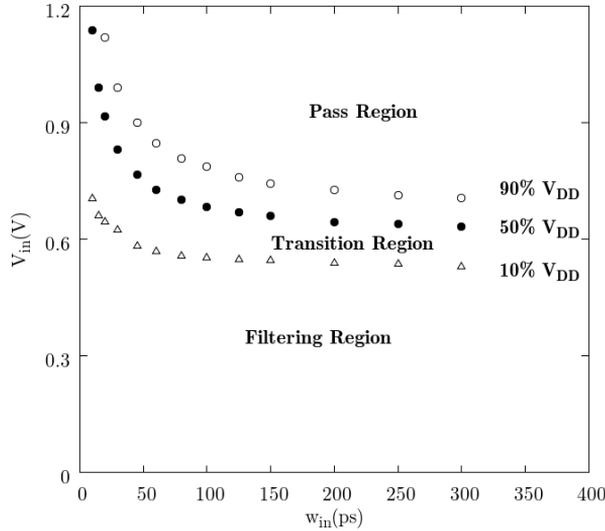


Fig. 3.12. Transition Region (TR) for a 65nm CMOS technology library inverter.

3.2.3 Width propagation

Similarly to the pulse height propagation, an excessively narrow SET pulse is not able to propagate through a logic gate causing virtually no impact at the gate output. As the width of the SET pulse increases, the gate output will exhibit a voltage perturbation whose width will also increase with the input pulse duration given that its height is beyond a given threshold. Fig. 3.13 shows the dependence of the output pulse width with the voltage and duration of the input perturbation. This figure alone can lead to misunderstandings due to the wide pulses observed. For instance, an input pulse with $w_{in} = 175$ ps and $V_{in} = 0.6$ V becomes at the output a pulse of $w_{out} = 70$ ps. Such width is long compared to the delay time of the gate (10 ps). But V_{out} is 0.3 V only, which represents a pulse not capable of propagating through the next gate. This is the reason why it is important to consider both voltage and width.

As would be expected, the curves tend to straight lines for full V_{dd} wide pulses since when the pulse duration is much larger than the gate delay,

both input and output pulses show the same width. This is shown in Fig. 3.14, where $w_{out}(w_{in})$ is represented for V_{out} values of 0.6V, 0.9V and 1.2V.

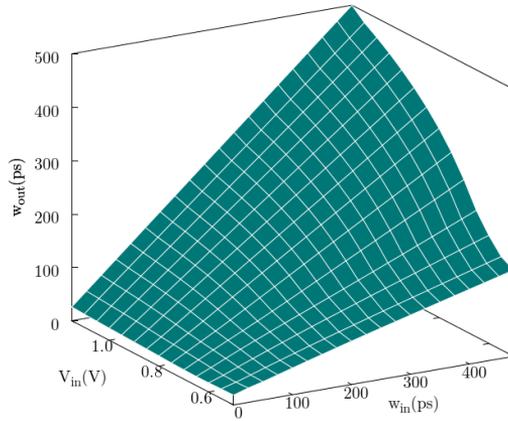


Fig. 3.13. Output pulse width (w_{out}) vs. input pulse width (w_{in}) perturbation for a 65nm technology library inverter depending on the SET input height (V_{in}).

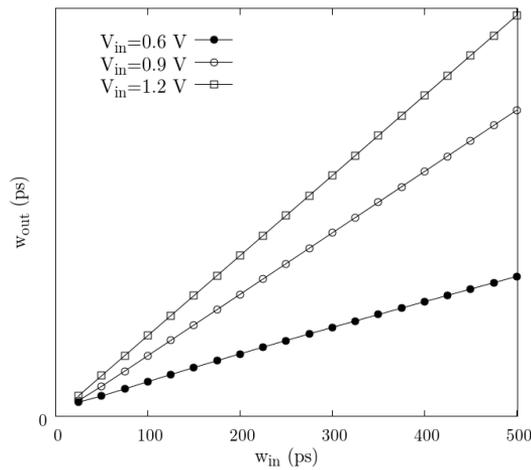


Fig. 3.14. w_{out} vs. w_{in} curves for pulse heights of 0.6, 0.9 and 1.2V.

Similarly to the pulse height propagation function, a time perturbation

relationship $w_{out}(w_{in})$ can be defined. A pulse is the waveform between two transitions. Assume a voltage transition at the input of a gate at the time instant t_1 . The transition at the output of the gate takes place at t_1+td_1 . With td_1 being the delay time of the gate. If a second transition restoring the initial voltage value takes place at t_2 , it is manifested at the output at t_2+td_2 . The width at the output is simply the difference between the two transition times:

$$w_{out} = w_{in} + \Delta td \quad (3.7)$$

Being $\Delta td = td_2 - td_1$. According to (3.7) every $w_{out}(w_{in})$ curve would have a slope equal to 1, differently from what is observed in Fig. 14, where curves for different V_{in} present different slopes. This is related to the fact that Δtd depends on w_{in} . Fig. 3.15 shows this dependence for 0.8V, 1.0V and 1.2V pulses for a 65nm technology library inverter. This dependence is due to that for narrow pulses the output doesn't complete the transition and also due to that, in the case of non-full V_{dd} pulses, the chosen waveform depends on w_{in} : rising and falling times that depend on pulse width are used to have a more realistic pulse.

Given the linear dependence of Δtd with w_{in} , and the linearity observed in Fig. 3.15, equation (3.7) can be written as:

$$w_{out} = aw_{in} + b \quad (3.8)$$

Where parameter a contains the w_{in} dependent factor of Δtd , and b is the independent factor. As in the height propagation case, it is assumed that (3.8) is valid for all V_{in} and that parameters a and b contain the dependence on V_{in} . Fig. 3.16 shows the variation of parameters a and b with V_{in} . It is difficult to describe the variation of these parameters through a simple function, especially parameter b . In this case it is more adequate to compute the delay time and use equation (3.7) directly. A delay model is presented in [Bar13] where, using a multivariable polynomial model, the delay time can be computed for several variables.

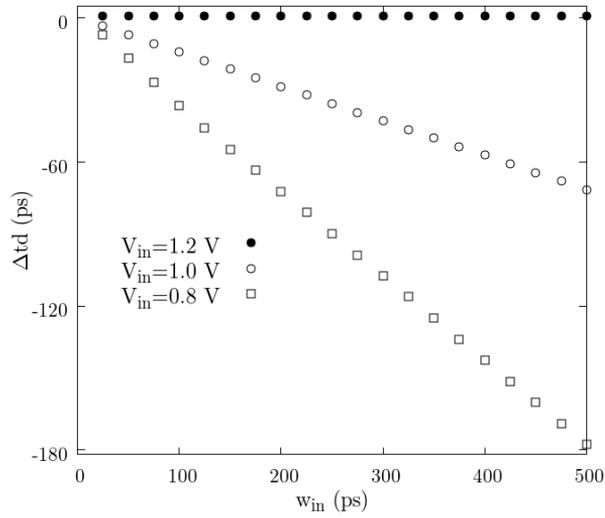


Fig. 3.15. Δt dependence on w_{in} for 0.8V, 1.0V and 1.2V pulses.

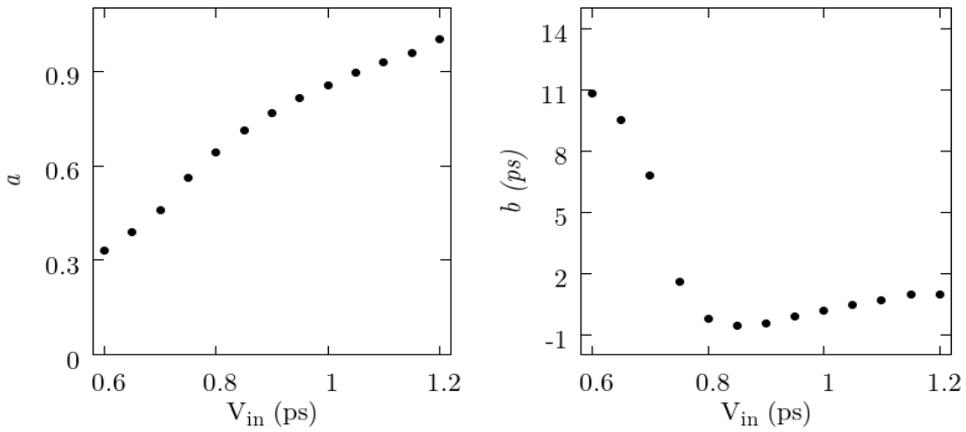


Fig. 3.16. Fig. 3.16. Width and height propagation results.

3.3 Results

The analytical height and width propagation functions derived in section 3.2 have been compared to electrical simulations for single library logic gates and several circuit paths using a 65 nm CMOS commercial technology. The results presented are divided in gate level and circuit level results. At the gate level, an inverter, a NAND and a NOR gates are used to compare the propagation model to the simulations and at the circuit level the model is used to propagate a pulse through paths taken from two ISCAS85 benchmark circuits.

3.3.1 Gate level results

The results of both height and width functions are compared to the simulations for an inverter, a NAND and a NOR. Also the TR curves, presented in section 3.2.2, are compared to simulations and the variation with the fan-out is shown.

3.3.1.1 Inverter

The inverter used corresponds to the minimum sized inverter of the library injecting a 010 pulse at its input.

3.3.1.1.a Width and height propagation.

Fig. 3.17 (a) compares the pulse width model developed to electrical simulations for the library inverter. The dots correspond to the results from simulations while the lines represent the model. Results are given for five voltage inputs from $V_{in} = 0.6 V$ to $V_{in} = 1.2 V$. An excellent agreement is obtained in all the cases for the range considered. Deviations appear for

input voltages below 0.7 V . Fig. 3.17 (b) shows the results of the pulse height propagation for several w_{in} values obtained from simulations (dots) compared to the model prediction (lines). The model provides a good accuracy for large w_{in} . For shorter pulses the behavior of the gates is such that, close to V_{dd} , the curve from simulation is sharper than the model curve. This introduces a deviation observed specially for $w_{in} = 25\text{ ps}$. This error may become significant when the model is used to describe the propagation of a pulse through a path.

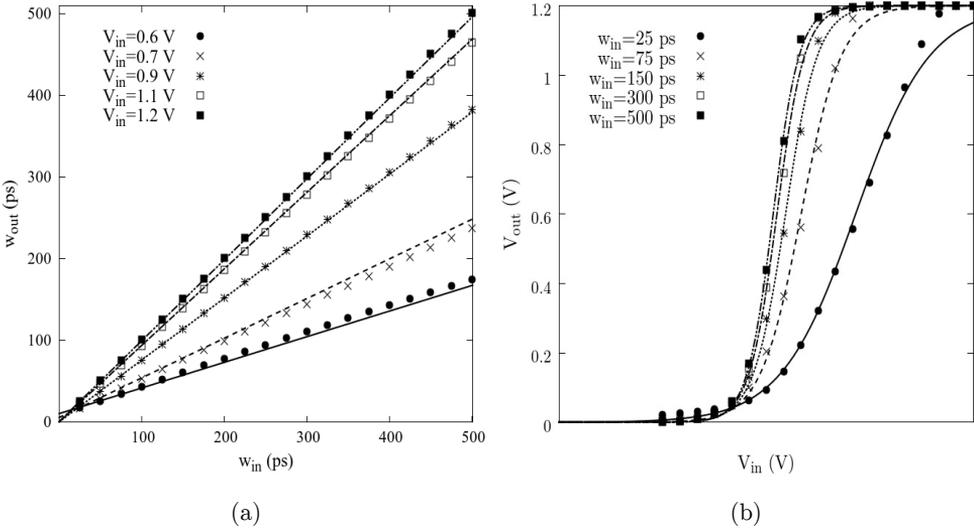


Fig. 3.17. Width and height propagation results for the inverter.

3.3.1.1.b TR curves

The TR curves of a gate, representing the input pulses $V_{in}(w_{in})$ that at the output are manifested as pulses with amplitudes of 10% V_{dd} , 50% V_{dd} and 90% V_{dd} , can be obtained analytically from equations (3.3) and (3.4):

$$V_{in} = V_0 - \frac{1}{k} \ln \left(\frac{V_{dd}}{V_{out}} - 1 \right) \quad (3.9)$$

The dependence on w_{in} is manifested through parameters k and V_0 . The curves for the three cases shown are:

$$\begin{aligned} V_{in} &= V_0 - \frac{2.197}{k} & 10\% V_{dd} \\ V_{in} &= V_0 & 50\% V_{dd} \\ V_{in} &= V_0 + \frac{2.197}{k} & 90\% V_{dd} \end{aligned} \quad (3.10)$$

The method to determine the curves by simulation is the following: for a fixed w_{in} , V_{in} is varied until the corresponding V_{out} is reached (10% V_{dd} , 50% V_{dd} or 90% V_{dd}) with the desired precision.

Fig. 3.18 compares the curves obtained using the model (lines) to the simulated ones (dots). It illustrates the model accuracy in describing the TR for a wide range of input pulse width and height values. The maximum deviation measured is of 8%, corresponding to the 90% curve for an input pulse with $w_{in} = 15$ ps. This w_{in} value is in the limit of the possible propagating pulses since the delay of this gate is about 10 ps.

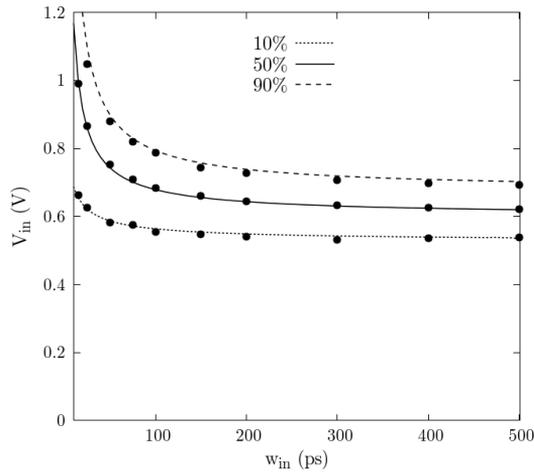


Fig. 3.18. 10% V_{dd} , 50% V_{dd} and 90% V_{dd} curves for the inverter.

3.3.1.1.c Variation with fan-out

Taking the fan-out into account is crucial to obtain a high accuracy of the predicted propagated pulse, and depending on it, an SET attaching a gate with a given fan-out can get filtered for a high f.o. or propagated for a low one. Fig. 3.19 shows how the width (a) and height (b) propagation are affected by increasing the f.o. from 1 to 5. The load of fan-out 1 corresponds to the minimum-sized library inverter of the 65nm technology used. The $w_{out}(w_{in})$ relation in (a) corresponds to a pulse with $V_{in} = 1.2$ V. And $V_{out}(V_{in})$ shown in (b) corresponds to a pulse with $w_{in} = 300$ ps.

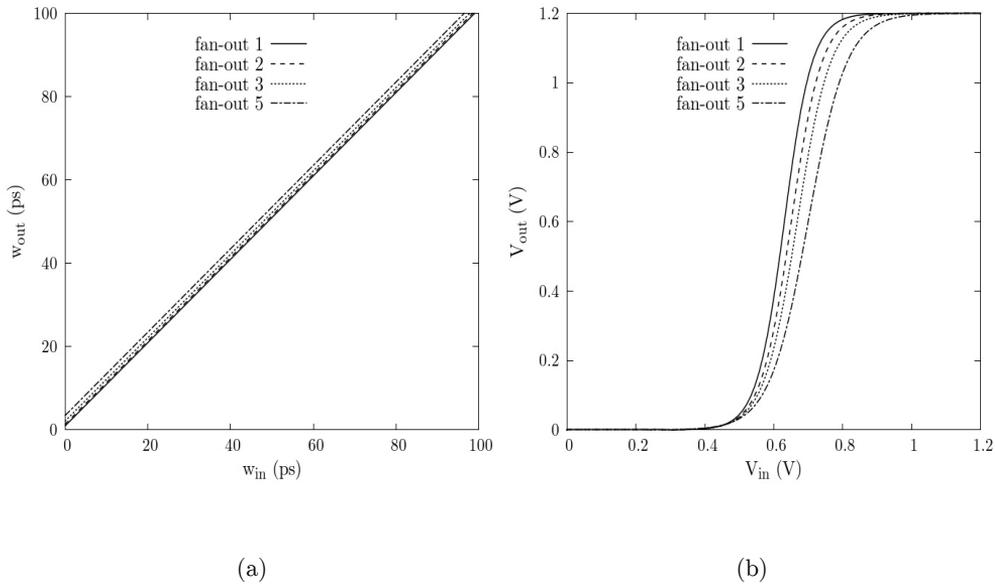


Fig. 3.19. Width and height propagation dependence on fan-out of inverter.

Table 3.1 shows the values of the extracted parameters for different fan-out values. The values of parameters a and b , used to compute the width propagation, correspond to the case with $V_{in} = 1.2$ V, and c , k_s , td and a provide the w_{in} dependence to the height propagation. Parameters suffering a higher variation are b , c , td and a , while k_s presents a small variation and a remains almost constant. Parameter b is of special interest because it describes the pulse broadening or narrowing, since parameter a is

approximately equal to 1. Thus, the values of parameter b of Table 3.1 show that the inverter broadens the pulses propagating through it, and the broadening is amplified for larger fan-outs.

Results shown in Table 3.1 correspond to a library inverter when a 010 pulse is injected at the input but different results are obtained for an inverted pulse (101). For the same inverter with fan-out 1 and a 101 pulse, the value of parameter b is -1.817 ps and increases in absolute value up to -6.42 for fan-out 5. Therefore, the effect of the increased fan-out is to amplify the broadening or narrowing of the pulse. To understand this effect, imagine the pulse as two transitions arriving to an inverter. Even if the inverter is balanced by design, there is always a difference in the response to a rising and a falling transition. Therefore, one of the transitions is faster than the other. A higher load amplifies the difference between them because it slows down the slowest of the two transitions to a greater degree than the fast one. This effect has been used in some previous works to obtain a significant broadening in chains of inverters [Fer07], [Wir08]. In these works, asymmetric fan-outs are used for odd and even inverters to favor slowing down the second transition and, therefore, the broadening.

Table 3.1. Variation of parameters with fan-out for an inverter

fan-out	a ($V_{in}=1.2$)	b (ps) ($V_{in}=1.2$)	c (V·ps)	k_s (V^{-1})	td (ps)	a
1	1.0000	0.969	1.847	29.45	9.347	0.8564
2	1.0006	1.388	2.899	29.05	13.866	0.8036
3	1.0003	2.153	3.847	28.34	18.036	0.7744
5	1.0002	3.485	5.455	26.57	25.266	0.7248

3.3.1.2 NAND

The same results than for the inverter are presented for the NAND gate. The pulse used to obtain these results was a 010 injected at the input corresponding to the gate of the n transistor closer to GND.

3.3.1.2.a Width and height propagation

Fig. 3.20 (a) and (b) compare the values of the modeled w_{out} and V_{out} to the simulations for different values of w_{in} and V_{in} . w_{out} values present deviations for pulses below V_{dd} . The same behavior than for the inverter is observed for V_{out} , with the model below the simulation for values close to V_{dd} .

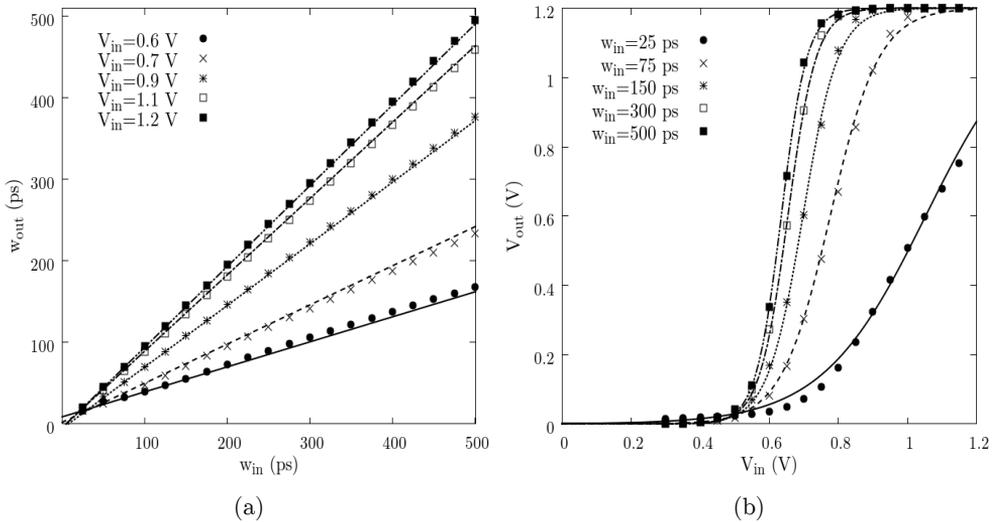


Fig. 3.20. Width and height propagation results for the NAND.

3.3.1.2.b TR curves

The results, shown in Fig. 3.21, provide an accurate description of the voltage propagation with small deviations from simulations for small values of w_{in} close to the limit of the gate delay.

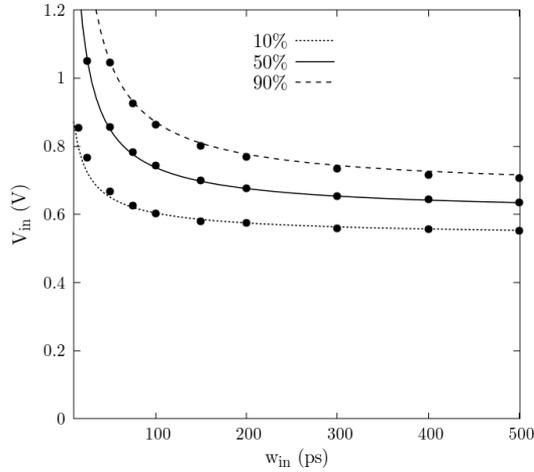


Fig. 3.21. 10% V_{dd} , 50% V_{dd} and 90% V_{dd} curves for the NAND.

3.3.1.2.c Variation with fan-out

The variation with fan-out is shown in Fig. 3.22 (a) and (b). The $w_{out}(w_{in})$ relation in (a) corresponds to a pulse with $V_{in} = 1.2 V$ and $V_{out}(V_{in})$ shown in (b) corresponds to a pulse with $w_{in} = 300 ps$.

Table 3.2 shows the parameter variation with the fan-out observing a pulse narrowing effect due to the increase of the output load, since parameter b (for $V_{in}=1.2$) varies from -4.87 to -8.44 when the fan-out is increased from 1 to 5.

Table 3.2. Variation of parameters with fan-out for a NAND

fan-out	a ($V_{in}=1.2$)	b (ps) ($V_{in}=1.2$)	c (V·ps)	K_s (V^{-1})	td (ps)	a
1	1.0001	-4.8717	2.9752	32.148	17.993	0.8577
2	0.9992	-6.3498	4.3323	32.330	23.794	0.8007
3	0.9992	-7.3254	5.6423	32.161	28.950	0.7592
5	0.9910	-8.4390	8.0438	30.913	38.314	0.69434

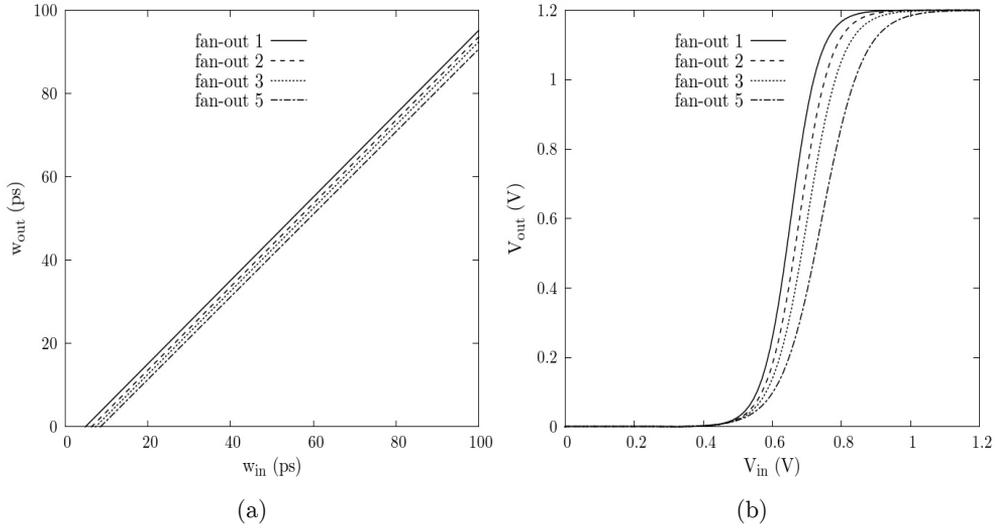


Fig. 3.22. Width and height propagation dependence on fan-out of NAND gate.

3.3.1.3 NOR

The pulse used to obtain these results was a 101 injected at the input corresponding to the gate of the p transistor closer to V_{dd} .

3.3.1.3.a Width and height propagation

The results of $w_{out}(w_{in})$ in Fig. 3.23 (a) show the high accuracy obtained by the model for all the values of V_{in} , providing a more precise description than for the inverter and the NAND. Regarding $V_{out}(V_{in})$, Fig. 3.23 (b) shows that the accuracy of the model for values close to V_{dd} is higher than for the inverter and the NAND. The deviations in this case are more important for low values of V_{out} , which is not important because such pulses don't propagate.

3.3.1.3.b TR curves

The model provides a very accurate description of the 50% and 90% curves (Fig. 3.24), but shows deviations in the 10% curve at w_{in} values below 75 ps, which agrees with the results observed in Fig. 3.23 (b).

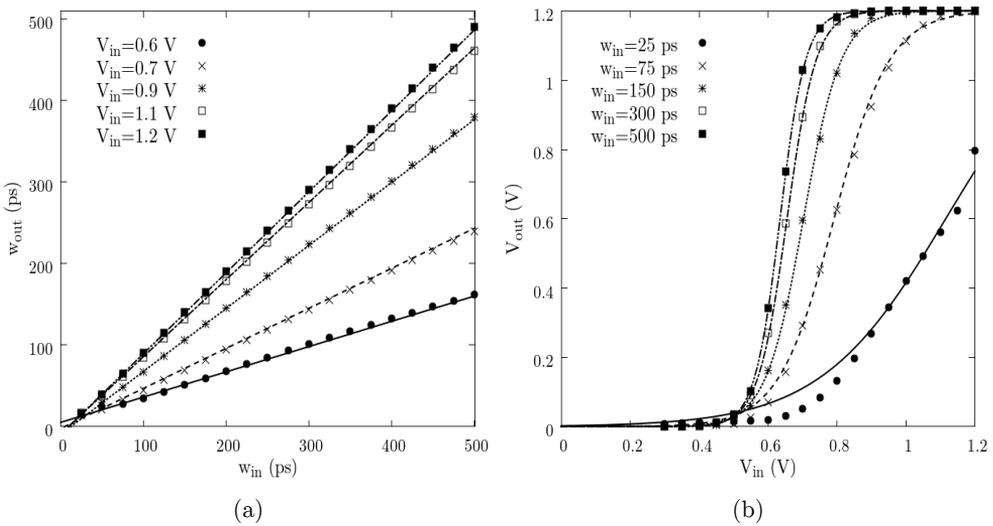


Fig. 3.23. Width and height propagation results for NOR.

3.3.1.3.c Variation with fan-out

The results for different fan-out presented in Fig. 3.25 correspond to a pulse with $V_{in} = 1.2V$ in (a) and to a pulse with $w_{in} = 300 ps$ (b). Table 3.3 shows the variation of width and height propagation parameters with fan-out where a strong pulse narrowing effect is observed. Parameter b varies from -9.7 to -18.5 increasing the fan-out from 1 to 5.

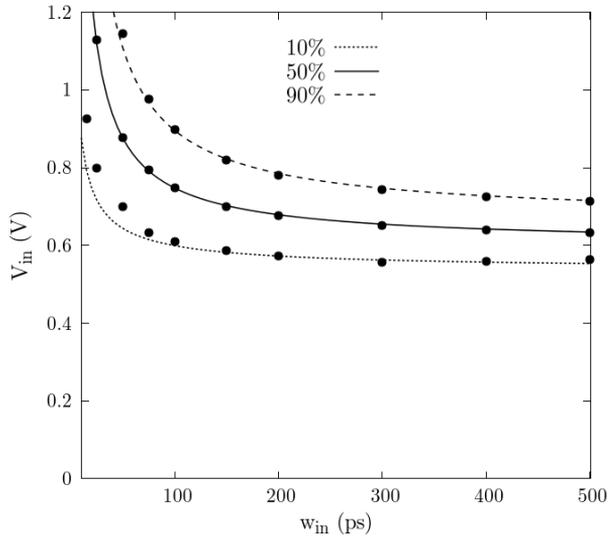


Fig. 3.24. 10% V_{dd} , 50% V_{dd} and 90% V_{dd} curves for the NOR.

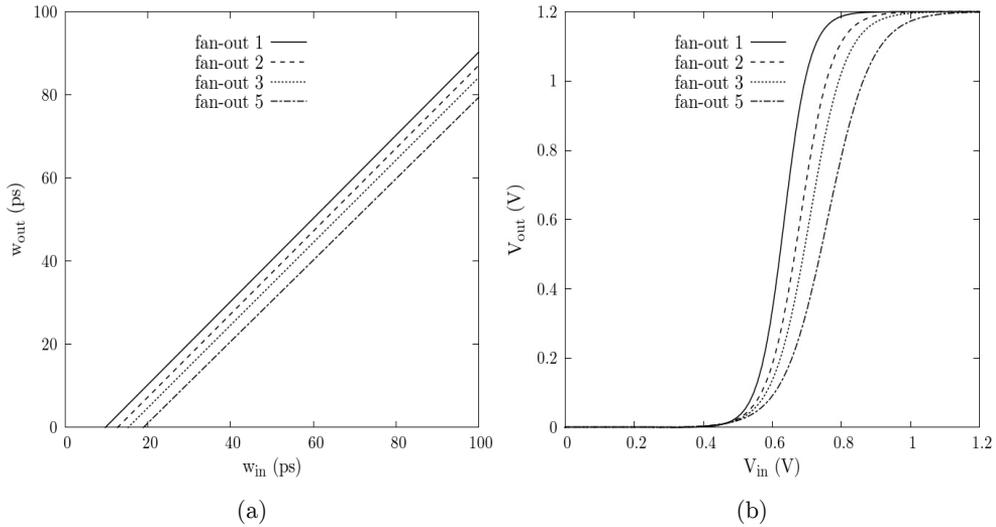


Fig. 3.25. Width and height propagation dependence on fan-out of NOR gate.

Table 3.3. Variation of parameters with fan-out for a NOR

fan-out	a ($V_{in}=1.2$)	b (ps) ($V_{in}=1.2$)	c (V·ps)	K_s (V^{-1})	td (ps)	a
1	0.9994	-9.686	3.811	34.118	21.112	0.9017
2	0.9968	-12.609	5.596	35.294	27.670	0.8409
3	0.9925	-15.080	7.340	35.767	33.570	0.7836
5	0.9788	-18.499	10.595	34.874	44.883	0.6962

3.3.2 Circuit level results

Once the parameters of the width and height propagation functions are extracted, these functions are used to compute the propagation of a pulse through a path. SET pulses are injected to the first gate of the path under analysis, and the input SET width and height are transformed to the corresponding output width and height through the functions of the first gate. The obtained output pulse height and width values become the input parameters for the next gate in the path. The process is repeated for all the gates of the path.

The paths chosen to validate the model at the circuit level are a chain of ten inverters, a path from the ISCAS85 C432, and four paths from ISCAS85 C5315 circuit, labeled as p59, p60, p80 and p956. The verification consists in comparing the TR curves and the evolution of the pulse through the subsequent nodes of the chain.

The TR curves is a concept used to describe the height propagation function of a single gate but it can also be applied to a path substituting the output of the gate for the output of the path. The main difference with the TR curves of a gate is that for a path the lines are closer to each other. It means that the transition from a filtered to a propagated pulse is more abrupt than for a gate.

3.3.2.1 Inverter chain

The chain consists of ten minimum-sized inverters from the 65nm CMOS commercial technology used. To apply the model, parameters a , b , c , k_s , td and a have to be extracted first for each gate. As has been commented previously, parameters are different depending on the sign of the pulse (010 or 101). Thus, the sign of the pulse at each node has to be known. In this case, a 010 pulse is injected at the input of the chain and therefore the input of the odd inverters is a 010 pulse while the input of the even inverters is a 101 pulse. The fan-out also has to be taken into account. In the case of this chain the fan-out is always 1 because chain is made up with the same inverter that has been used as a load to extract the parameters. If a different gate is connected at the output, a fan-out equivalent to the load of the connected gate has to be used. If the values of the extracted parameters for each fan-out are tabulated, once the equivalent fan-out is known, the values of the parameters are found by interpolation.

3.3.2.1.a TR curves

The TR curves from simulation are obtained in the same way than for a single gate while the curves from the model can't be obtained using equations (3.10) because propagating functions correspond to one gate only and the propagation is computed applying several functions successively. Therefore, the process to determine the TR curves using the model is similar to the process used with simulations. For a fixed w_{in} the V_{in} is varied until V_{out} reaches the corresponding value. The difference is that using the model, V_{out} is computed through the analytical derived functions.

Fig. 3.26 shows the TR curves for the chain obtained from simulation (dots joined with dashed lines) and using the model (solid lines). The accuracy of the model is high for large values of w_{in} providing a very good description of the height propagation. For lower values the model deviates slightly from the simulations. The model curves stay below the simulation curves indicating that the model is conservative because there is a region where,

according to the model, propagation occurs while according to the simulations belongs to the filtering region. This curves show the limitations of the model to describe the pulse propagation as will be shown in the next subsection. As mentioned before, the curves for a path are closer than for a single gate. It can be observed in Fig. 3.26 where the curves for 10%, 50% and 90% are almost superposed.

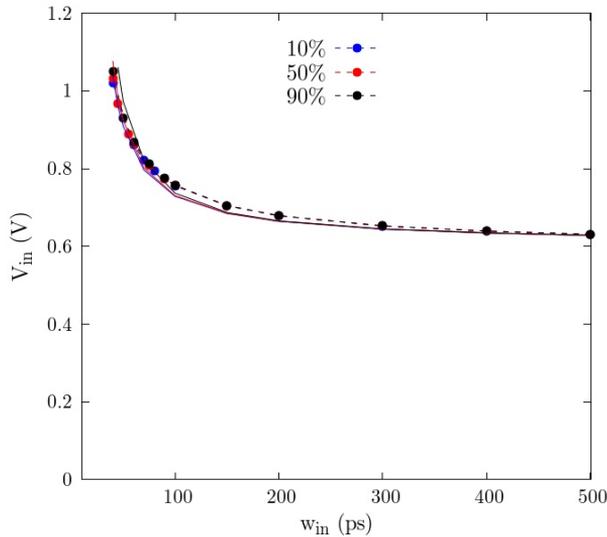


Fig. 3.26. 10% V_{dd} , 50% V_{dd} and 90% V_{dd} curves for the inverters chain.

3.3.2.1.b Pulse evolution

The objective of this test is to observe the pulse at each node of the path comparing the model to the simulations. The test is performed for three different input pulses. The first input pulse is a pulse below 10% curve from both simulation and model. It means that it is in the filtering region. In this case the pulse evolution through the chain ends in pulse filtering for both simulation and model. Table 3.4 compares the modeled values of the pulse width and height to the simulations at the even nodes of the chain from 0 (chain input) to 10 (chain output). And Fig. 3.27 shows a graphical

representation of the pulse evolution in Table 3.4. Each dot of the graph corresponds to a (w, V) at a chain node.

The second pulse injected at the input is a pulse in the TR region of the simulated curves. Since the modeled curve is below the simulated one, it is expected that, according to the model, the pulse propagates, while according to simulations the pulse may get filtered or propagated since it is in the simulated TR. Table 3.5 shows the evolution of such a pulse at even nodes, and Fig. 3.28 is its graphical representation. As expected, according to the model the pulse propagates and manifests at the output with $w_{out} = 10.23$ ps and $V_{out} = 0.43$ V, while the results from simulation show that the pulse gets filtered.

The last of the three pulses injected is a pulse above the 90% simulated curve, therefore it is expected that it propagates according to both model and simulation. Table 3.6 and Fig. 3.29 show the evolution of such pulse and confirm that both model and simulation coincide in the propagation prediction. Regarding the difference between the simulated and modeled propagated pulse, the maximum deviation corresponds to the last node with a relative error of 7.7%.

Table 3.4. Pulse in the Filtering Region (inv)

Node	Simulation		Model	
	V (V)	w (ps)	V (V)	w (ps)
0	0.70	100.00	0.70	100.00
2	0.29	28.20	0.50	30.56
4	0.00	0.00	0.00	0.00
6	0.00	0.00	0.00	0.00
8	0.00	0.00	0.00	0.00
10	0.00	0.00	0.00	0.00

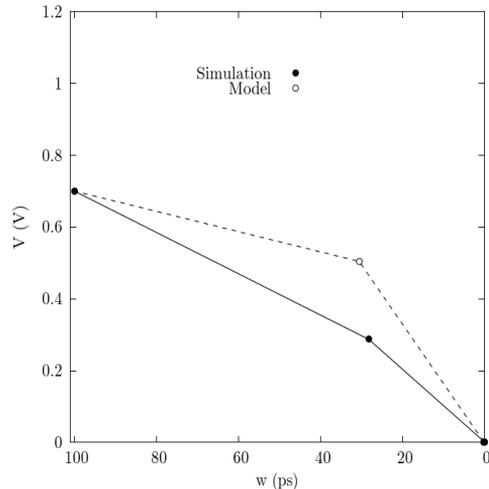


Fig. 3.27. Pulse in the Filtering Region (inv).

Table 3.5. Pulse in the TR (inv)

<i>Node</i>	<i>Simulation</i>		<i>Model</i>	
	<i>V (V)</i>	<i>w (ps)</i>	<i>V (V)</i>	<i>w (ps)</i>
0	0.80	70.00	0.80	70.00
2	0.86	34.21	1.11	34.58
4	0.31	15.00	1.16	29.26
6	0.00	0.00	1.13	25.39
8	0.00	0.00	1.03	20.53
10	0.00	0.00	0.43	10.23

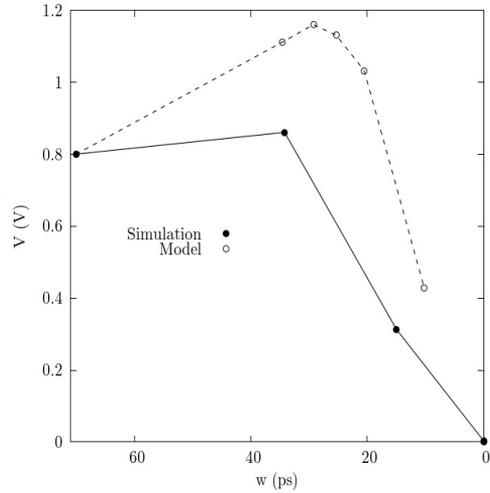


Fig. 3.28. Pulse in the TR (inv).

Table 3.6. Pulse in the Pass Region (inv)

<i>Node</i>	<i>Simulation</i>		<i>Model</i>	
	<i>V (V)</i>	<i>w (ps)</i>	<i>V (V)</i>	<i>w (ps)</i>
0	0.80	150.00	0.80	150.00
2	1.20	94.92	1.20	90.18
4	1.20	94.12	1.20	89.39
6	1.20	94.23	1.20	88.59
8	1.20	94.31	1.20	87.79
10	1.20	94.28	1.20	86.99

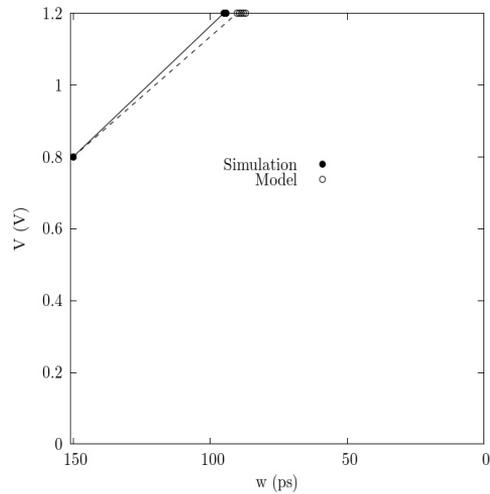


Fig. 3.29. Pulse in the Pass Region (inv).

3.3.2.2 C432

A chain of inverters is valid as an academic example but it is not a path that can be found in an actual circuit. To account for realistic circuits

several paths from ISCAS85 circuits have been tested. The first one is a path from the circuit C432 shown in Fig. 3.30.

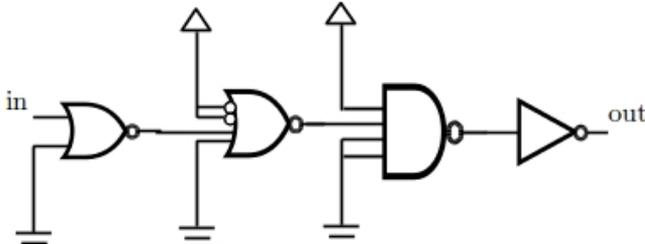


Fig. 3.30. Path from ISCAS85 C432.

3.3.2.2.a TR curves

The deviation of the model from the simulation is larger than for the inverter chain, which implies that the accuracy of the model for this chain will be worsen.

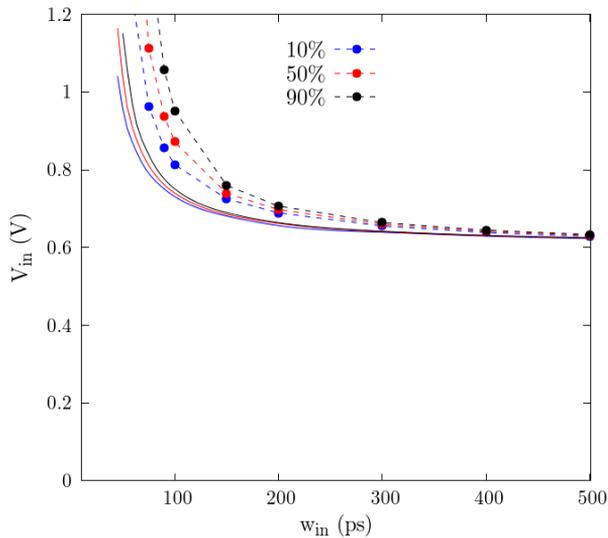


Fig. 3.31. Fig. 28. 10% V_{dd} , 50% V_{dd} and 90% V_{dd} curves for C432.

3.3.2.2.b Pulse evolution

The pulses used in this case are chosen in the same way than for the inverters chain. Table 3.7 and Fig. 3.32 show the results of a pulse below both simulated and modeled 10% curve. Both cases predict the pulse filtering and the height and width modeled agree with the values from simulations, specially the pulse width.

The second pulse chosen corresponds to a pulse in the Transition Region of the simulated curves. The evolution of the pulse as it propagates through the path is shown in Table 3.8 and Fig. 3.33. As expected, the divergence between model and simulation in this case is high. According to the model the pulse propagates to the output while according to the simulation results the pulse is filtered.

The third pulse is in the Pass Region of both model and simulation. The agreement of the model with the simulation results is significant in this case, with a maximum width relative error of only 4%.

Table 3.7. Pulse in the Filtering Region
(c432)

Node	Simulation		Model	
	V (V)	w (ps)	V (V)	w (ps)
0	0.65	200.00	0.65	200.00
1	0.72	96.78	0.77	95.41
2	0.37	53.47	0.63	56.17
3	0.01	23.53	0.13	32.53
4	0.00	0.00	0.00	0.00

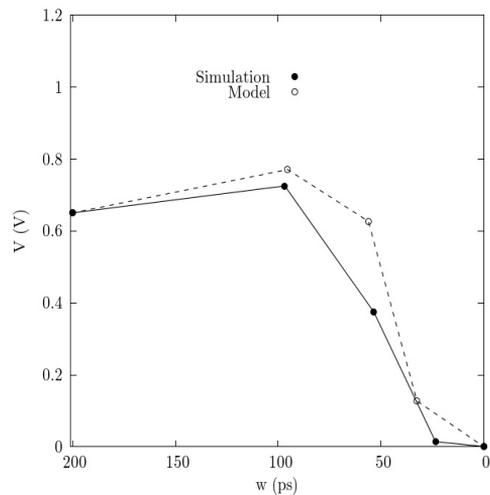


Fig. 3.32. Pulse in the Filtering Region (c432).

Table 3.8. Pulse in the TR (c432)

<i>Node</i>	<i>Simulation</i>		<i>Model</i>	
	<i>V (V)</i>	<i>w (ps)</i>	<i>V (V)</i>	<i>w (ps)</i>
0	0.71	150.00	0.71	150.00
1	0.97	84.71	1.01	84.44
2	0.84	59.68	1.10	63.86
3	0.34	35.95	1.00	49.70
4	0.01	18.09	1.19	42.14

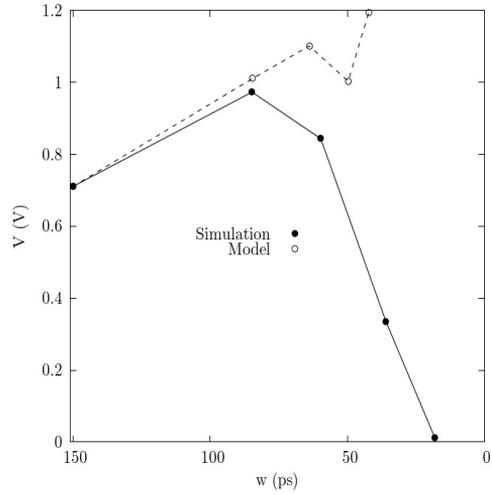


Fig. 3.33. Pulse in the TR (c432).

Table 3.9. Pulse in the Pass Region (c432)

<i>Node</i>	<i>Simulation</i>		<i>Model</i>	
	<i>V (V)</i>	<i>w (ps)</i>	<i>V (V)</i>	<i>w (ps)</i>
0	1.00	120.00	1.00	120.00
1	1.20	108.83	1.20	108.01
2	1.20	96.13	1.20	96.05
3	1.05	73.64	1.18	75.05
4	1.20	61.21	1.20	63.61

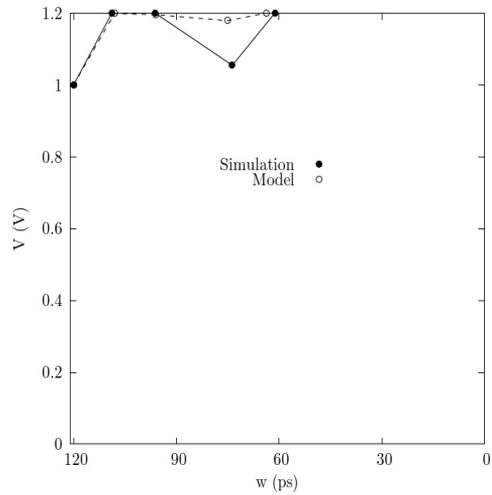


Fig. 3.34. Pulse in the Pass Region (c432).

3.3.2.3 Path 956

The next path to be analyzed is the p956 from the ISCAS85 C5315, shown in Fig. 3.35. The first stage of the path is a buffer made up with two inverters. Then, since the model is developed for single gates, the buffer is treated as two inverters and the propagation functions for each gate has to be determined.

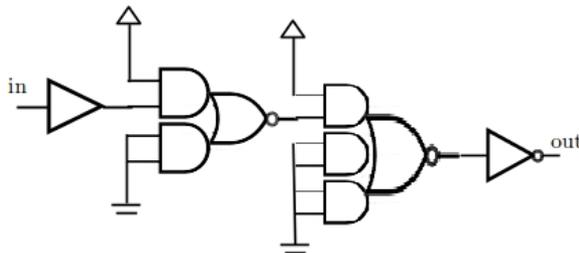


Fig. 3.35. Path 956.

3.3.2.3.a TR curves

Fig. 3.36 compares the model (solid lines) to the simulation (dots with dashed lines). The model lines are always below the simulation lines, making it a conservative model. Deviations are observed for pulses with w_{in} below 250 ps.

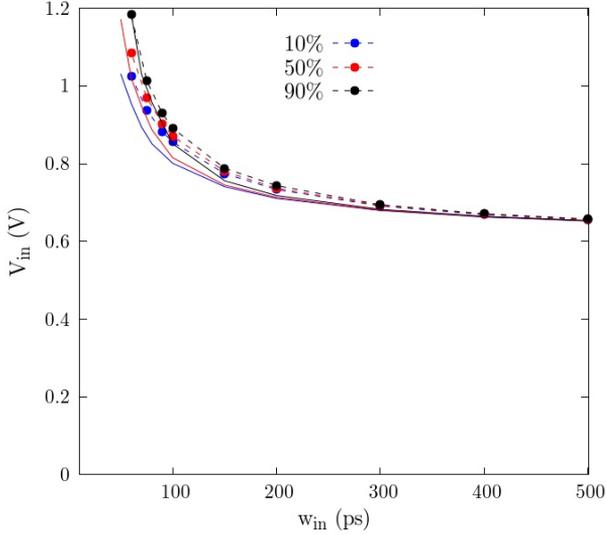


Fig. 3.36. 10% V_{dd} , 50% V_{dd} and 90% V_{dd} curves for p956.

3.3.2.3.b Pulse evolution

The same kind of pulses than in the previous pulse evolution analysis have been injected to the input of the path 956. Table 3.10 and Fig. 3.37 show the evolution through the path of an initial pulse in the Filtering Region. The prediction of both model and simulation agree that the pulse is filtered. The evolution of the second pulse injected at the input is shown in Table 3.11 and Fig. 3.38. As in the previous cases where the initial pulse is chosen inside the TR of the simulation curves, there is a difference between the prediction of the model and the simulation. The model predicts an almost full- V_{dd} propagated pulse while from simulation the propagated pulse is about $V_{dd}/2$.

The last pulse used in this analysis is a pulse in the Pass Region of both modeled and simulated curves. It is shown in Table 3.12 and Fig. 3.39. The prediction of the model agrees completely with the simulations obtaining a maximum width deviation of 5%.

Table 3.10. Pulse in the Filtering Region (p956)

Node	Simulation		Model	
	$V (V)$	$w (ps)$	$V (V)$	$w (ps)$
0	0.78	100.00	0.78	100.00
1	0.39	36.37	0.67	38.04
2	0.03	17.77	0.16	23.81
3	0.00	0.00	0.00	0.00
4	0.00	0.00	0.00	0.00

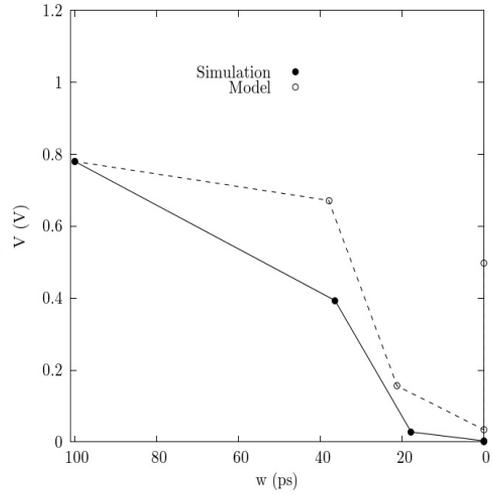


Fig. 3.37. Pulse in the Filtering Region (p956).

Table 3.11. Pulse in the TR (p956)

Node	Simulation		Model	
	$V (V)$	$w (ps)$	$V (V)$	$w (ps)$
0	0.87	100.00	0.87	100.00
1	1.10	58.97	1.19	63.49
2	1.20	51.25	1.20	70.84
3	0.69	52.19	1.11	66.71
4	0.58	26.56	1.14	55.00

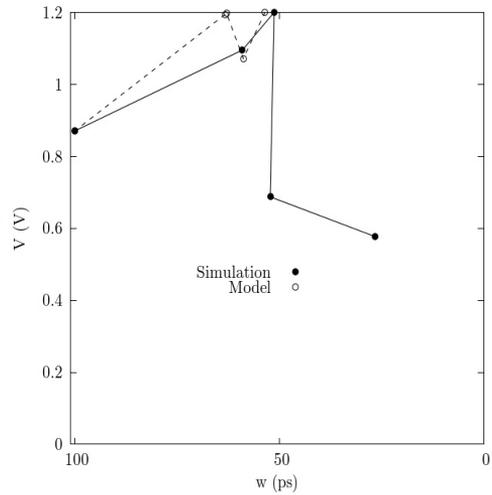


Fig. 3.38. Pulse in the TR (p956).

Table 3.12. Pulse in the Pass Region (p956)

Node	Simulation		Model	
	V (V)	w (ps)	V (V)	w (ps)
0	0.90	150.00	0.90	150.00
1	1.20	112.72	1.20	114.63
2	1.20	110.64	1.20	114.89
3	1.20	105.74	1.19	110.79
4	1.20	104.77	1.20	109.34

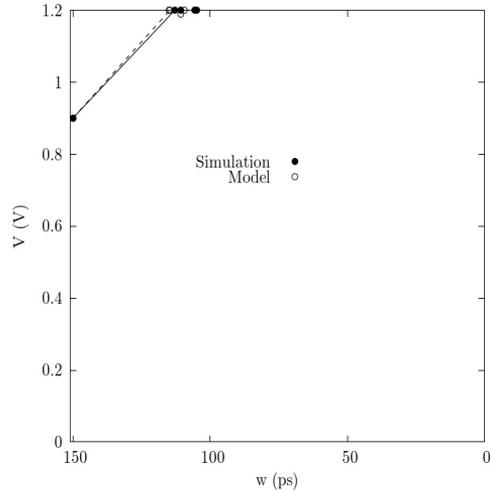


Fig. 3.39. Pulse in the Pass Region (p956).

3.3.2.4 Path 80

This path is taken from the ISCAS85 C5315 and is shown in Fig. 3.40.

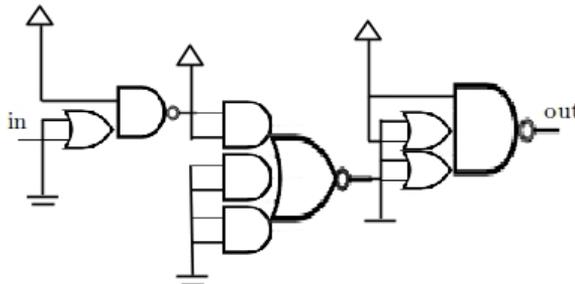


Fig. 3.40. Path 80.

3.3.2.4.a TR curves

The results of the modeled curves in Fig. 3.41 show a significant deviation from the simulations and, again, a the model is conservative since the modeled curves are below the simulated curves.

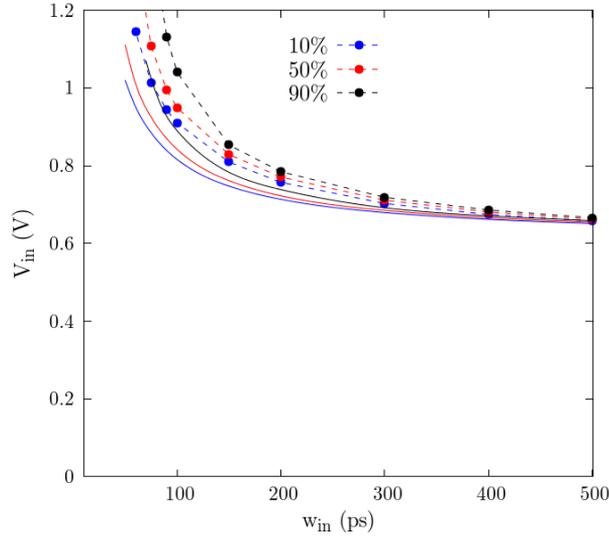


Fig. 3.41. 10% V_{dd} , 50% V_{dd} and 90% V_{dd} curves for p80.

3.3.2.4.b Pulse evolution

The pulse in the Filtering Region is shown in Table 3.13 and Fig. 3.42. Both model and simulation predict that the pulse gets filtered by the path.

The pulse in the TR evolves differently from model to simulation, as observed in Table 3.14 and Fig. 3.43. The model predicts an almost full- V_{dd} propagated pulse while from simulations a pulse of 0.61 V is observed at the output.

The prediction of the model agrees with the simulation for the pulse in the Pass Region, as can be seen in Table 3.15 and Fig. 3.44. The model propagated pulse presents a deviation from simulations at the output of 1%.

Table 3.13. Pulse in the Filtering Region
(p80)

Node	Simulation		Model	
	V (V)	w (ps)	V (V)	w (ps)
0	0.80	100.00	0.80	100.00
1	0.61	62.24	0.81	60.03
2	0.09	40.54	0.57	41.16
3	0.00	0.00	0.00	0.00

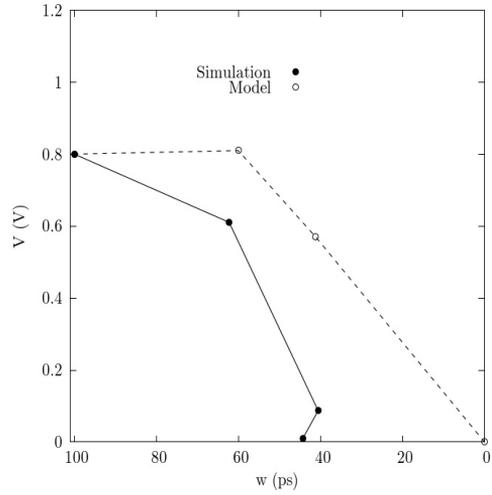


Fig. 3.42. Pulse in the Filtering Region
(p80).

Table 3.14. Pulse in the TR (p80)

Node	Simulation		Model	
	V (V)	w (ps)	V (V)	w (ps)
0	0.83	150.00	0.83	150.00
1	1.00	103.54	1.10	96.23
2	0.92	88.03	1.18	89.02
3	0.61	57.17	1.18	80.91

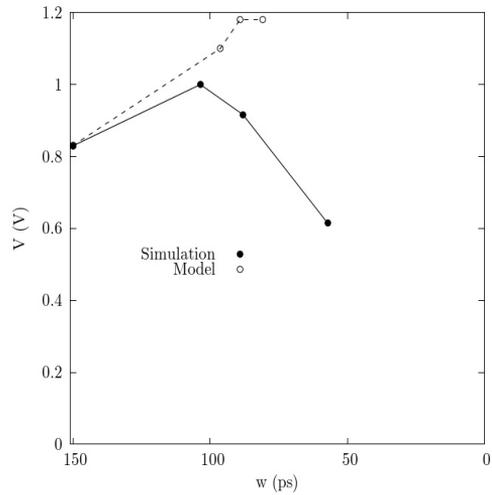


Fig. 3.43. Pulse in the TR (p80).

Table 3.15. Pulse in the Pass Region (p80)

Node	Simulation		Model	
	V (V)	w (ps)	V (V)	w (ps)
0	0.90	170.00	0.90	170.00
1	1.19	132.87	1.18	124.75
2	1.18	129.18	1.20	121.75
3	1.20	115.98	1.20	114.44

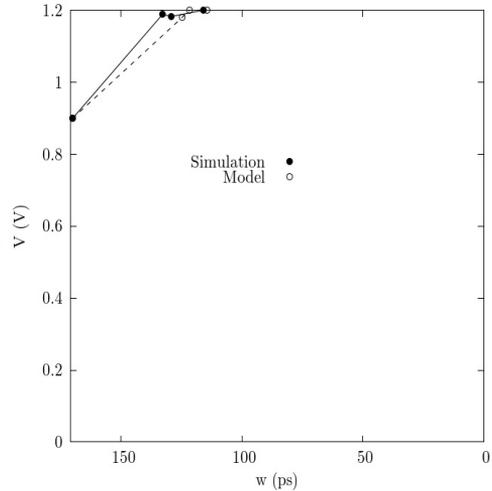


Fig. 3.44. Pulse in the Pass Region (p80).

3.3.2.5 Path 59

This is a path from the ISCAS85 C5315 circuit.

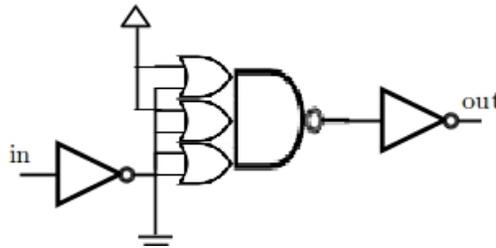


Fig. 3.45. Path 59.

3.3.2.5.a TR curves

The curves obtained from simulations and applying the model are shown in Fig. 3.46. The modeled curves (solid lines) are below the simulated curves (dots with dashed lines), providing a conservative model. The model presents deviations from simulations for pulses below approximately 250 ps.

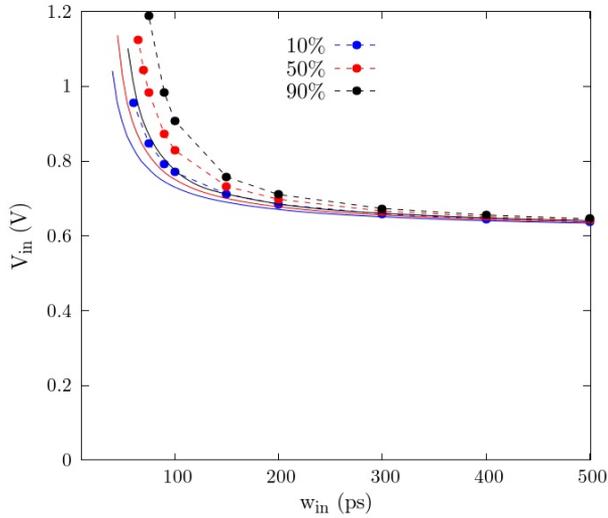


Fig. 3.46. 10% V_{dd} , 50% V_{dd} and 90% V_{dd} curves for p59.

3.3.2.5.b Pulse evolution

The evolution of a pulse in the Filtering Region is shown in Table 3.16 and Fig. 3.47. Both model and simulations predict the pulse filtering.

Regarding the pulse in the TR (Table 3.17 and Fig. 3.48), the results are similar than for the last two paths analyzed. The model predicts a full- V_{dd} propagated pulse while from simulations a 0.59 V pulse is observed at the output.

The case of a pulse in the Pass Region shows the most accurate predictions of the model (Table 3.18, Fig. 3.49) which agrees with the simulations that the pulse is propagated and provides a width estimation with a deviation of 8% from simulations.

Table 3.16. Pulse in the Filtering Region (p59)

Node	Simulation		Model	
	V (V)	w (ps)	V (V)	w (ps)
0	0.70	100.00	0.70	100.00
1	0.79	53.84	0.90	51.43
2	0.15	43.85	0.35	37.23
3	0.00	0.00	0.00	0.00

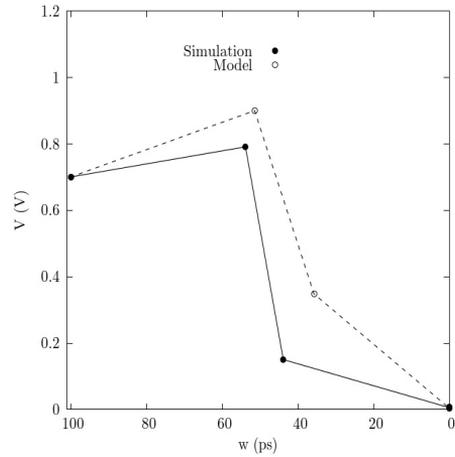


Fig. 3.47. Pulse in the Filtering Region p59.

Table 3.17. Pulse in the TR (p59)

Node	Simulation		Model	
	V (V)	w (ps)	V (V)	w (ps)
0	0.87	90.00	0.87	90.00
1	1.20	67.13	1.19	63.79
2	0.71	68.01	0.95	61.03
3	0.59	36.54	1.19	48.55

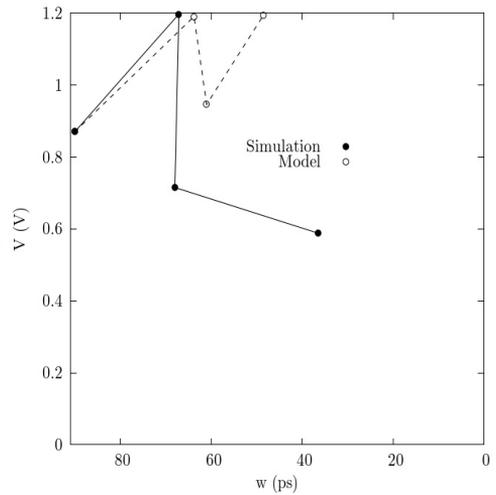


Fig. 3.48. Pulse in the TR p59.

Table 3.18. Pulse in the Pass Region (p59)

Node	Simulation		Model	
	V (V)	w (ps)	V (V)	w (ps)
0	0.90	200.00	0.90	200.00
1	1.20	158.78	1.20	149.83
2	1.20	156.81	1.19	147.89
3	1.20	158.51	1.20	145.98

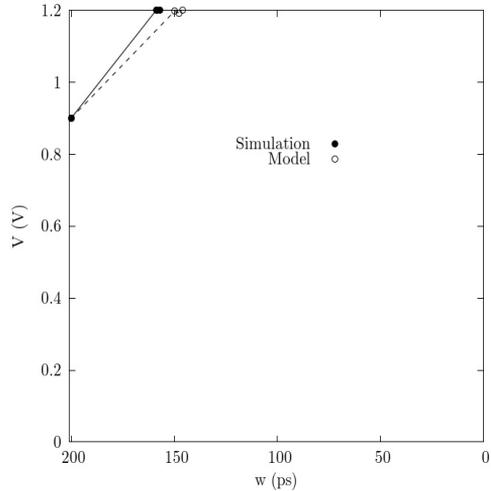


Fig. 3.49. Pulse in the Pass Region p59.

3.3.2.6 Path 60

This path is like the p59 with an additional gate, an OAI212 (Fig. 3.50).

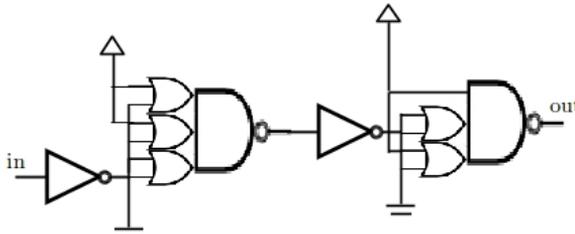


Fig. 3.50. Path 60.

3.3.2.6.a TR curves

The comparison of the curves obtained with the model to the curves obtained from simulation is shown in Fig. 3.51. Dots with dashed lines correspond to the simulation and the solid lines to the model. The deviation between model and simulations become significant for pulses below 200 ps.

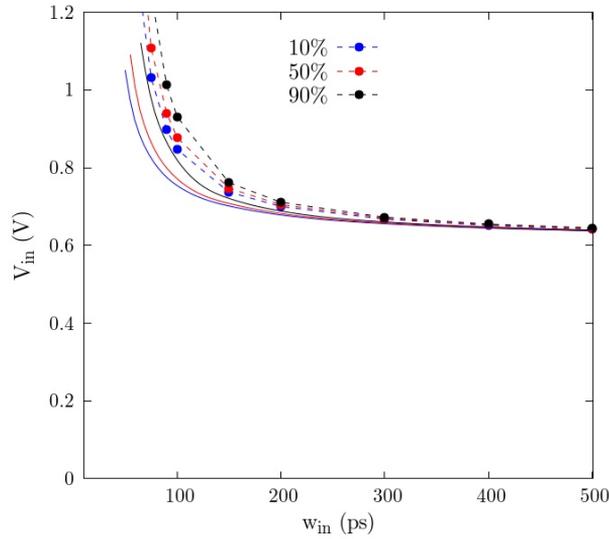


Fig. 3.51. 10% V_{dd} , 50% V_{dd} and 90% V_{dd} curves for p60.

3.3.2.6.b Pulse evolution

The pulse in the Filtering Region injected at the input of the path (Table 3.19, Fig. 3.52) is filtered according to both model and simulations.

In the case of a pulse in the TR observed in Table 3.20 and Fig. 3.52, the model predicts the propagation of the pulse reaching the output as a full- V_{dd} pulse while the simulations show a pulse filtering.

Finally, the prediction of both model and simulations for a pulse in the Pass Region (Table 3.21, Fig. 3.53) agree that the pulse propagates through the whole chain. The model provides a width deviation from simulations at the output of 6%.

Table 3.19. Pulse in the Filtering Region (p60)

Node	Simulation		Model	
	$V (V)$	$w (ps)$	$V (V)$	$w (ps)$
0	0.70	150.00	0.70	150.00
1	0.94	77.83	0.97	75.85
2	0.45	61.31	0.67	58.54
3	0.00	0.00	0.58	30.11
4	0.00	0.00	0.07	0.00

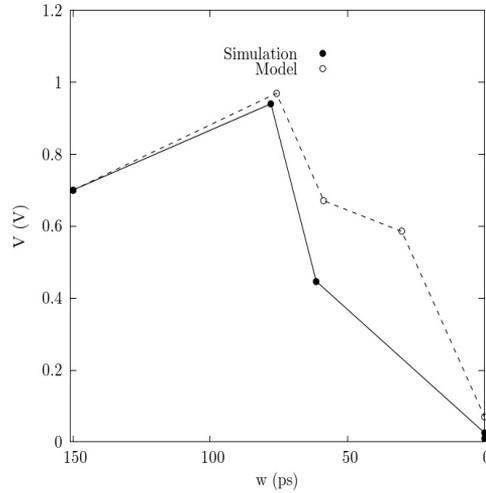


Fig. 3.52. Pulse in the Filtering Region p60.

Table 3.20. Pulse in the TR (p60)

Node	Simulation		Model	
	$V (V)$	$w (ps)$	$V (V)$	$w (ps)$
0	0.85	100.00	0.85	100.00
1	1.19	72.26	1.18	68.49
2	0.75	73.11	0.98	65.52
3	0.74	43.18	1.20	54.69
4	0.16	28.03	1.15	52.72

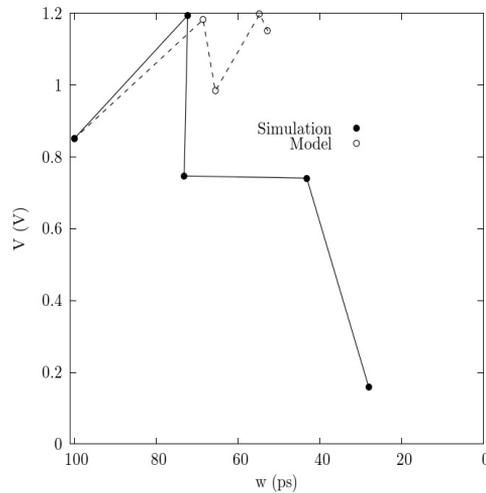


Fig. 3.53. Pulse in the TR p60.

Table 3.21. Pulse filtered (p60)

<i>Node</i>	<i>Simulation</i>		<i>Model</i>	
	<i>V (V)</i>	<i>w (ps)</i>	<i>V (V)</i>	<i>w (ps)</i>
0	0.90	150.00	0.90	150.00
1	1.20	117.14	1.20	112.21
2	1.15	114.42	1.17	110.09
3	1.20	112.82	1.20	107.42
4	1.20	112.86	1.20	105.68

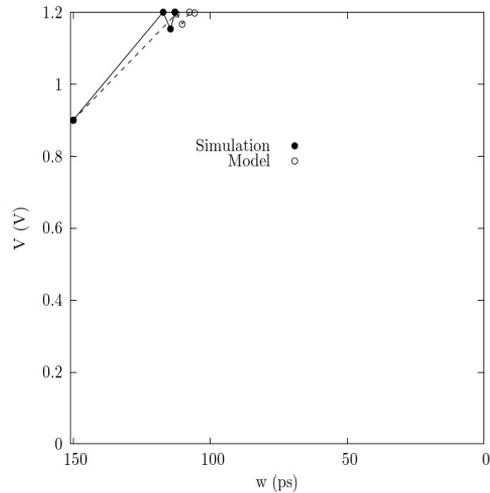


Fig. 3.54. Pulse propagated p60.

3.4 Conclusion

The SET propagation model presented differs from the previous models, presented in the first part of the chapter, in that the model developed here provides analytical continuous functions for both SET width and height. The model assigns a width and a height propagation function to each gate. These functions include parameters related to the gate characteristics that have to be extracted by fitting. This process must be done once for each gate. The model can be applied to any CMOS single gate as has been proved in this chapter, where different gates have been tested such inverters with different drive strength, NANDs and NORs with a different number of inputs, and also complex gates like AOI22, AOI222, OAI222, OAI212 and OAI21.

Once the parameters are extracted for each gate the model is used to propagate SET pulses through paths. In this process the load of the gate connected at the output of the gate under analysis is crucial to have a good accuracy. This is taken into account by extracting the parameters for different fan-outs and using the fan-out equivalent to the output load.

At circuit level, the model has been tested in two different ways. First, it has been checked its capability of describing the three limit regions: Filtering Region, Transition Region and Pass Region. The results obtained are very good for the inverters chain and the p956 and present deviations for C432, p80, p59 and p60. A common result obtained for all the analyzed paths is that the model is conservative. It means that it predicts the propagation of pulses that actually get filtered. A conservative model is desired rather than a model that predicts filtering when the pulse actually propagates. One comment to be done is that the deviation of the model from the simulations in the TR curves means that there is a region where the model doesn't agree with the simulation. But it doesn't mean that the model fails in predicting the width and height correctly in the Pass Region. In fact, it has been shown in the tables and figures corresponding to pulses in the Pass Region at different paths that the model predicts the SET characteristics with a high accuracy.

Finally, the model presented is suitable to be incorporated in CAD tools to automatically determine the Transition Region for all the paths departing from a set of nodes of interest in a given circuit. This analysis is key to determine the reliability of nanometer CMOS ICs against SET effects and compute its impact on the circuit Soft Error Rate.

The model developed in this chapter has been conceived to be implemented within a CAD tool capable of helping in the design of current technology ICs given its analytical description. Such a CAD tool development requires a huge amount of additional work to effectively deal with current circuits with a large number of logic structures. Among other issues and in addition to SET propagation, it must deal with logic path determination, path delay estimation, logic reconvergence situations, statistical path estimation and specific metric analysis. All this work has been the subject of a Doctoral Thesis developed within the Electronics System Group by Dr. S. Barceló [Bar13].

Chapter 4

SET propagation

experimental results

This chapter presents the experimental results obtained by using a pulsed laser to induce transient events on a circuit consisting of chains of logic gates. The data obtained is used to verify the validity of the model developed in the previous chapter.

4.1 GSE-UIB Laser facility

In this section the GSE-UIB pulsed laser equipment described briefly, a schematic and a photo of the equipment are shown in Fig. 4.1. The Verdi G5 (Coherent Inc.) (Fig. 4.2) is an optically pumped semiconductor laser that generates a continuous wave of 532 nm that implies a SPA. The beam generated in this stage is directed to an ultrafast mode-locked titanium:

sapphire laser Mira 900-S (Coherent Inc.) shown in Fig. 4.3. Mode-locking is a technique used to produce extremely short pulses (on the order of pico- or femtoseconds) and consists in setting a fixed phase between the modes of the laser. Then, these modes periodically interfere constructively producing a pulse.

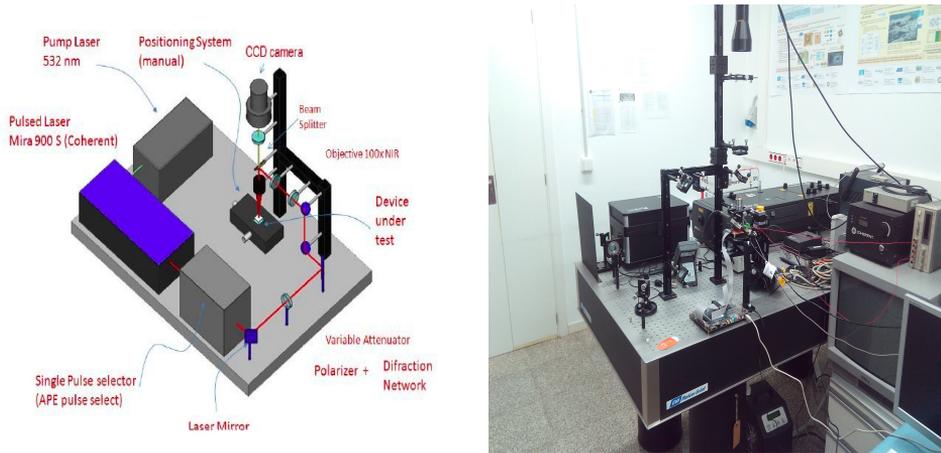


Fig. 4.1. Schematic and photo of the laser equipment.



Fig. 4.2. Verdi G5.



Fig. 4.3. Mira 900-S.

A *pulseSelect* module (APE GmbH) is used to adjust the pulse repetition rate. The *pulseSelect* (Fig. 4.4) is an acousto-optical single pulse selector developed for femtosecond laser technology for high repetition rates (70-80 MHz) and high contrast ratio. Its operation is based on the acousto-optic effect that applies a short RF pulse to the acousto-optic modulator so as to deflect the wanted pulse into a slightly modified direction. The deflected pulses are the only ones reaching the output of the *pulseSelect* module with division ratios ranging from 1:20 to 1:5000. A high frequency photodiode located in the cavity of the Mira 900-S provides the electrical signal required to synchronize the *pulseSelect* module.

A combined waveplate and polarizer, shown in Fig. 4.5, are used to modulate the laser pulse energy. The waveplate rotates the polarization angle of the beam changing its intensity while the polarizer selects only one component of the beam, implying additional intensity attenuation. The waveplate used is mounted on a rotator support that allows varying the energy of the pulse by rotating the waveplate.



Fig. 4.4. PulseSelect.

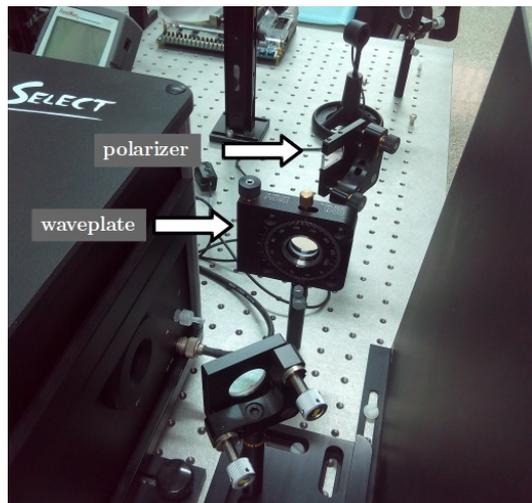


Fig. 4.5. Waveplate and polarizer.

The MPlanNIR 100 microscope (Mitutoyo) is used to focus the beam on the target surface. It has 100x magnification, a numerical aperture of 0.5 and a working distance of 12 mm. The target and the laser spot are visualized on a monitor through a CCD camera, together with an optical system composed by an objective and two lenses.

The positioning system is constructed by mounting three Precision Linear Stage PLS-85 (PI miCos GmbH), one for each axis (x , y , z), with a travel

range up to 155 mm and a resolution of 50 nm. The system is shown in Fig. 4.6. Each PLS-85 has a two-phase stepper motor with a maximum velocity of 50 mm/s. The PLS-85 is controlled with the SMC Corvus eco, a microstep-controller system that can be controlled from a PC via command language or a user interface.

The whole system is placed on an optical table with vibration-damping features and pneumatic bearings.

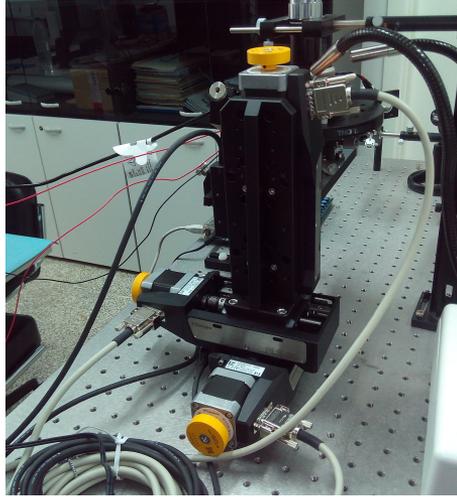


Fig. 4.6. Positioning system.

As mentioned previously, the backside laser test is sometimes the only option to access the circuit. In these cases, a specific system to open a window in the package and thin the DUT substrate is required. The ASAP-1 ISP (ULTRA TEC) sample preparation equipment (Fig. 4.7) is the equipment available in the GSE-UIB facilities for this purpose. This system contains a full 100mm x 100mm stage area, an XY precision of 200 nm and a Z precision of 40 nm. This equipment was used to prepare a 0.12 μm ST technology IC that contained a block with 15 chains of 256 logic gates. As shown in Fig. 4.8 the circuit was observable after the preparation process. The circuit finally used to perform the laser test was a circuit that had no metal layers over the area of interest, and was therefore exposed from the

circuit front-side.



Fig. 4.7. ASAP-IPS.

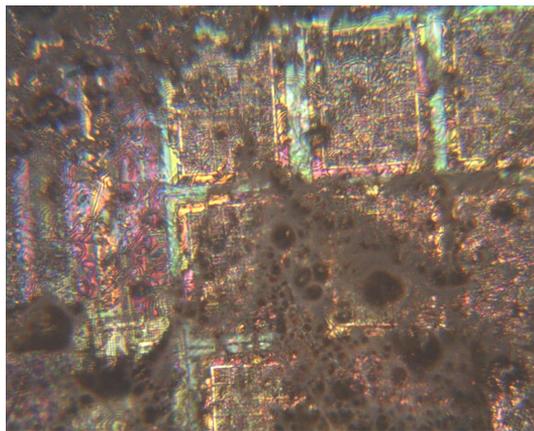


Fig. 4.8. View of the 0.12 μm ST technology circuit after substrate thinning.

4.2 IC design

The chains to be tested are part of an IC designed by the GSE-UIB using a 0.35 μm AMS technology. The chains block is shown in Fig. 4.9 enclosed within a red dotted box. A magnified section of the block is shown in Fig. 4.10 for a portion of five chains. The block was originally designed to investigate the effect of the temperature on multistage logic circuits and consists of sixteen chains of 100 logic gates each, plus one metal line used as a reference. The sixteen chains are accessed through a two-cascade 1-to-16 demultiplexer, and the logic output is multiplexed inversely (16-to-1). The delay line is used to determine the delay impact of the access circuitry. The composition of the chains in the circuit is given in Table 4.1.

Table 4.1. Chains present in the circuit

0	Reference	8	NOR3a
1	NAND3c-NOR3c	9	NAND3c
2	NAND3b-NOR3b	10	NAND3b
3	NAND3a-NOR3a	11	NAND3a
4	NOR3a-NOR3c	12	INV f.o. 3
5	NAND3a-NAND3c	13	INV f.o. 2
6	NOR3c	14	INV f.o. 1 (4.95 μm)
7	NOR3b	15	INV f.o. 1 (9.8 μm)



Fig. 4.9. Fig. 4.9. Chains block.

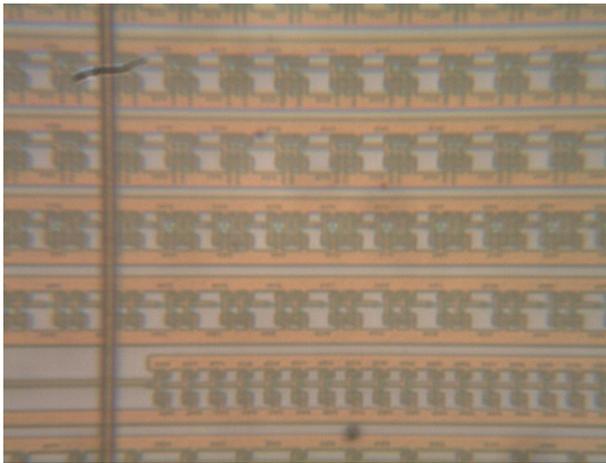


Fig. 4.10. Magnified view of the chains.

The first five chains alternate NAND and NOR gates where inputs a, b and c correspond to the input closer to GND , middle input, and input closer to output node, respectively, for the NAND gates; and to the input closer to V_{dd} , middle input, and input closer to the output node, respectively, for the NOR gates. All the cells are equally sized ($12.7 \mu\text{m} \times 9.8 \mu\text{m}$) except the inverters in chain 14 whose gate area is $12.7 \mu\text{m} \times 4.95 \mu\text{m}$. There are four chains of inverters: chain 15, chain 14 with reduced size, and chain 13 and

12 with the same inverters than chain 15 with fan-out 2 and 3 respectively. The transistors forming each gate are all equally sized: $L_n=L_p=0.3 \mu\text{m}$, $W_n=1 \mu\text{m}$, $W_p=2 \mu\text{m}$.

There is one common input for all the chains ($chain_in$), and four signals ($d0$, $d1$, $d2$, $d3$) to select the chain through which the input signal is propagated and shown at the output, being $d0$ the LSB and $d3$ the MSB, and the output signal ($chain_out$). The demultiplexer and multiplexer shown in Fig. 4.11 (a) and (b) respectively perform the chain selection as detailed previously.

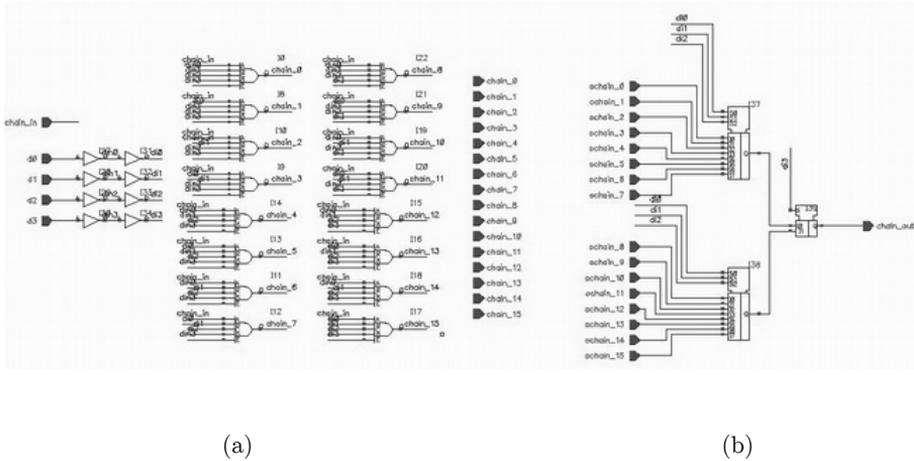


Fig. 4.11. Input demultiplexer and output multiplexer.

A specific PCB was designed and fabricated. Fig. 4.12 (a) and (b) show the schematic and the layout of the board respectively. A 68-pin socket connects the IC to the PCB and a 20-pin header connects the PCB to an Altera DE2-70 FPGA board that controls the circuit operation. The PCB was designed with two different supplies, a general one, that supplies the demultiplexer and the multiplexer, and a specific supply for the chains. Two resistors were placed close to both the general and the chains supply socket inputs to monitor the supply current as this current can provide useful information, as will be explained later.

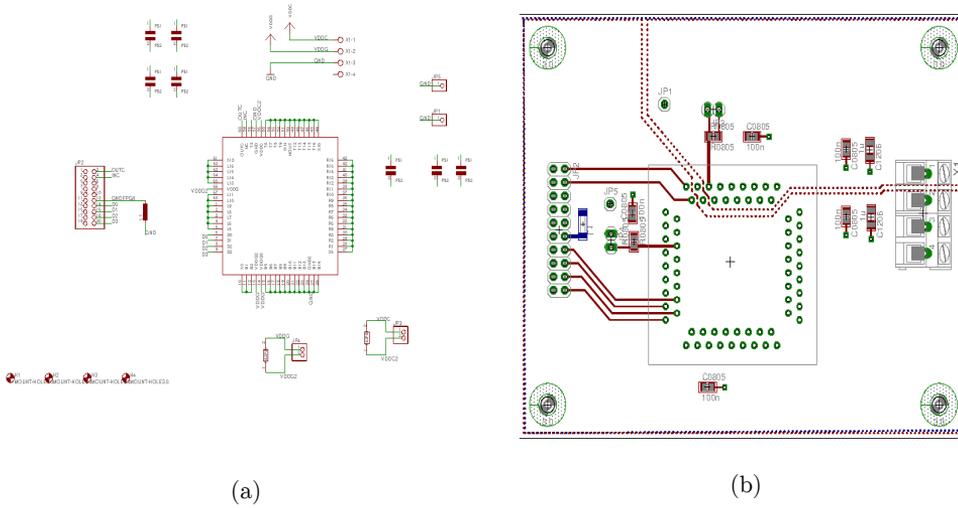


Fig. 4.12. Schematic and layout of the designed PCB.

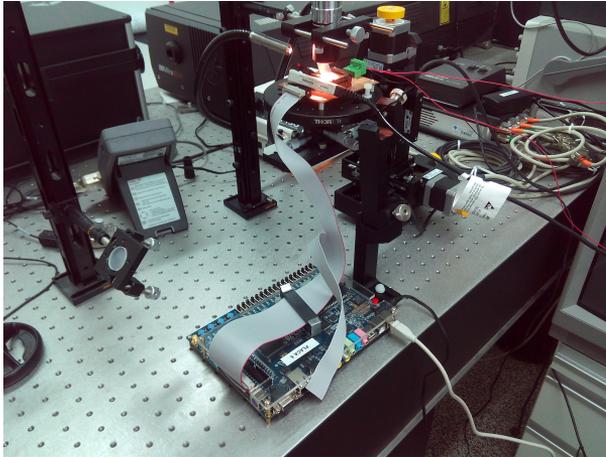


Fig. 4.13. PCB connected to the Altera DE2-70.

The IC operation was controlled with an Altera DE2-70 Board equipped with an Altera Cyclone [®] II 2C70. Fig. 4.13 shows the DE2-70 connected to the PCB on the positioning system. Other DE2-70 board components are: 2-Mbyte SSRAM, two 32-Mbyte SDRAM, 8-Mbyte Flash memory SD Card socket, 50-MHz oscillator and 28.63-MHz oscillator for clock sources, four

push button switches, 18 toggle switches, 18 red LEDs, 9 green LEDs, 24-bit audio CODEC, 2 TV decoders, ethernet controller, USB Host/Slave controller, PS/2 mouse/keyboard connector, two 40-pin expansion headers with diode protection [Alt09].

The DE2-70 was configured to provide the input signals to the circuit. These signals correspond to the chain selection ($d0$, $d1$, $d2$, $d3$) and to the input chain value ($chain_in$).

The oscilloscope used to monitor the output signal and the currents at chains supply was a DPO 70604, a digital phosphor oscilloscope with a bandwidth of 6GHz and a sample rate of 25GS/s [Dpo09].

4.3 Experimental results

Both the voltage at the output pin and the current through the chains supply were concurrently monitored at the oscilloscope. The supply current was measured using a Tektronix P7380A 8GHz differential probe connected to a low-inductance resistor specifically placed on the PCB. A typical current and voltage waveform sample measurement is shown in Fig. 4.14. The wider pulse recorded in Channel 1 corresponds to the current through the chains supply while the smaller pulse in Channel 2 corresponds to the generated SET measured at the output. It has been observed that the SET at the output has a quite strong sensitivity to the specific laser spot position on the chain gate. When the spot was focused directly on the well, the generated current pulse was much larger than when the spot hit the substrate as shown in Figs. 4.15 (a) and (b).

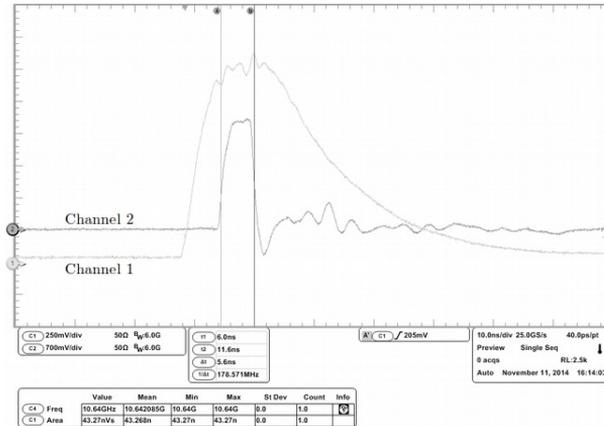


Fig. 4.14. Oscilloscope capture.

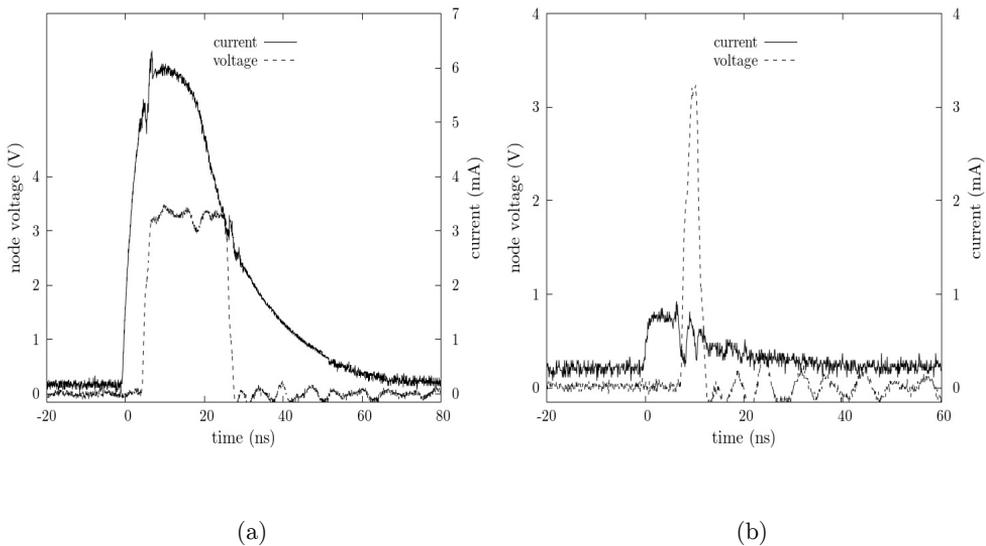


Fig. 4.15. Large and small current pulses depending on the position of the spot on the gate.

The difference in the current induced implies a difference of the SET obtained at the output. For a high current level the SET obtained is up to five times wider than the SET obtained for the low current level (Fig. 4.15). The huge width increase is due to an extra amount of charge collected. Given that the laser spot size is comparable to the size of one gate, the exact origin of this extra amount of charge is not determined. The size of

the spot compared to the size of a gate is shown in Fig. 4.16. The spot is located on the NAND3b chain, which has been used to measure the SET propagation. The layout of this gate is shown in Fig. 4.17.



Fig. 4.16. Laser spot on the chains.

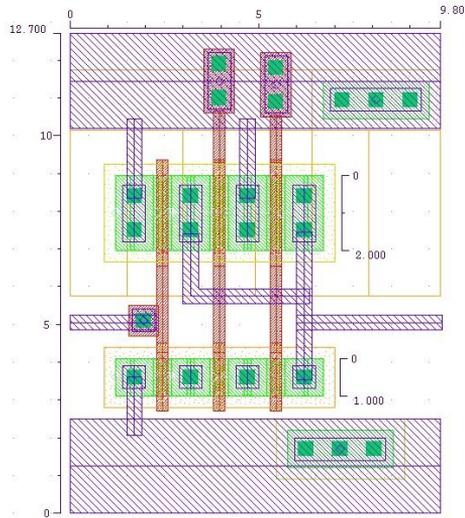


Fig. 4.17. NAND3b layout.

Another interesting effect observed is the creation of double pulses as shown in Fig. 4.18. The cause of such an effect can be two consecutive charge collections at the same node or charge collection at two different nodes. In the first case the node suffers another voltage pulse when it is recovered from the first one. And in the second case, an inverted pulse is generated due to the charge collection at an opposite transistor, lowering the voltage of the first pulse. When the second collection is finished the first pulse recovers V_{dd} .

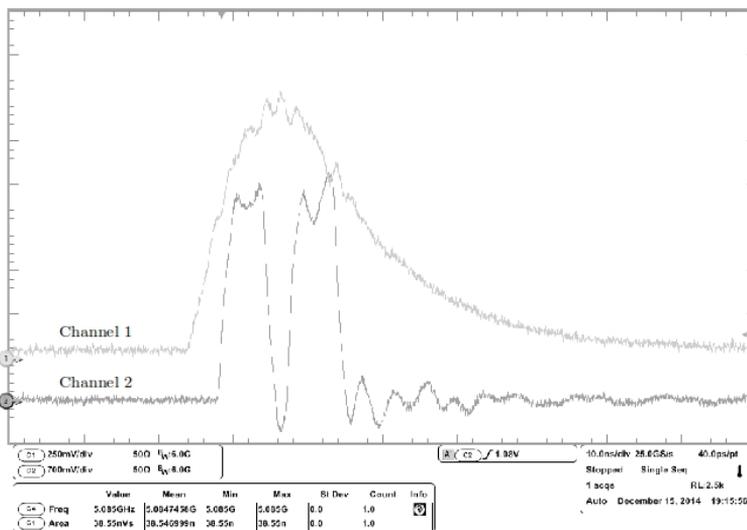


Fig. 4.18. Double pulse.

The laser energy required to induce a logic SET at the circuit output induces an excess of charge collected at the circuit supply voltage such that masks the transient supply current due to the circuit activity resulting from the pulse propagation. This circuit activity related supply current would provide a valuable information about the pulse width. In an ideal situation, when a pulse propagates through a chain, the supply current is similar to that shown in Fig. 4.19, where the chain input and output node voltages are represented together with the current through the chain supply. Two current levels are observed while the SET pulse traverses the chain: the lower value

is registered when only the first transition of the pulse occurred, inducing activity only at one gate (the one propagating the transition at each time instant). When the second transition of the pulse happens, then there are simultaneously two gates being active at any instant until the first rising transition reaches the chain end, and a second higher level (approximately at a double value than the previous one) is registered. The time window during which the current stays at the low level is a measure of the SET width.

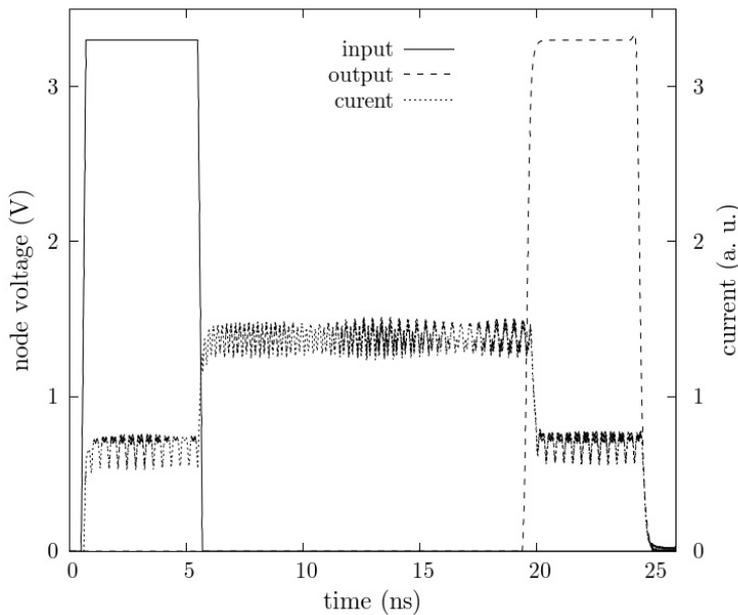


Fig. 4.19. Ideal situation obtained from simulation.

In the laser-induced SET, the generated SET width cannot be measured through the activity of the gates given the contribution of the current injected at the substrate and/or well. Therefore a different parameter relating the generated SET to the perturbation measured at the output is required. In this sense, we found a relationship between the charge, computed as the integral of the current pulse and the voltage perturbation width. Fig. 4.20 shows the relationship between the voltage pulse width at the circuit output vs. the obtained charge at different positions in the chain

of NAND3b (chain 10). Each dot color represents one chain gate output node (ranging from 1 to 100), while the lower the node number, the closer the gate to the chain input. To obtain different charge values, the energy of the laser was varied through the waveplate while the position of the laser spot on the chain remained unchanged. For each node the spot was placed at the same relative position with respect to the gate within the precision limits allowed by the positioning system. Fig. 4.20 shows a clear tendency of the lines joining the points corresponding to the same node. The intersection of this line with the horizontal axis provides an estimation of the minimum charge to generate an SET capable of propagating to the output. Then, the tendency observed indicates that for nodes closer to the output the minimum charge is lower than for nodes closer to the input. It also may imply that, assuming that the generated SET by a given charge is the same independently of the strike position in the chain, the pulse gets narrowed as it propagates through the chain. This agrees with the simulations carried out. Results for node 4 do not follow this tendency. A possible explanation is that it is due to some structural element (due the proximity to the input of the chain) that distorts the charge collection.

In the same experiment the charge generating a limit pulse was obtained, as well as the width and height of the propagated pulse. The limit pulse is the smaller pulse that can be generated at a specific node of the chain capable of reaching the output. Such a smaller pulse is obtained by changing the energy of the laser. Four chains were measured in this case: chain 1 (NAND3c-NOR3c), chain 4 (NOR3a-NOR3c), chain 10 (NAND3b) and chain 12 (INV f.o. 3). The charge corresponding to the limit pulse at several measured nodes is shown in Figures 4.21, 4.22, 4.23 and 4.24. Each point corresponds to the average of 10 measures.

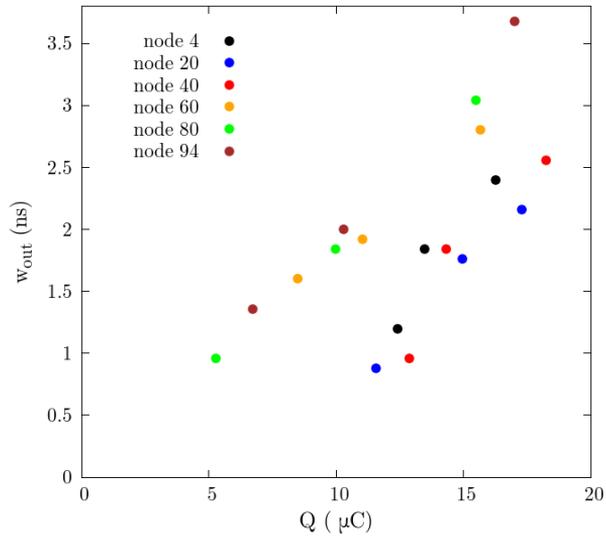


Fig. 4.20. Output width as a function of charge at several nodes.

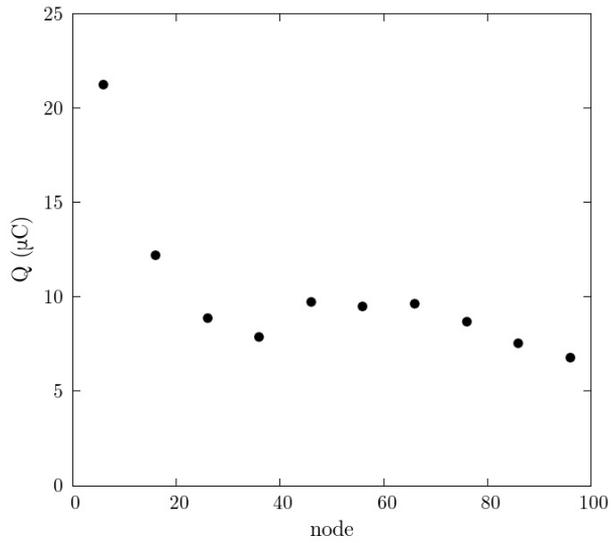


Fig. 4.21. Charge for limit pulse for several nodes for chain 4 (NOR3a-NOR3c).

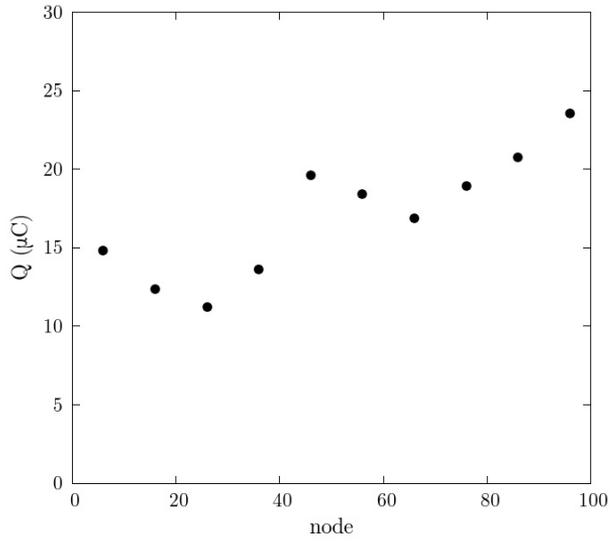


Fig. 4.22. Charge for limit pulse for several nodes for chain 4 (NOR3a-NOR3c).

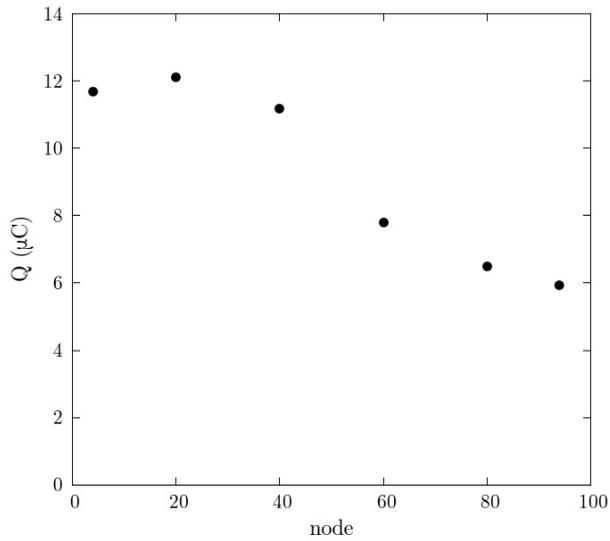


Fig. 4.23: Charge for limit pulse for several nodes for chain 10 (NAND3b).

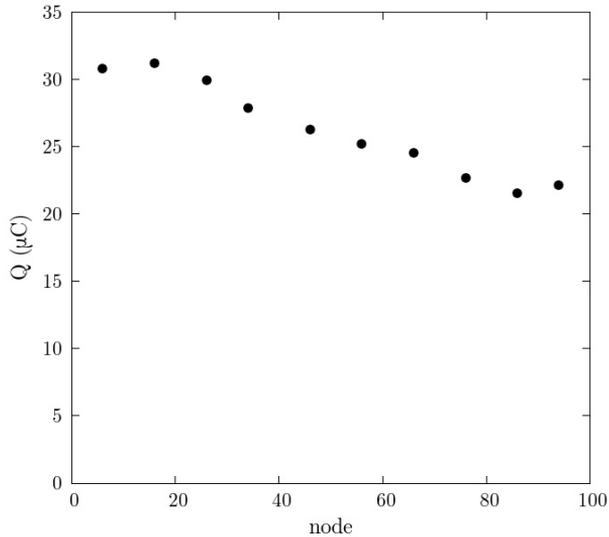


Fig. 4.24: Charge for limit pulse for several nodes for chain 12 (INV f.o. 3).

Two behaviors types are observed in the previous figures: increasing and decreasing charge with chain node. The tendency is clear in all figures although there are deviations from it in chain 1 and specially in chain 4. Since each point is obtained as an average, the cause of these effects may be geometrical.

4.4 Model validation

We compared the results of the model presented in the previous chapter to the results obtained experimentally from the circuit chains using the laser system. Since the current generated by the laser masks the current due to the chain activity, the width of the generated SET is not known and, therefore, it is not possible to adopt this straightforward method to validate the model. Instead, we validated the model through a combination of experimental data and electrical simulations. The electrical simulations were used to estimate the SET shape generated within the circuit chain with the laser from the pulse measured experimentally at the circuit output. A trail

and error technique was used to determine an in-circuit SET that after traveling the whole chain and the MUX circuitry provided the measured SET perturbation. The results shown in this section correspond to the same chain used in the previous section.

After traveling within the chain, the propagated signal passes through the multiplexer and the output PAD connected to the socket, the lines on the PCB and the oscilloscope probe. In the simulations, the effect of the socket, the lines and the probe was simulated as a lumped capacitance. The estimated value of this capacitance is about 4pF. Fig. 4.22 shows the results of the SETs obtained experimentally and the SETs obtained by simulation. The results shown correspond to the pulses measured at the PAD output with a load capacitance of 4pF. Simulation agrees with experimental data except for a deviation for pulses with widths between 1 and 2 ns due to a variation in the shape of the measured experimental pulse. The results shown in Fig. 4.22 validate the chosen value of 4pF for the load capacitance. The next step consists in finding a relationship between the pulses measured at the output (w_{out}) and the output of the chains pulses (w_{chain}). Fig. 4.23 shows a linear relation obtained by simulation:

$$w_{chain}(ns) = 1.0223 w_{out}(ns) - 0.3678 \quad (4.1)$$

Therefore, given an SET width at the output (w_{out}), the chain SET output width (w_{chain}) is obtained using equation (4.4) and the model and simulations are then used to determine to which initial SET corresponds. The comparison between model and simulation has been done taking the limit pulses at each measured node. The values obtained for chains 1, 4, 10 and 12 are shown in the next subsections.

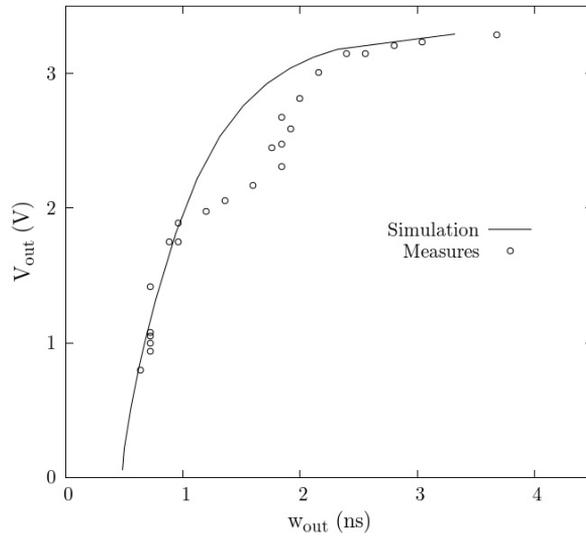


Fig. 4.25. Experimental and simulated SETs at the output of the pad.

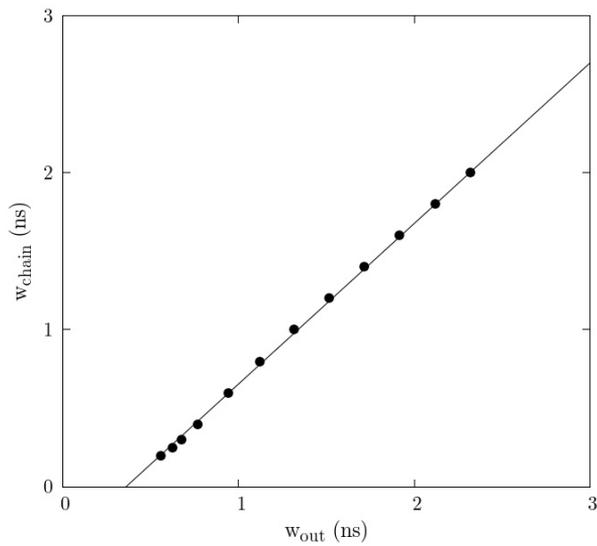


Fig. 4.26. Linear relation between w_{chain} and w_{out} .

4.4.1 Chain 1 (NAND3c-NOR3c)

Table 4.2. Comparison of model results to experimental data and simulations for chain 1.

<i>node</i>	$Q_{limit}(\mu C)$	$w_{out}(ns)$	$w_{chain}(ns)$	$w_{gen,exp}(ns)$	$w_{gen,model}(ns)$	<i>Error</i> (%)
6	21.2	15.7	15.7	3.0	3.3	9
16	12.2	13.2	13.1	1.8	2.0	12
26	8.9	11.8	11.7	1.8	1.9	8
36	7.9	10.2	10.1	1.5	1.6	10
46	9.7	9.2	9.0	1.8	1.9	7
56	9.5	8.2	8.0	2.2	2.2	4
66	9.6	6.6	6.4	1.9	1.9	2
76	8.7	5.0	4.7	1.5	1.5	1
86	7.6	3.6	3.3	1.5	1.5	1
96	6.8	1.6	1.2	0.8	0.7	9

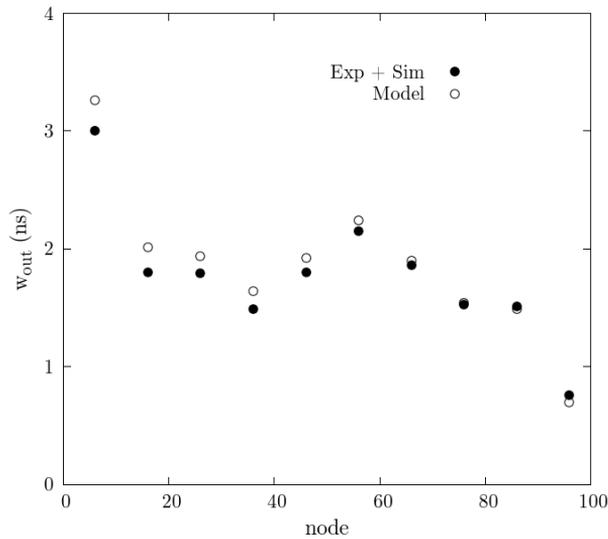


Fig. 4.27. Model vs experimental + simulation prediction of limit pulse for chain 1.

4.4.2 Chain 4 (NOR3a-NOR3c)

Table 4.3. Comparison of model results to experimental data and simulations for chain 4.

<i>node</i>	$Q_{limit}(\mu C)$	$w_{out}(ns)$	$w_{chain}(ns)$	$w_{gen,exp}(ns)$	$w_{gen,model}(ns)$	<i>Error</i> (%)
6	14.8	1.82	1.49	0.44	0.41	7
16	12.4	0.97	0.62	0.44	0.41	7
26	11.2	0.94	0.60	0.44	0.41	7
36	13.6	1.19	0.85	0.44	0.41	7
46	19.6	1.08	0.74	0.44	0.41	7
56	18.4	1.20	0.86	0.44	0.41	7
66	16.9	1.03	0.69	0.44	0.41	8
76	19.0	1.01	0.67	0.45	0.41	8
86	20.8	1.02	0.67	0.47	0.44	6
96	23.5	0.97	0.62	0.49	0.48	2

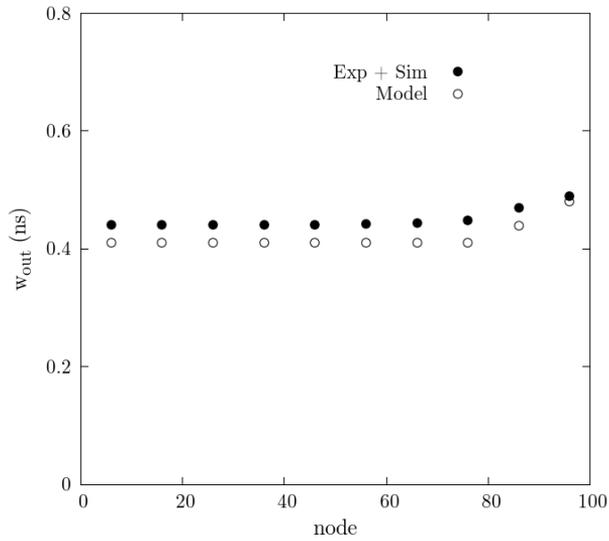


Fig. 4.28. Model vs experimental + simulation prediction of limit pulse for chain 4.

4.4.3 Chain 10 (NAND3b)

Table 4.4. Comparison of model results to experimental data and simulations for chain 10.

$node$	$Q_{limit}(\mu C)$	$w_{out}(ns)$	$w_{chain}(ns)$	$w_{gen,exp}(ns)$	$w_{gen,model}(ns)$	$Error(\%)$
4	11.7	0.72	0.37	0.915	1.04	14
20	12.1	0.72	0.37	0.875	0.92	5
40	11.2	0.72	0.37	0.817	0.805	1
60	7.8	0.72	0.37	0.747	0.7	6
80	6.5	0.72	0.37	0.648	0.6	7
94	5.9	0.64	0.29	0.49	0.54	10

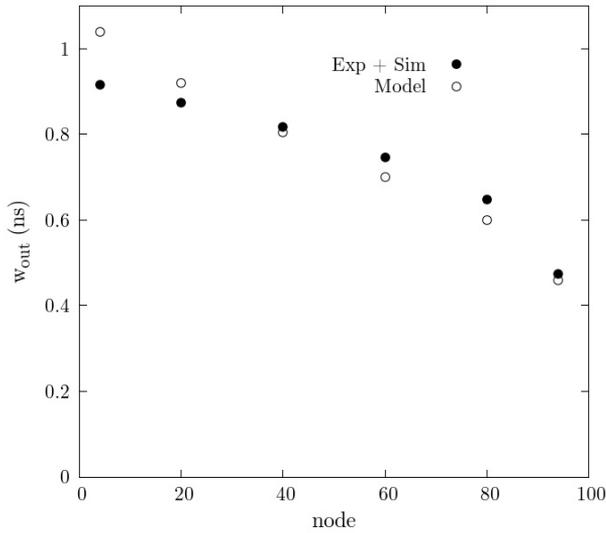


Fig. 4.29. Model vs experimental + simulation prediction of limit pulse.

4.4.4 Chain 12 (INV f.o. 3)

Table 4.5. Comparison of model results to experimental data and simulations for chain 12.

<i>node</i>	$Q_{limit}(\mu C)$	$w_{out}(ns)$	$w_{chain}(ns)$	$w_{gen,exp}(ns)$	$w_{gen,model}(ns)$	<i>Error</i> (%)
6	30.8	0.75	0.40	0.60	0.55	8
16	31.2	0.72	0.37	0.56	0.54	4
26	29.9	0.77	0.42	0.58	0.54	7
36	27.9	0.75	0.40	0.54	0.53	2
46	26.7	0.78	0.43	0.54	0.53	2
56	25.2	0.80	0.45	0.54	0.53	3
66	24.5	0.84	0.49	0.55	0.53	3
76	22.7	0.82	0.47	0.52	0.51	1
86	21.6	0.83	0.48	0.51	0.51	0
96	22.1	0.81	0.46	0.46	0.48	4

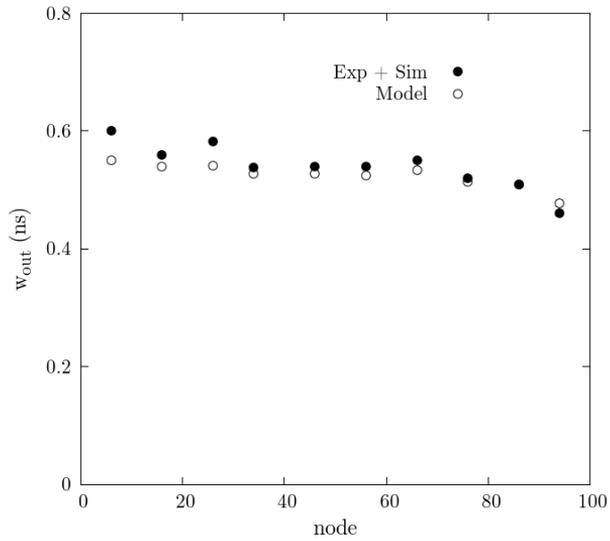


Fig. 4.30. Model vs experimental + simulation prediction of limit pulse for chain 12.

4.4.5 Results discussion

First of all, the tables and graphics from the previous subsections show that the model provides a good result compared to the combination of experimental data and simulations in all chains with a maximum error of 14% and a mean error of only 5.5%.

The broadening and narrowing effect is assessed by computing $\Delta w = w_{chain} - w_{gen}$ (columns 5 and 4 of the tables). $\Delta w > 0$ corresponds to pulse broadening whereas $\Delta w < 0$ indicates pulse narrowing. In Fig. 4.31 Δw is plotted for each node. Fig. 4.31 (a) shows a case of broadening for chain 1, and Fig. 4.31 (b) shows a case of narrowing for chain 12.

Once w_{gen} is obtained a relationship with the charge can be determined. Fig. 4.32 shows this relationship for all the measured chains. As expected, w_{gen} increases with the charge. Another interesting result is that the minimum width is almost the same for chains 4, 10 and 12 and a bit larger for chain 1. It is reasonable that the minimum SET width is similar in all the cases because the SETs are generated at the same transistors.

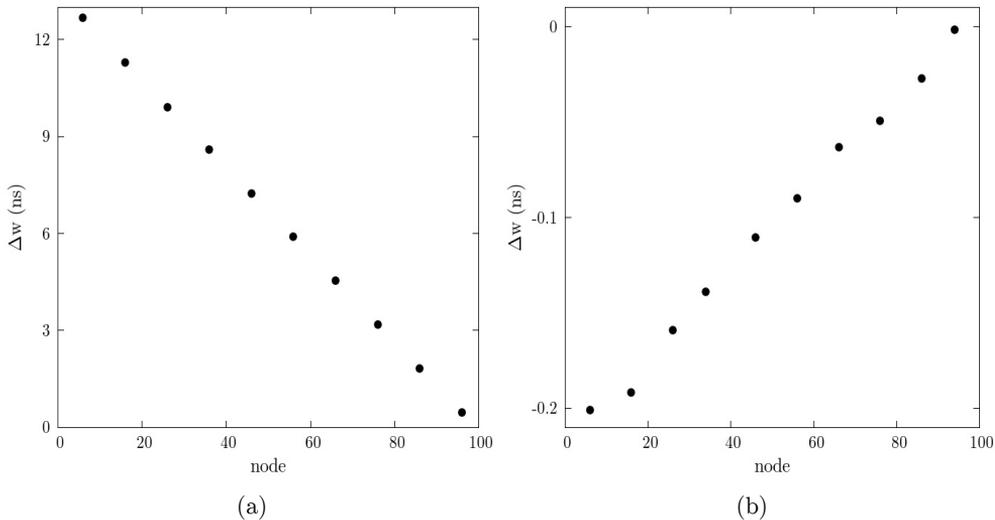


Fig. 4.31. Broadening and narrowing effects.

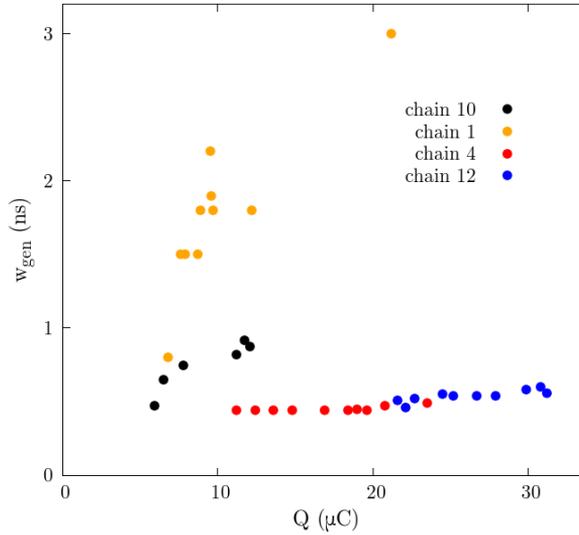


Fig. 4.32. Relation between width and charge.

4.5 Conclusions

The laser equipment has been used to generate SETs in a chain of 100 NAND gates. One of the main conclusions is that the characteristics of the SET generated depends strongly on the laser spot position and is highly sensitive to it. It is therefore crucial to have a positioning system with a good space resolution. The system used in these tests has a resolution of 50 nm, providing an acceptable margin to obtain stable signals.

The experimental limitations encountered to determine the width of the generated SET requires validating the model presented in Chapter 3 by combining experimental data and simulation results. The validation of the model for this technology also indicates the usefulness of the model for various technologies.

Regarding model accuracy, the larger error on the predicted SET width observed is of 14% for the node closer to the output. It is a significant error but it is obtained for a case where the SET propagates through 96 gates, implying a highly recursive model application (96 times) that will be

difficult to obtain in real circuits. Typical error for a 10-20 gates propagations is below 7% which is an acceptable error for a more realistic chain depth.

Chapter 5

Latch perturbation analysis

As explained previously, an SEU consists in the change of a memory element state, and may be due to an SET being captured by a latch when it is transparent, or by a direct particle impact within the memory element. The propagation of an SET has been studied in the previous chapter, while the conditions for an SET capture are covered in the next chapter. The first part of this chapter is dedicated to the study of SEUs originated directly from particle impacts within the latch. This effect is known from long time and has been widely studied [Dodd03]. The impact of a given ionizing particle on a memory element depends on the particle characteristics like energy, impact point within the circuit or travel direction, as well as on various intrinsic memory cell characteristics related to latch metastability [Noi93], [Kim90] or the cell static noise margins (SNM) [Loh79], [See87]. While SNM characterizes DC noise impact on the latch element, an important parameter to characterize SEU in ICs is the critical charge (Q_{crit})

as it encloses the cell dynamic characteristics [Jah09]. The SNM of a memory cell is a static parameter whose calculation requires simulating the memory element and can be computed either when the latch is isolated (eliminating the topological feedback), or when the cell is being accessed (by simulating an equivalent circuit configuration). Although providing an estimation of a given memory element robustness, the SNM represents a static parameter with inherent limitations to describe dynamic phenomena like the memory cell response to transient ionizing events.

Q_{crit} is the minimum amount of charge that, injected at a memory node, produces a change of the stored logic value, and is typically used to categorize the memory robustness in radiation environments.

This chapter develops an approach to determine the latch sensitivity to particle strikes hitting an internal node by combining the study of the latch stability with the perturbation at a latch node. This method is used to develop a model for the critical charge.

The second part of the chapter is dedicated to the study the latch capture of SETs. As pointed in the previous chapter, an SET can propagate through a combinational circuit reaching a memory element, giving rise to an effective SEU if it is captured. Some conditions must be held to capture an SET [Dod04]:

- There is at least one open logic path to the memory element.
- SET duration and height are sufficient to propagate without being filtered out electrically.
- SET must arrive at the memory element while it is transparent.
- SET must be capable of causing a flip.

The last two conditions, related to the timing conditions and the SET characteristics respectively, are treated in this chapter. Regarding the timing conditions for SET capture, the common approach is to define the capture probability in terms of the latch window - the time interval in which the SET can propagate through the latch. This window, also known as WOV (window of vulnerability), is defined by the latch setup and hold times [Baz06] and is used to compute the probability of capture as the WOV divided by the clock period [Sei01], [Oma07], [Isl12]. However, the definition

of the WOV used in these works doesn't include the SET width, which is a decisive factor for latch capture probability [Ben06], because a wider SET is more likely to happen in the window than a short one. In [Dhi06] the circuit unreliability is defined as the sum of the SET width at the circuit outputs. A more accurate approach consists in calculating the capture probability as $P = (pw-w)/T$, where pw is the pulse width, w is the latching window size of the latch and T is the clock period [Shi02], [Zha06]. All these works consider only full- V_{dd} SETs, omitting a wide range of non-full V_{dd} SETs than can actually be captured by a latch. Simple electrical simulations show that, in general, a non full- V_{dd} SET pulse injected at a gate input capable of traversing a logic path gains a full V_{dd} voltage excursion within the first or second gates traversed [Gil12]. Moreover, SET pulses generated toward the circuit output will experience a smaller logic and electrical filtering than SET pulses occurring toward the circuit inputs, as they need to traverse a smaller number of gates to reach the circuit output. Such a smaller logic and electrical filtering may even increase the ratio of non-full V_{dd} SETs reaching the circuit output, making the analysis of their latching condition more relevant. Modern CMOS ICs logic depth is decreasing as technology scales down to fulfill the overall frequency requirements. In [Liu12] the optimal logic depth, in terms of energy per operation, for a 65nm CMOS inverters chain is found to be only 8. As a first approximation, the percentage of logic gates whose input nodes are two gates away from the circuit output on a combinational circuit with a mean logic depth of 10 is 20%. Therefore SET pulses originated within the circuit region corresponding to the two last circuit stages may reach a memory element without having gained a full V_{dd} voltage excursion.

This chapter provides a detailed analysis of the necessary conditions for a given SET to be captured by a memory element in terms of SET width and also height.

5.1 Latch stability

In digital circuits, the latch is the basic element of storage having two stable states corresponding to the two values that can be stored. The latch considered in this chapter is the conventional two-inverter latch used in many previous works as a reference [Oma07], [Nic08]. The structure of this latch is shown in Fig. 5.1. It consists of two inverters connected in a feedback loop. The two stable states depend on the values of the internal nodes of the latch (A and B): one state has node A at high value and node B at low value, while the other corresponds to node A at low value and B at high value. Any other state of the latch, denoted as the voltage values of their nodes (V_A , V_B), tend to one of the stable states (0 , V_{dd}) or (V_{dd} , 0). There is another non-stable state – called the metastable state – in which the internal nodes A and B are at self-consistent voltage values (V_{Am} , V_{Bm}) different from those of stable states, where the system can remain indefinitely. Differently from a stable state, a small perturbation when the system is in this metastable state brings it back to one of the stable states, or causes indefinite oscillations.

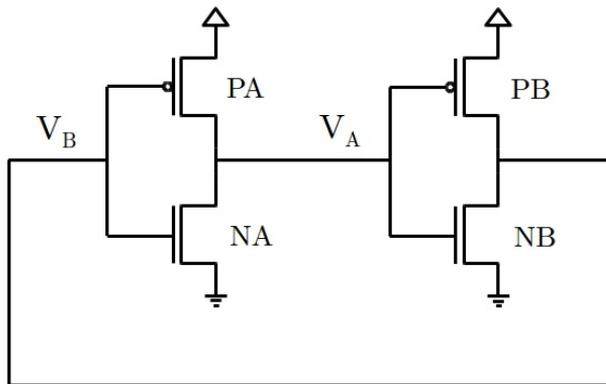


Fig. 5.1. Two-inverter Latch.

The dynamic behavior of a latch is similar to the behavior of a mechanical system under the influence of a field (gravitational, electric, etc.). In such

systems the potential diagrams provide relevant information like the forbidden regions or the stable points. In a gravitational field, for example, the potential diagram is defined by the system gravitational potential $V(r)$, with r being the distance to the object that generates the field. The proposed analog to $V(r)$ for a two-node latch element is the energy that the system dissipates when evolves from the initial state (V_{Ai}, V_{Bi}) to one of the final stable states, $(0, V_{dd})$ or $(V_{dd}, 0)$ and is denoted as $E(V_{Ai}, V_{Bi})$. It is computed using Eq. 5.1 with data from electrical simulations.

$$E = \left| \int V_A I_{NA} dt \right| + \left| \int (V_{dd} - V_A) I_{PA} dt \right| + \left| \int V_B I_{NB} dt \right| + \left| \int (V_{dd} - V_B) I_{PB} dt \right| \quad (5.1)$$

The initial simulation conditions of V_A and V_B are settled and the system evolution simulated until a stable final value. The obtained curves of V_A and V_B and the currents through all the transistors are then used to compute E . The integration time corresponds to the time that the system requires to reach one of the stable states. In the latch case, if the system reaches metastability, it can remain for an indefinite time in a state where all transistors are conducting, and the energy value increases for initial values close to metastability. When the initial states coincide exactly to metastable states, E tends to infinite. Fig. 5.2 shows E as a function of the initial state of the latch. It is zero for the initial states coinciding with the stable states $(0, V_{dd})$ and $(V_{dd}, 0)$, and tends to infinite for the points over a line called in this work the *Line Switch Contour* (LSC). This concept is defined in the next section. However, this analogy is not completely valid because the latch system doesn't represent a conservative field and the energy depends on the path to the final state. In any case, it provides a valid picture of the latch stability.

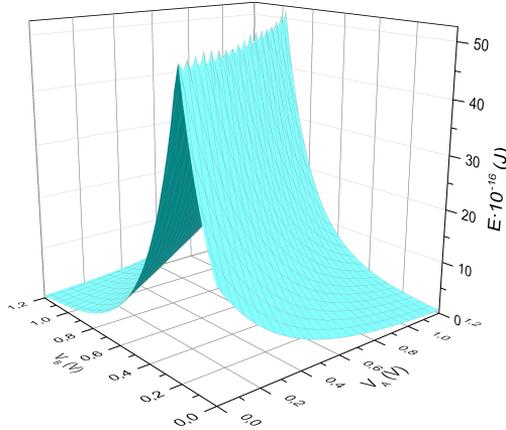


Fig. 5.2. $E(V_A, V_B)$ plot for a 65nm commercial technology two-inverter latch.

5.2 Line Switch Contour

Fig. 5.3 shows the latch behavior for various initial states. Fig. 5.3 (a) shows the latch state diagram, with node A voltage in the x axis, and node B voltage in the y axis. Fig 5.3 (b) shows the time evolution of each node for three cases: Case 1 evolving to $(0, V_{dd})$, Case 2 with final state $(V_{dd}, 0)$, and Case 3 evolving to metastability. The curves were obtained from electrical simulations of a latch built with transistors from a 65nm CMOS commercial technology. Case 1 starts from the initial state $(V_A = 0.4V, V_B = 0.8V)$ from where it evolves to $(0, V_{dd})$. On the contrary, Case 2 starts from $(V_A = 0.9V, V_B = 0.8V)$ and ends at $(V_{dd}, 0)$. Note that the two initial states lay at different V_A - V_B plane regions that are separated by the diagonal dashed line. This line represents the (V_A, V_B) values of the initial states that tend to metastability which we call the *Line Switching Contour* (LSC). This line has been presented in previous works and there are several ways to compute it [Loh79], [See87] and [Gil12]. This last one is developed in the next section. The latch behavior for an initial state on the LSC is represented in Case 3, where the latch evolves from $(V_A = 0.4V, V_B = 0.4V)$ to the metastable point, that for the latch in the example is $(V_A = 0.59V, V_B = 0.59V)$. Since

the latch designed is perfectly balanced, the LSC contains the diagonal points $V_A = V_B$.

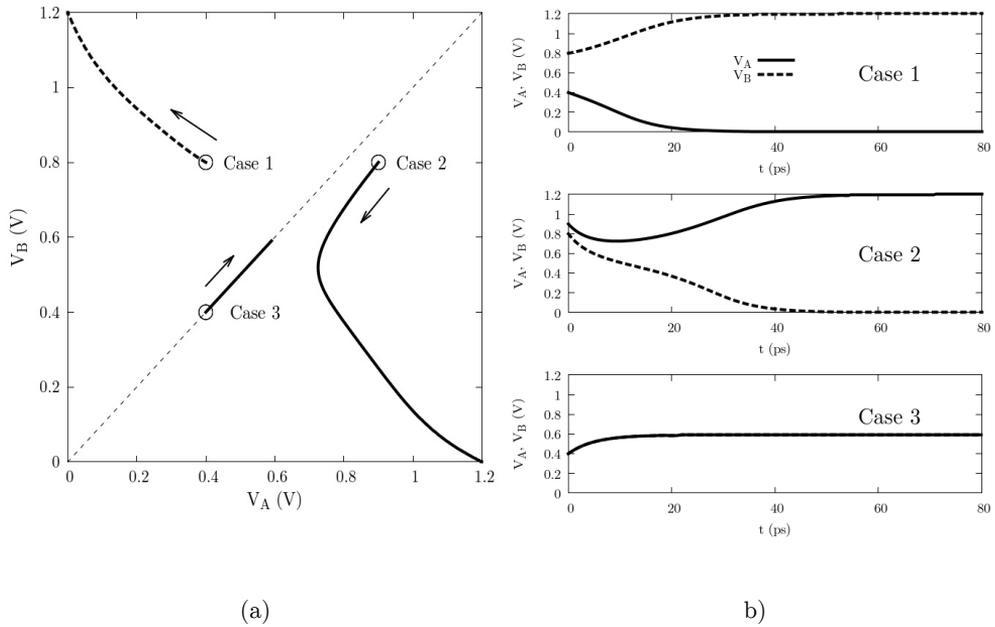


Fig. 5.3. State diagram and time evolution of node voltages for a balanced latch.

Fig. 5.4 shows the same simulations performed for a non-balanced latch obtained by doubling the NA and PA transistors widths. The notation for this latch is 2X-1X instead of 1X-1X for the balanced one. The same initial states taken for the balanced latch are used in Case 1 and Case 2. The most relevant result for the unbalanced latch is that the LSC doesn't coincide with the diagonal, implying that there are initial states that for the balanced latch ended up at $(V_{dd}, 0)$, that for the unbalanced latch end at $(0, V_{dd})$.

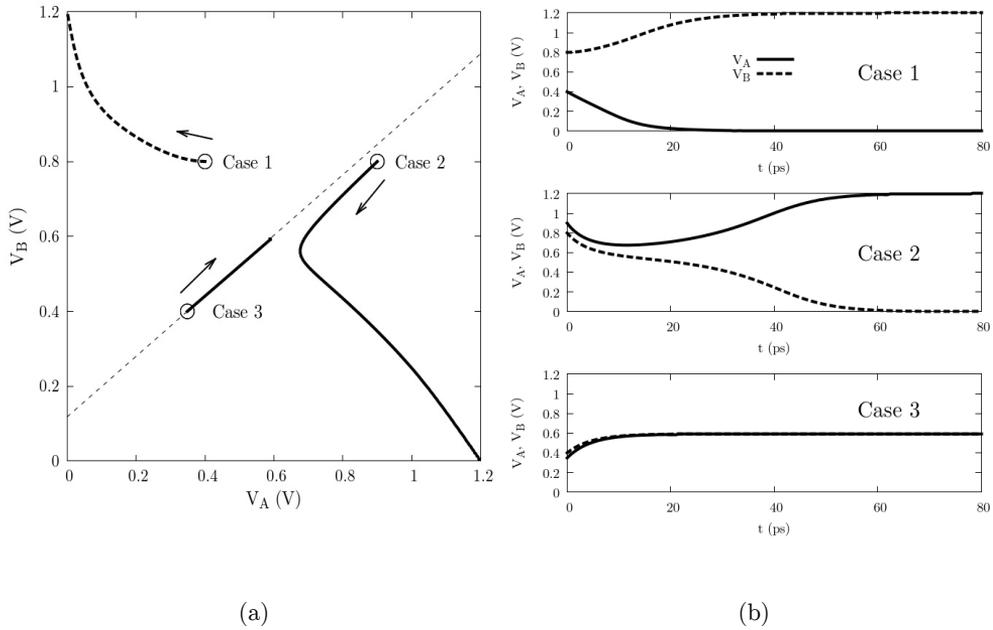


Fig. 5.4. State diagram and time evolution of node voltages for an unbalanced latch.

Fig. 5.5 (a) represents the 4X-1X latch (the widths of transistors NA and PA are multiplied by 4) together with the 1X-1X and 2X-1X latches, showing that the larger circuit asymmetry, the higher the diagonal deviation from the balanced case. However, a latch with such a mismatch is not a realistic case. In contrast, the 2X case can represent a real mismatch compared to the results obtained when variations are applied to a 1X latch. Fig. 5.5 (b) shows ten LSCs obtained from a Monte-Carlo analysis of a 1X latch. Even though the number of different LSCs shown is small, deviations similar to those for the 2X latch are obtained.

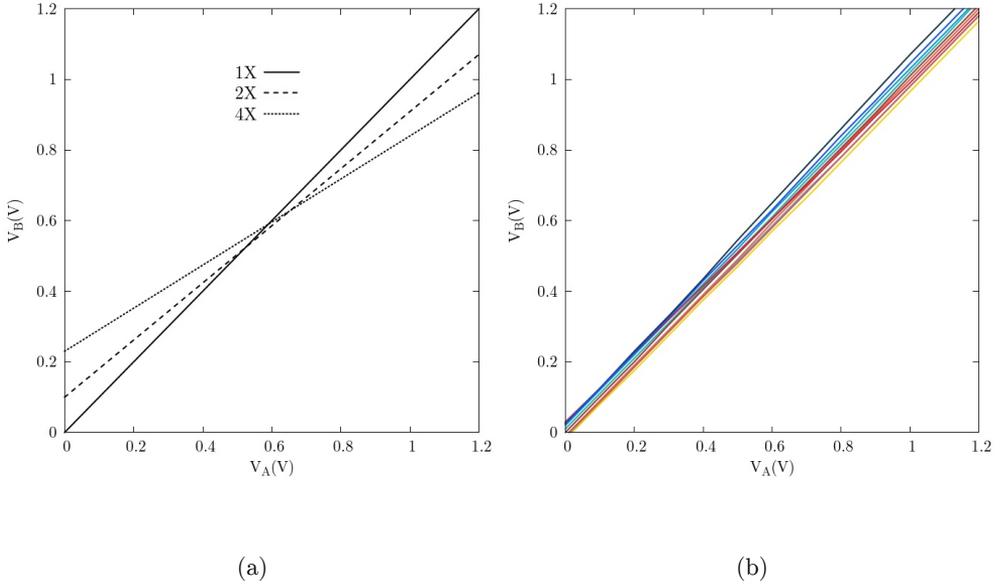


Fig. 5.5. LSC for 1X, 2X, 4X (a) compared to 1X Monte-Carlo (b).

The determination of the LSC requires obtaining the analytical relationship $V_B(V_A)$. Assuming that the LSC is a straight line [Noi93], its expression is of the form $V_B = mV_A + V_{B0}$ and only two points are required to define it. We concentrate on points P1 and P2 as shown in Fig. 5.6 that are computed as follows:

P1: It corresponds to $(0, V_{B1})$. In this case $V_A = 0$ and V_B is small for what we assume that initially $I_{NA} = I_{NB} = 0$ and that both *PA* and *PB* transistors are in the saturation region. The point P1 is given by the V_B value (V_{B1}) for which I_{PA} and I_{PB} are equal. A V_B voltage higher than V_{B1} implies $I_{PA} < I_{PB}$ and that node A will be set to zero, reaching the final state $(V_A, V_B) = (0, V_{dd})$. On the other hand, if $V_B < V_{B1}$, then $I_{PA} > I_{PB}$ and the final state is $(V_A, V_B) = (V_{dd}, 0)$.

P1 is obtained by equating the currents at transistors PA and PB:

$$\frac{1}{2}\beta_{PA}(V_{dd} - V_{B1} - V_{TPA})^2 = \frac{1}{2}\beta_{PB}(V_{dd} - V_A - V_{TPB})^2 \quad (5.2)$$

Where V_{TPA} and V_{TPB} are the threshold voltages of PA and PB respectively. From (5.2) an expression for V_{B1} is obtained:

$$V_{B1} = V_{dd} - V_{TPA} - (V_{dd} - V_{TPB}) \sqrt{\frac{\beta_{PB}}{\beta_{PA}}} \quad (5.3)$$

P2: It corresponds to (V_{dd}, V_{B2}) . In this case $V_A = V_{dd}$, $I_{PA} = I_{PB} = 0$ and both NA and NB transistors are in the saturation region. Analogously to (5.3) the V_B value of P2 is obtained:

$$V_{B2} = V_{TNA} + (V_{dd} - V_{TNB}) \sqrt{\frac{\beta_{NB}}{\beta_{NA}}} \quad (5.4)$$

The parameters of the line defining the LSC $V_B = mV_A + V_{B0}$ are easily obtained. Parameter V_{B0} coincides with V_{B1} and m is obtained as:

$$m = \frac{V_{B2} - V_{B1}}{V_{A2} - V_{A1}} \quad (5.5)$$

with $V_{A2} = V_{dd}$ and $V_{A1} = 0$.

Being the LSC of a latch $V_B = mV_A + V_{B0}$ and (V_A, V_B) its initial state, if $V_B > mV_A + V_{B0}$, then the final state will be $(0, V_{dd})$, while if $V_B < mV_A + V_{B0}$ then the final state will be $(V_{dd}, 0)$.

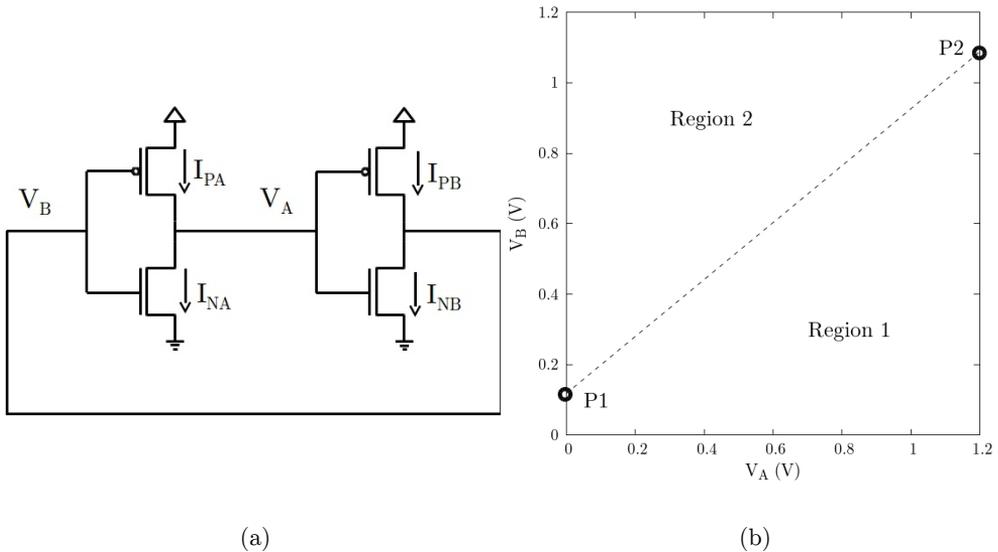


Fig. 5.6. Convention of transistor currents (a) and points P1 and P2 determining the LSC (b).

Although the LSC represents a static situation, it also accounts for the latch dynamics as it is computed through the system evolution. Therefore, the LSC provides more qualitative information about latch stability against radiation than the SNM (that accounts only for DC perturbations) as observed in Fig. 5.7. In this figure, the diagrams used to calculate the SNM for 1X, 2X and 4X latches are compared to the LSC lines. The SNM diagrams are quite similar for the three cases, while the LSC lines account for the latch mismatch and, therefore, for the latch robustness.

The LSC itself is a measure of robustness because the larger the distance between the points P1 and P2, the more robust the latch is. At this point the question of whether this distance can be used as a metric arises. The answer is that this distance can be a qualitative estimation of robustness but, as shown in next section, when the latch is perturbed the LSC approach is not valid.

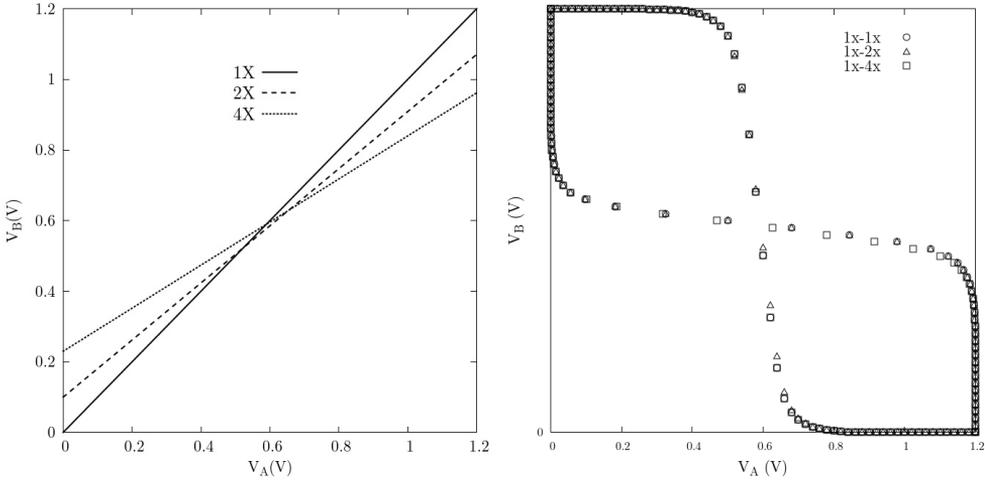


Fig. 5.7. LSC vs. diagrams for 1X, 2X and 4X latches.

5.3 Latch current perturbation

Although the LSC determination is obtained from a dynamic analysis, it represents a static situation and does not provide any information about whether it can be crossed, providing only a qualitative information about cell robustness. However, it can be complemented with a perturbation analysis to analyze such latch robustness. Depending on the impacted transistor and assuming that the impact takes place at the transistor drain, four situations may occur (Fig 5.8).

If the initial state is $(V_A, V_B) = (0, V_{dd})$ and a particle strikes transistor PA, the current generated increases the voltage at node A (I arrow in Fig. 5.8). It can reach a value high enough to diminish V_B to a point where the feedback favors the state change. With the latch in the same initial state, if transistor NB is impacted, the current diminishes V_B (II arrow) leading to a flip. On the other hand, if the initial state is $(V_A, V_B) = (V_{dd}, 0)$, a strike at PB increases V_B (III arrow) and an impact at transistor NA generates a current that diminishes V_A (IV arrow) and may produce a flip.

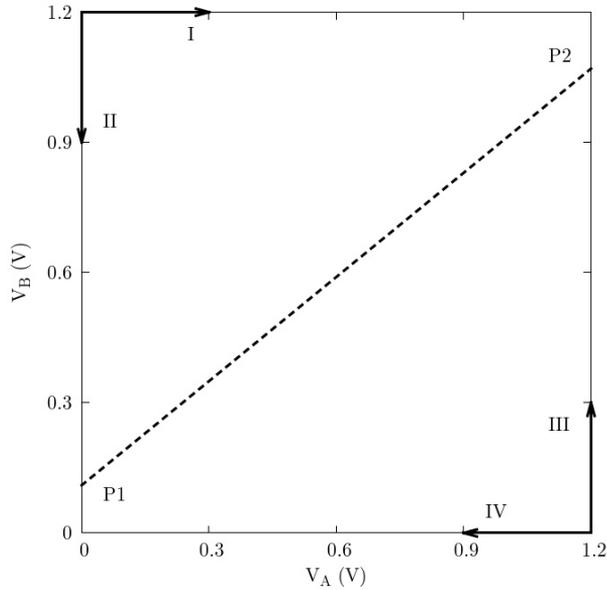


Fig. 5.8. Four directions of latch voltages evolution after a perturbation.

The current perturbation most extensively used is a double exponential pulse (Eq. 5.6). Such a pulse is based on the study in [Mes82] where the current generated by a particle strike is estimated. It can be injected at the nodes of the latch to simulate the current generated by the impact of a particle at a transistor.

$$I(t) = I_0 \left(e^{-t/\tau_a} - e^{-t/\tau_\beta} \right) \quad (5.6)$$

where:

- I_0 defines the scale of the current.
- τ_a is a constant related to the falling time of the pulse.
- τ_β is related to the rising time of the pulse.

If the perturbation leads the latch to a state beyond the LSC (i.e.: if the line connecting the initial state with the final state after the perturbation crosses the LSC), then there will be a latch state flip as illustrated in Fig.

5.8. From initial state $(0, V_{dd})$, if perturbations I and II take the latch to states beyond P1 and P2 respectively, the latch flips to state $(V_{dd}, 0)$. On the contrary, from initial state $(V_{dd}, 0)$, if perturbations III and IV take the latch to states beyond P2 and P1 respectively, the latch will flip to state $(0, V_{dd})$. This situation was simulated for a 2X mismatch latch from a commercial 65nm CMOS technology transistors with a voltage supply $V_{dd} = 1.2V$. The V_A and V_B values at each point correspond to the cell values immediately after the perturbation. The perturbation was considered to be finished when it reached a 1% of its maximum. These points are plotted on a graph together with the LSC (Fig. 5.9). The initial state considered is $(V_A, V_B) = (V_{dd}, 0)$. Therefore if $V_B > mV_A + V_{B0}$ the state changes, while if $V_B < mV_A + V_{B0}$ then the cell remains at the same state. The result is that all the points above the theoretical LSC correspond to (V_A, V_B) values that switch the latch state as indicated by simulations (red points). Also, all the points below the LSC correspond to (V_A, V_B) values that don't flip the latch when simulated (green triangles).

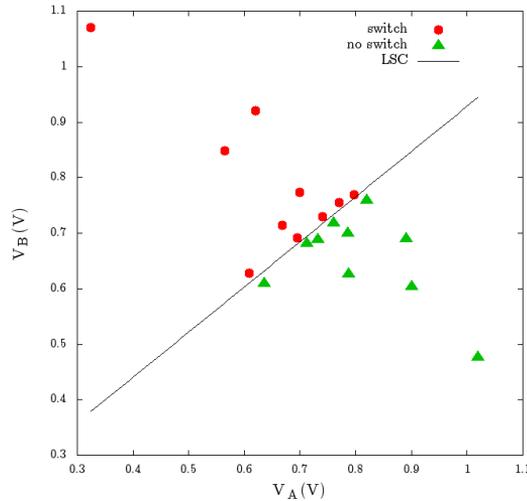


Fig. 5.9. Developed model and simulation results comparison. Switch (circles) and no switch (triangles) computed at the end of the perturbation separated by the LSC computed using the method in section 5.2.

A detailed analysis shows that the perturbation generated by a particle impact does not require bringing the latch to a state beyond the LSC to provoke a flip. Figures 5.10 and 5.11 show the V_A - V_B diagram and the time evolution of a balanced latch with an injected double exponential current perturbation that doesn't flip the latch (5.10) and another one that flips it (5.11). Both perturbations have the same time constants and parameter I_0 is varied to change the current pulse. Obviously, the perturbation flipping the latch is larger than the perturbation that doesn't flip it, but Fig. 5.11 shows that it is not required reaching P2 of the LSC to induce a memory flip. Instead, it is enough reaching a value slightly above $V_{dd}/2$.

An interpretation is that the effect of a current perturbation on the LSC is a displacement of the points that define it, as shown in Fig. 5.12. As a consequence of the perturbation, a new point P2' represents a new limit value that must be reached to induce a state change. The position of this new point is determined analytically below.

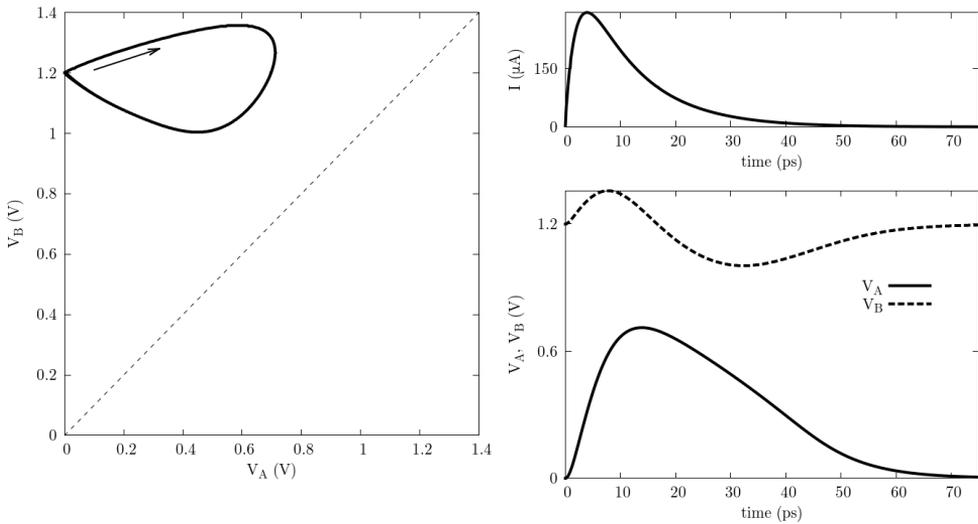


Fig. 5.10. Current perturbation that doesn't flip the latch.

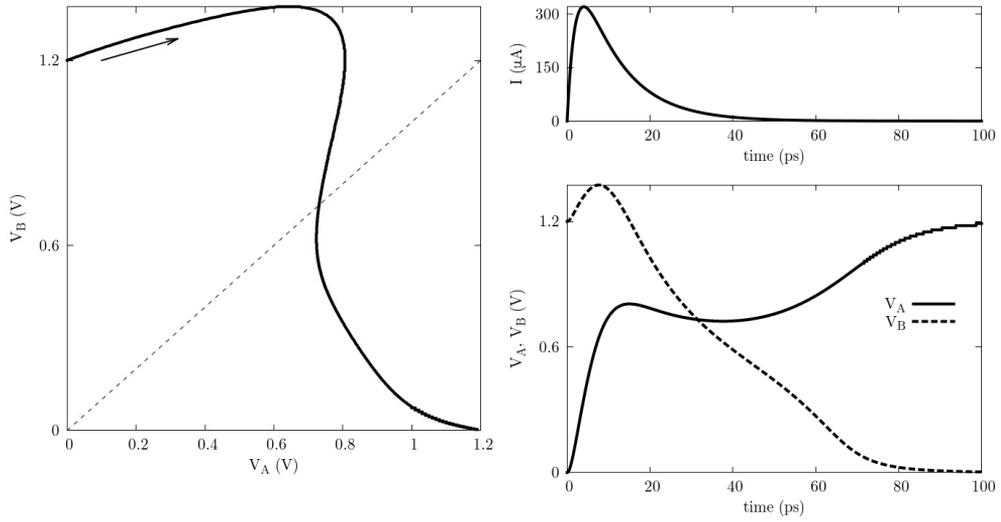


Fig. 5.11. Current perturbation flipping the latch.

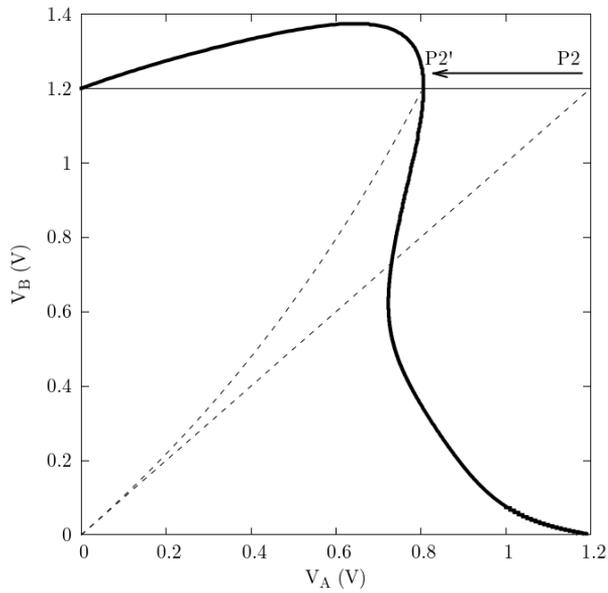


Fig. 5.12. Displacement of the LSC due to a current perturbation.

The case shown in Fig. 5.12 corresponds to initial state $(0, V_{dd})$, with a perturbation that increases V_A . To get a flip, V_A must exceed the new limit $(V_A, V_B) = (V_{AL}, V_{dd})$. To determine the value of V_{AL} the same technique used to find the points P1 and P2 of the LSC is applied. The only difference is that now the double exponential current must be included:

$$\frac{1}{2}\beta_{NA}(V_B - V_{TNA}) + I_0(e^{-t/\tau_a} - e^{-t/\tau_\beta}) = \frac{1}{2}\beta_{NB}(V_{AL} - V_{TNB}) \quad (5.7)$$

And obtain:

$$V_{AL} = V_{TNB} + \frac{\beta_{NA}}{\beta_{NB}}(V_{dd} - V_{TNA}) - \frac{2I_0}{\beta_{NB}}(e^{-t/\tau_a} - e^{-t/\tau_\beta}) \quad (5.8)$$

This result is used in the next section to obtain an analytical expression for the latch critical charge.

5.4 Critical charge

The critical charge (Q_{crit}) is a widely used metric for the latch robustness. It is defined as the minimum charge required to modify the stored logic value. It is typically evaluated by simulation injecting a set of current pulses and determining the smallest one being capable of modifying the cell state. Q_{crit} is computed as the time integral of the injected current. Even though several pulse shapes have been proposed and used [Nas07], the current pulse mostly used is the double exponential [Oma07], [Din06], defined in Eq. (5.6). Then Q_{crit} is computed as:

$$Q_{crit} = \int I(t) dt = \int I_0(e^{-t/\tau_a} - e^{-t/\tau_\beta}) dt \quad (5.9)$$

The result of this integral is:

$$Q_{crit} = I_0 (\tau_a - \tau_\beta) \quad (5.10)$$

It is known that its value strongly depends on the current pulse shape [Dod95]. Fig. 5.13 shows a set of curves obtained by simulation on a 65nm CMOS commercial technology. Parameter τ_a is represented in the horizontal axis, while I_0 is represented in the vertical axis. Therefore, each point in the graph represents a different double exponential current pulse. The solid line represents the cell switch curve separating the set of pulses that flip the cell from those that don't flip it. Points above the switch curve flip the cell, while points below it don't flip it. The four dashed lines in the graph correspond iso- Q curves. It means that each line represents a set of pulses with the same Q value. The figure shows that it is possible to get many different pulses with the same Q value, some of which will flip the cell while the others will not. This effect indicates the importance of defining Q_{crit} for different pulses.

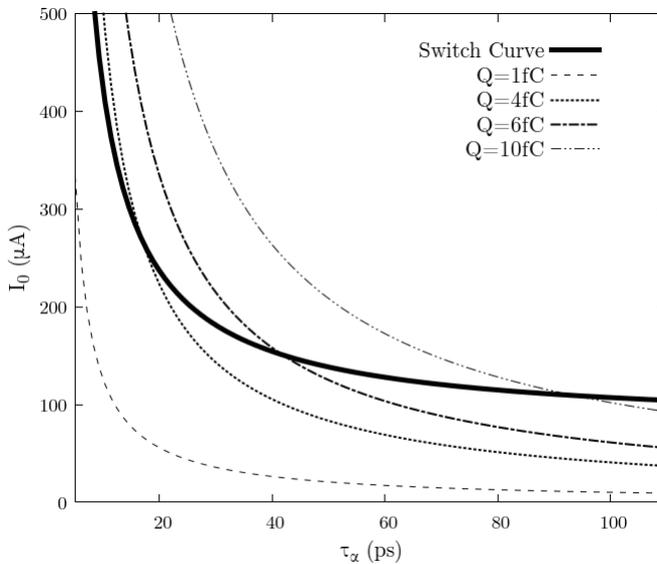


Fig. 5.13. Switch curve and sets of pulses with the same Q_{crit} .

Since the Q_{crit} is accepted as the main metric for the latch robustness, a model to compute analytically this magnitude has been developed. It is based on the LSC and the displacement suffered by the points defining it when a current perturbation is injected. Fig. 5.14 shows the evolution of a latch when a current perturbation is injected, leading the system to metastability. It is observed that V_A increases until a maximum $V_{A\ max}$. If $V_{A\ max}$ is lower than V_{AL} , the cell does not flip, while if $V_{A\ max}$ is larger than V_{AL} the cell flips. The perturbation leading the cell to a $V_{A\ max}$ equal to V_{AL} represents the perturbation carrying a charge equal to Q_{crit} . Therefore, the procedure to find an analytical equation for Q_{crit} consists in:

- Compute V_{AL} with Eq. (4.7).
- Find $V_{A\ max}$.
- Equate both expressions $V_{A\ max} = V_{AL}$ to obtain a relation for the double exponential parameters.
- Use Eq. (4.9) to obtain Q_{crit} .

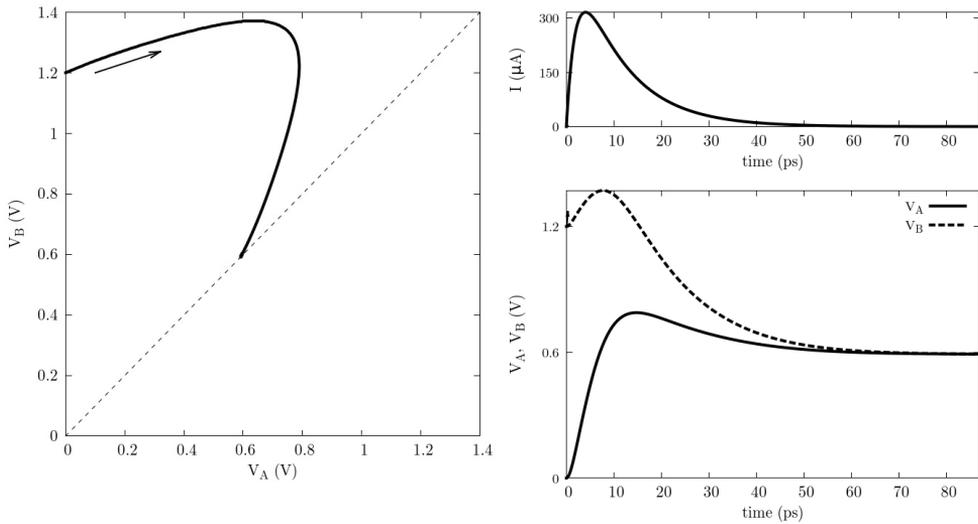


Fig. 5.14. Current perturbation leading to metastability.

First, an expression for V_A is obtained by solving:

$$C_A \frac{dV_A}{dt} = I_0 \left(e^{-t/\tau_a} - e^{-t/\tau_\beta} \right) - \frac{1}{2} \beta_{NA} V_A \quad (5.11)$$

Assuming that $V_B = V_{dd}$ and that, therefore, transistor PA is off, the solution to this equation is:

$$V_A = \frac{I_0 / C_A}{r - 1/\tau_a} \left(e^{-t/\tau_a} - e^{-rt} \right) - \frac{I_0 / C_A}{r - 1/\tau_\beta} \left(e^{-t/\tau_\beta} - e^{-rt} \right) \quad (5.12)$$

Where $r = \beta_{NA} / 2C_A$ and C_A is the capacitance of node A.

The maximum of this function appears approximately at a time:

$$t_{max} \approx \frac{1}{r - 1/\tau_a} \ln \left[\frac{r(\tau_a - \tau_\beta)}{1 - r\tau_\beta} \right] \quad (5.13)$$

Then $V_{Amax} = V_A(t_{max})$ and can be written as:

$$V_{Amax} = I_0 R(t_{max}) \quad (5.14)$$

With

$$R(t_{max}) = \frac{\left(e^{-t_{max}/\tau_a} - e^{-rt_{max}} \right)}{C_A (r - 1/\tau_a)} - \frac{\left(e^{-t_{max}/\tau_\beta} - e^{-rt_{max}} \right)}{C_A (r - 1/\tau_\beta)} \quad (5.15)$$

To have a cell flip, the condition $V_{Amax} > V_{AL}$ needs to be hold. Therefore equating $V_{Amax} = V_{AL}$, and using $I_0 = Q(\tau_a - \tau_\beta)$, the following expression can be obtained:

$$Q_{crit} = \frac{V_{TNB} + \frac{\beta_{NA}}{\beta_{NB}} (V_{dd} - V_{TNA})}{R(t_{max}) + \frac{2}{\beta_{NB}} \left(e^{-t_{max}/\tau_a} - e^{-t_{max}/\tau_\beta} \right)} (\tau_a - \tau_\beta) \quad (5.16)$$

In the development the voltage of the struck node was $V_A=0$ and the injected pulse was a positive current. If the struck node is at V_{dd} , the expression for the critical charge can be found in a similar way. The difference is that the n-MOS transistors are now off and the p-MOS ones are conducting. The procedure in this case is the same changing V_A by $V_{dd}-V_A$, and therefore now the quantity $V_{dd}-V_A$ has to be maximum and that $V_{dd}-V_A=I_0R(t_{max})$. The expression for t_{max} is the same changing β_{NA} by β_{PA} in the definition of r , getting:

$$Q_{crit} = \frac{V_{TPB} + \frac{\beta_{PA}}{\beta_{PB}} (V_{dd} - V_{TPA})}{R(t_{max}) + \frac{2}{\beta_{PB}} \left(e^{-t_{max}/\tau_a} - e^{-t_{max}/\tau_\beta} \right)} (\tau_a - \tau_\beta) \quad (5.17)$$

5.5 SET capture

The parameters determining the latch capture are related to both SET and latch characteristics. SET voltage and duration determine the capability of the SET to change the latch state, and the SET initial time together with the latch setup and hold times establish the conditions for the timing requirements for SET capture. The conditions that must be held in order to capture an SET are [Fer13]:

- The pulse must arrive to the memory element input with a time margin with respect to the clock edge of at least the latch setup time.
- The pulse must remain at the latch input for, at least, a time equal

to the latch hold time.

These conditions can be expressed mathematically as:

$$\begin{aligned} t_{\text{ini}} &\leq t_{\uparrow} - t_{\text{setup}} \\ t_{\text{end}} &\geq t_{\uparrow} + t_{\text{hold}} \end{aligned} \quad (5.18)$$

Where t_{ini} and t_{end} are the initial and end times of the pulse respectively, and t_{\uparrow} is the time at which the rising flank of the clock occurs (Fig. 5.15). Equation (5.18) can be rearranged in terms of SET parameters such as the pulse duration (w) and the distance between the initial time of the pulse and the clock flank ($\Delta t = t_{\uparrow} - t_{\text{ini}}$):

$$\begin{aligned} \Delta t &\geq t_{\text{setup}} \\ \Delta t &\leq w - t_{\text{hold}} \end{aligned} \quad (5.19)$$

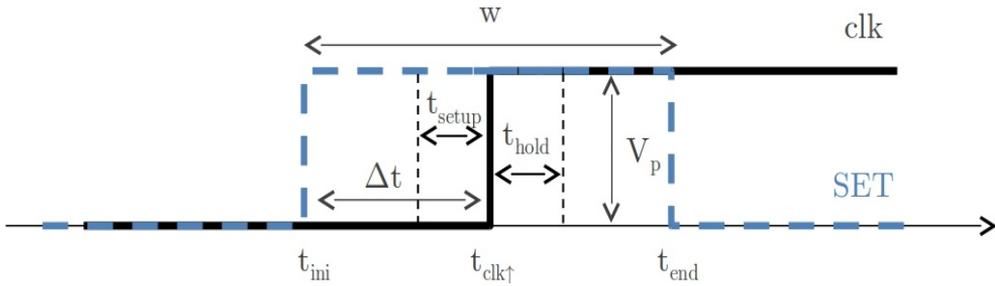


Fig. 5.15. Nomenclature.

To observe the dependence of the SET capture with SET voltage, electrical simulations were performed to obtain upper ($w - t_{\text{hold}}$) and lower (t_{setup}) bounds for Δt as a function of w for various pulse heights (V_p). Fig. 5.16 (a) shows, in the regions of the $\Delta t - w$ space, such bounds for a library flip flop taken from a commercial 65nm CMOS technology. The dashed region corresponds to full V_{dd} SET pulses, while each colored region corresponds to one subsequent lower V_p . All the pulses contained within the region borders correspond to pulses being captured by the latch. The maximum value taken

for w is one clock period because SET with larger widths always get captured. The graph in Fig. 5.16 (b) shows a bar diagram representing the values of the areas for each V_p normalized to the largest one.

Fig. 5.16 reveals that the lower bound (the setup time) depends on the SET pulse duration, and that the upper bound for V_{dd} pulses intersects the upper bound of lower V_p values. Such behavior is due to the shape of the pulses considered for which (as explained in Chapter 3), to be more realistic, the rise and fall times depend on whether the pulse reaches full V_{dd} or not, i.e.:

- fixed rise time for pulses with $V_p = V_{dd}$.
- rise time depending on SET width (w) for $V_p < V_{dd}$.

The area of a pulse reaching V_{dd} is the largest one, being smaller for lower values of V_p . These areas are related to the probability of a pulse to get captured as will be shown in the next section.

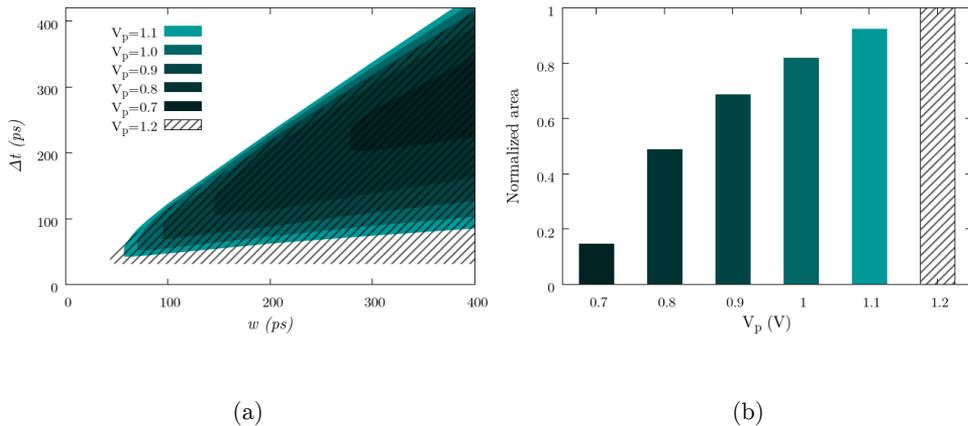


Fig. 5.16. $\Delta t - w$ graphic for several values of V_p and normalized areas.

5.6 Capture probability

An SET pulse with a sufficient height and a given width w will be capable of inducing a latch flip depending on the instant at which the pulse arrives to the latch data node with respect to the clock edge. This time window (W) for the pulse initial instant depends on the pulse height and width (as shown in Fig. 5.16), together with the latch parameters. Such an interval defines the probability within a clock period (T): $P = W/T$. From (5.19) we get:

$$W = w - (t_{hold} + t_{setup}) \quad (5.20)$$

and therefore the probability can be expressed as:

$$P(w) = \frac{w - (t_{hold} + t_{setup})}{T} \quad (5.21)$$

5.7 Probability model

For a fixed V_p , the probability is computed as the integral of $P(w)$ over the width within a clock period and it corresponds to the area of the capture region divided by the total area (T^2). However, this integral can't be easily computed since hold and setup times depend on w as shown in Fig. 5.16 (a). The lower value of each region corresponds to the setup time and it is shown that, except for the full- V_{dd} case, it depends on w . Similarly, the upper bond, related to the hold time, also depends on w since the slope varies with w . Due to the difficulties of computing the capture probability in such way, a model is proposed next.

$$W = a\sqrt{w(w - w_0)} \quad (5.22)$$

Parameters a and w_0 are extracted by a process similar to that explained in Chapter 3. W is obtained from simulations and then fitted to (5.22) using the Marquardt-Levenberg algorithm to obtain the values of both parameters. The dependence of this parameters with V_p is shown in Fig. 5.17.

Parameter w_0 corresponds to the minimum pulse width capable of causing a flip for a given V_p . It increases exponentially as V_p diminishes, which means that for lower V_p values, larger SET widths are required to be captured. Parameter a is a dimensionless parameter that can be interpreted as a correction factor for W due to a non-full V_{dd} pulse. The values of parameters shown in Fig. 5.17 correspond to the values of V_p captured. No capture was observed for $V_p < 0.7V$.

Fig. 5.18 compares the W obtained from simulation to the expression of Eq. (5.22) once a and w_0 are determined. The points correspond to the W values obtained from simulation and the solid lines correspond to model.

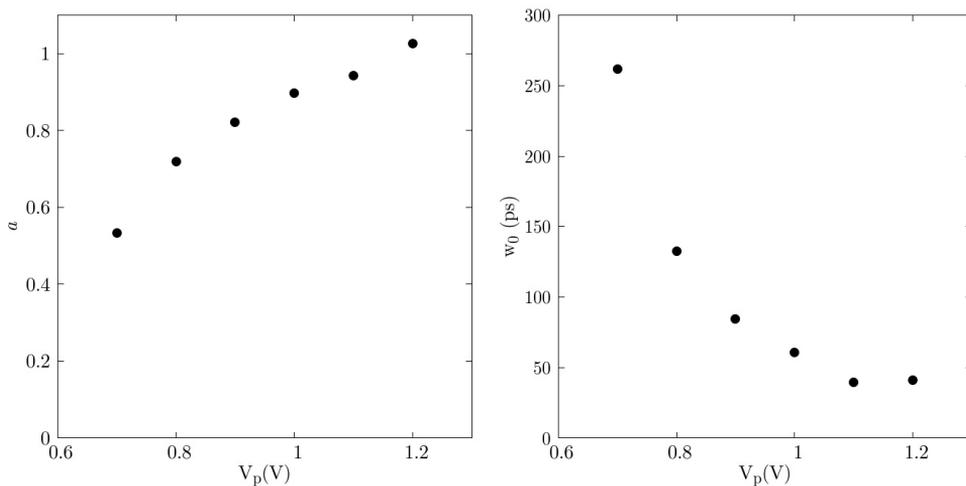


Fig. 5.17. Variation of a and w_0 parameters with V_p .

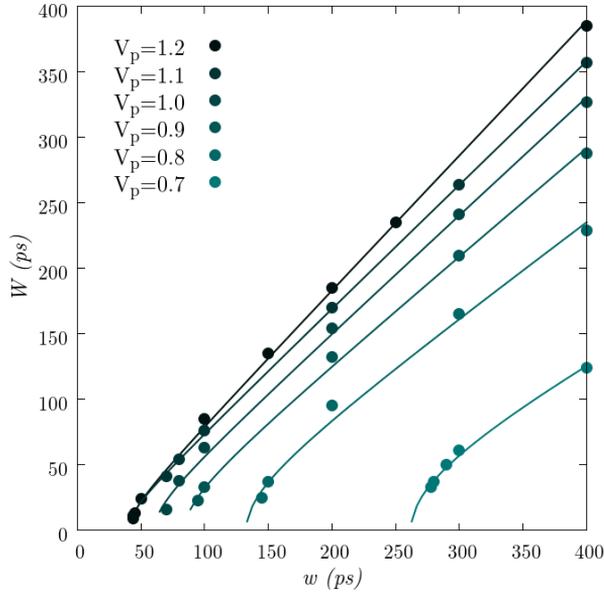


Fig. 5.18. W obtained from simulations and using (4.5).

With the new expression of the latching window, the probability of a pulse with a given width w and height V_p to flip the latch is given by:

$$P(w, V_p) = \frac{a\sqrt{w(w-w_0)}}{T} \quad (5.23)$$

And the probability for all possible w within a clock period is obtained by integrating (4.6) over the pulse width w within a whole clock period:

$$P(V_p) = \frac{a}{8} \frac{w_0^2}{T^2} \ln \left[\frac{w_0}{2(T + \sqrt{T(T-w_0)}) - w_0} \right] + \frac{a}{4} \frac{(2T - w_0)}{T^2} \sqrt{T(T-w_0)} \quad (5.24)$$

5.8 Results

At the beginning of the chapter the LSC was defined and an expression was developed. Extensive simulations were performed to validate this method. Fig. 5.19 compares the LSC obtained analytically to the one obtained through simulation for various latches with different mismatch values. The mismatch values are varied to verify the LSC behavior cell against process variations.

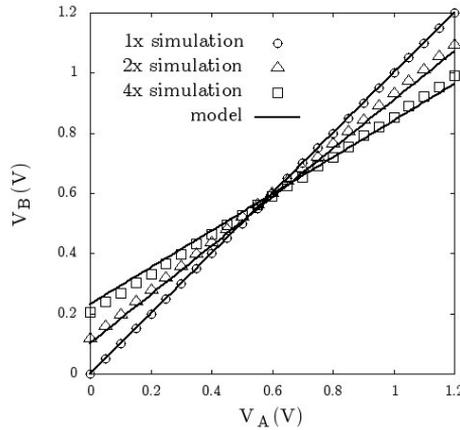


Fig. 5.19. Comparison of simulation to model LSC for different values of mismatch.

When there is no mismatch (1X), from Eq. (5.3) and Eq. (5.4) it follows that $V_{B1} = 0$ and $V_{B2} = V_{dd}$ and in this case the model agrees completely with simulations. In the other cases, as the mismatch increases, the difference between model and simulation also increases since the $I_{NA}=I_{NB}=0$ assumption at points P1 and P2 is not valid.

Regarding the critical charge model, it is compared to the critical charge obtained by simulation for various SRAM cells from a 65-nm CMOS technology. The values of transconductances, threshold voltages and capacitances needed to compute the critical charge using the model Eq. (5.16) and Eq. (5.17) have been first extracted from simulation. Results show a good agreement between model and simulations obtaining

discrepancies lower than 6%. Fig. 5.20 compares the results obtained from simulation to the ones obtained using the model for case 1 ($V_A=0$, $V_B=V_{dd}$) using Eq. (5.16) and case 2 ($V_A=V_{dd}$, $V_B=0$) using Eq. (5.17). As expected Case 1 presents larger values than Case 2 because of the higher strength of n-MOS transistors. Fig. 5.21 shows results for an ideally symmetrical cell 1X-1X, a TT-FF cell (one inverter with TT corner and the other with FF) and TT-SS cell (one inverter with TT corner and the other with SS). Fig. 5.22 shows the results obtained for different V_{dd} values.

In all the examples presented a value of parameter $\tau_\beta = 2$ ps was used. The impact of τ_β variation on Q_{crit} was also checked for τ_β values ranging from 1ps as in [Mes82] to 10ps [Sri96] obtaining that Q_{crit} barely changed for such τ_β range values.

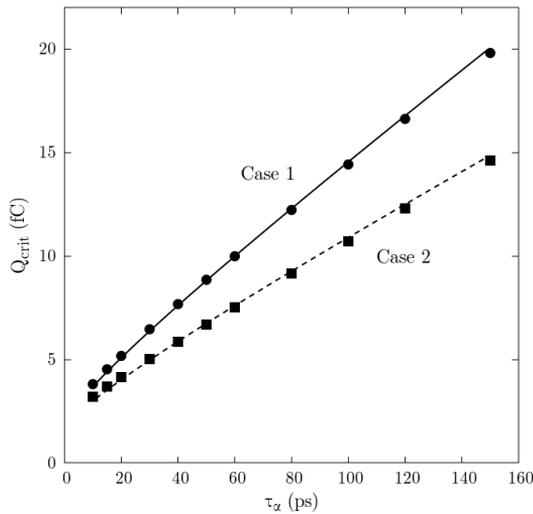


Fig. 5.20. Comparison of Q_{crit} for case 1 ($V_A=0$, $V_B=V_{dd}$) and case 2 ($V_A=V_{dd}$, $V_B=0$).

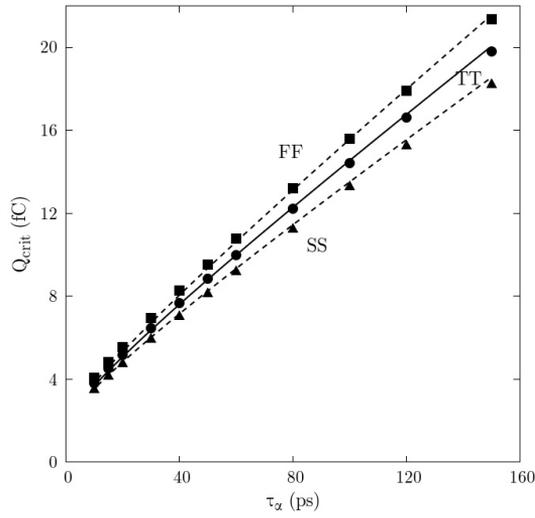


Fig. 5.21. Comparison of Q_{crit} for 1X-1X, TT-FF, TT-SS for case 1.

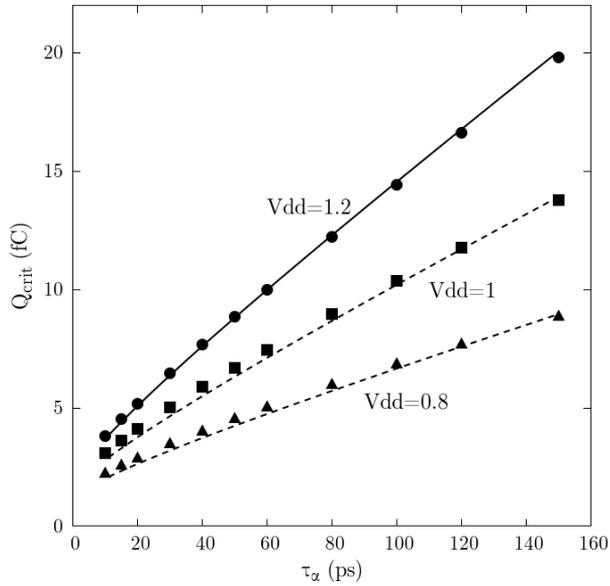


Fig. 5.22. Comparison of Q_{crit} for cells with $V_{dd}=1.2, 1$ and $0.8V$ for case 1.

Regarding the capture probability, extensive simulations were performed to validate the developed model. Pulses were injected at the input of flip flops from a commercial CMOS 65nm technology. The pulses initial time and width were generated randomly and limited to one clock period. For a given SET voltage (V_p) a large amount of SETs was generated (of the order of thousands) and the probability obtained dividing the number of SETs causing a flip by the total number of injected SETs. The value obtained for each V_p is compared to the one obtained using expression (5.24) in Figures 5.23 to 5.26 for four different flip flop types. A quite good accuracy is obtained for all SET heights with a maximum relative error of 5%.

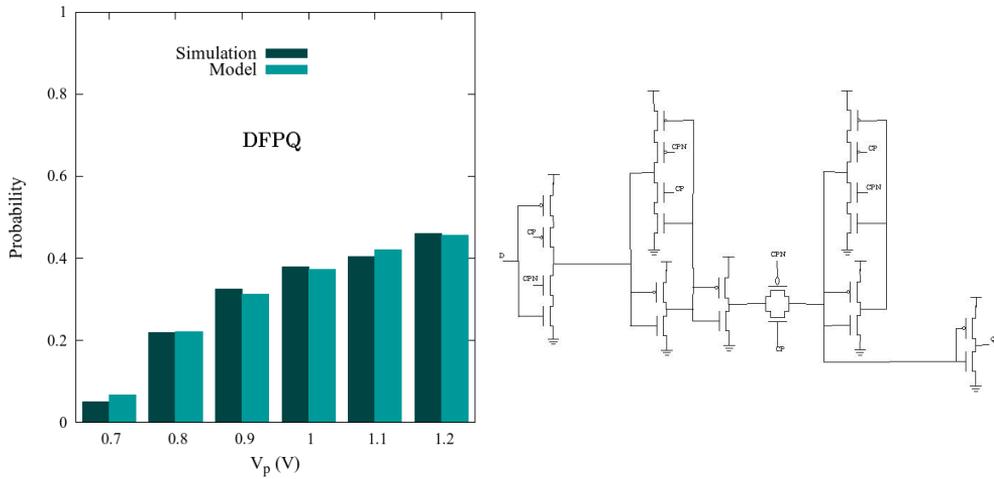


Fig. 5.23. Comparison of probabilities for DFPQ.

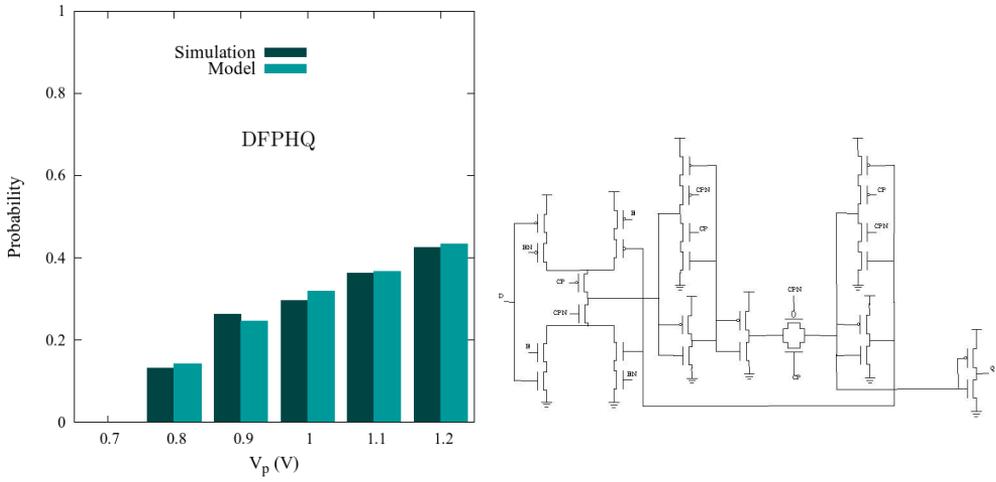


Fig. 5.24. Comparison of probabilities for DFPHQ.

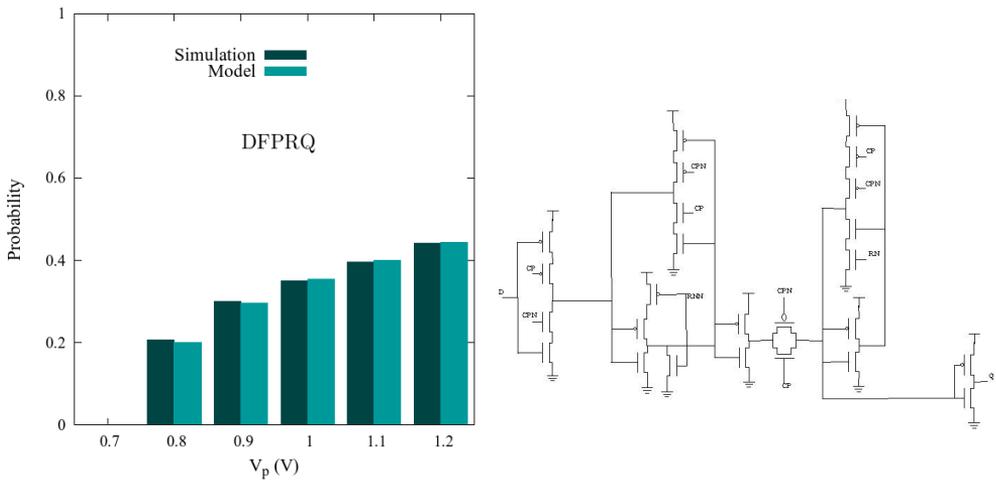


Fig. 5.25. Comparison of probabilities for DFPRQ.

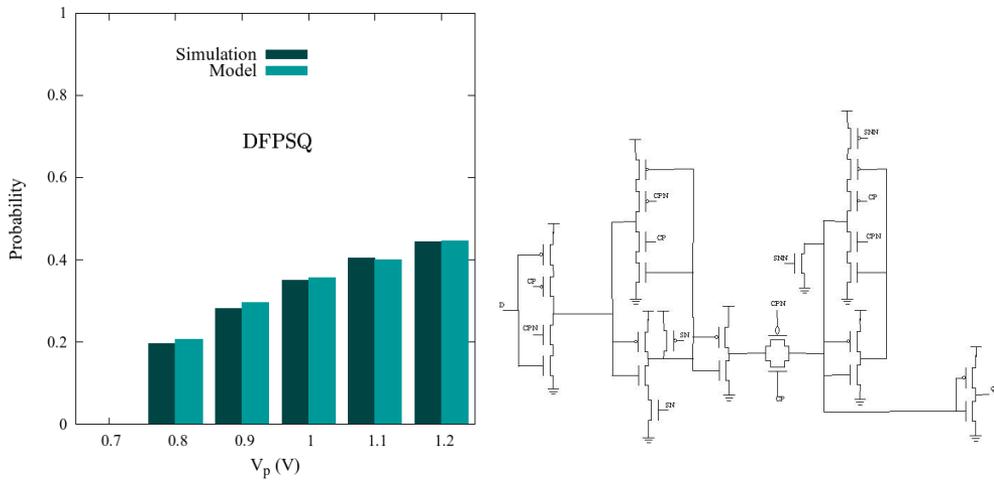


Fig. 5.26. Comparison of probabilities for DFPSQ.

The structure of the four library FFs used is very similar. DFPQ is a typical D flip-flop with a positive edge triggered clock, DFPRQ has an active low reset, and DFPSQ and DFPHQ have an active low set. The difference between these two last FFs is that in DFPSQ the Set signal affects the slave latch, while in DFPHQ the set signal affects the master latch. The figures show that the FF with a higher probability of capture is DFPQ. Not only presents higher probability values but is also capable of capturing pulses with a lower value of V_p .

5.9 Conclusions

The robustness of a latch against radiation depends on both latch and radiation characteristics. In this way, two concepts are revisited in the first part of this chapter: the LSC and the critical charge. The LSC provides information about latch stability and shows the latch stable points. Although it is a measure of robustness itself, when a perturbation is applied the LSC is not valid.

Then, the LSC study is linked to the critical charge given its wide adoption, although it is important to remark that the critical charge depends strongly on the pulse shape considered, and that this pulse must be appropriately chosen to obtain the effects of a specific radiation type.

The results for the critical charge using the model proposed show a very good agreement simulations from a 65nm CMOS commercial technology with an error less than 6%. Such an error is due to the assumptions made to develop the model as $V_B=V_{dd}$ in Eq. (4.10), or the approximation for the time at which V_A is maximum. Model comparisons have been checked for various cases ($V_A=0$, $V_B=V_{dd}$ and $V_A=V_{dd}$, $V_B=0$), process corners and for the supply voltage values.

Finally, the goal of the study of radiation, beyond any metrics, is to obtain the SER (Soft Error Rate). And SER has been already related to the critical charge in previous works [Hei05] through the following expression:

$$SER_j = \kappa \Phi_{rad} \sum_n A_{dif}^n e^{-\frac{Q_{crit}^{n,j}}{Q_s}} \quad (4.17)$$

Being:

κ a scaling parameter.

Φ_{rad} the radiation flux.

A_{dif}^n the sensitive area of node n.

η a measure of the charge collection efficiency.

$Q_{crit}^{n,j}$ the critical charge of node n for a state j.

However, it is also important to remark that critical charge alone is not enough to accurately predict SER values, since not only the electrical cell parameters determine the SER as layout geometry and collection efficiency play a role [Tor14].

The logic depth reduction in combinational circuits increases the relative number of non-full V_{dd} SETs reaching a latch input. This chapter showed that there is an actual significant probability of non-full V_{dd} SETs being captured. As an example, Fig. 4.2 shows a decrease in capture probability of 30% when V_p is 0,9V instead of 1,2V. A relevant result observed using non-full V_{dd} SETs is that hold and setup times depend on the SET width for different V_p values. Therefore, the conventional setup and hold time parameters are not useful in this scenario. The model proposed includes the height parameter providing an approach that requires two parameters to be extracted. The model was applied to four similar library flip-flops. The FF without any set or reset presents the higher probability of capturing an SET. Moreover, contrary to the other tested FFs, pulses with a $V_p = 0.7V$ can be captured by this FF. An explanation for that is that FFs with set or reset contain extra circuitry that actually acts as a filter for SETs with heights below a certain threshold.

Chapter 6

Conclusions and future work

In this thesis we have presented a study of Single-Event Transients, mainly focused on the detailed analysis of the SET propagation and latch SET capture mechanisms. The propagation model developed computes the SET propagation through logic gates using analytical continuous functions. The model, based on the observation of the logic gates response to a pulse is applied at the gate level and does not determine if a given pulse is filtered or not by the gate. For each logic gate, a set of parameters related to gate characteristics are obtained by fitting the results obtained from simulations. This process is done only once per gate for a given technology library. At the gate level, the model has been applied to inverters, NAND and NOR gate, considering the various gate inputs and for various fan-outs, providing a good accuracy at this level. At the circuit level, the model has been verified for a chain of inverters, and some representative paths taken from various ISCAS85 circuits. A SET propagation specific metric, the The

Transition Region (TR), has been defined at the gate level, and has been extrapolated to circuit level analysis. In this sense, the TR has been defined for a path within a circuit, and the specific TR graphs derived for the specific paths within the benchmark circuits, comparing the model results to electrical simulations with good accuracy. It is important to remark that there are situations for which the TR model predicts pulse propagation while the simulation provides no propagation. Despite these cases represent a quite small percentage within the overall TR space, the most important feature of the TR model developed is that it is conservative when compared to electrical simulations, in the sense that all pulses predicted to propagate within the circuit have been confirmed through the simulations. Another important model feature is that the pulse characteristics predictions of model and simulations are compared node by node observing that the model provides a good description of the SET characteristics as it propagates through the circuit.

The model was also checked through experimental data. A pulsed laser was used to generate SETs in a chain of 100 NAND gates. Given the experimental limitations, the model was validated through a combination of experimental data and simulation results. The model provides a prediction of the propagated SET with a mean error of only 7%, that can be considered a very good result given the length of the chain. The obtained data, experimental and from simulation, indicate a validation of the model for different technologies, since the technology used for the experimental data is different from the technology used to develop the model. In addition to the model validation, the measures showed a relation between the SET width and the charge deposited by the laser.

Once the SET propagation model is validated, the analysis of SEU induction through SET capture at latch memory circuits has been approached. The study has been extended to Single-Event Upsets on a latch by means of the Line Switch Contour and the critical charge analysis. The LSC represents a static parameter and represents a first approximation to SEU induction through input signal perturbation capture as it provides a picture of the latch stability, although it is not valid to describe dynamic perturbations. A

more appropriated parameters is the critical charge as it accounts for dynamic situations. A model for this parameter has been developed providing a good accuracy with simulations, although it must be noted memory robustness analysis through the critical charge requires considering its dependence with the current pulse shape.

To summarize conclusions, this work presents a contribution of a simple and efficient model to compute SETs propagation and capture within a circuit. The propagation model can be applied to SETs generated at any circuit node, detecting which nodes are more sensitive and providing valuable information to the design stage. The propagation model has been implemented in an EDA tool that ranks the nodes of the circuit depending on the SET sensitivity as reported in [Bar13].

The Single-Event Transients analysis developed has been focused on the propagation and capture mechanisms. Both analyses are key to determine the circuit nodes being most sensitive to propagate an SET event with a high probability of being captured by a memory element and result in a circuit SEU. However, overall circuit SER estimation requires a generic probability model compound of the SET generation, propagation and capture. An additional step of SET generation analytical model development has not been treated in this work, and represents a strategic research as a subsequent step.

The experimental part of the work devoted to characterize SET generation and propagation of events created by means of a pulsed laser impact has provided quite important guidelines regarding specific rules to follow in the design of test chips. In this sense it has been observed that test chips designed for laser induced SET propagation analysis must include isolated PADs to polarize the circuit well and substrate from the PADs providing the logic circuit polarization. Such a polarization metal lines must be also separated from the supply voltage of the access circuitry. Such rules would provide an intrinsic separation of supply current components that would provide quite valuable information about SET pulse propagation and capture mechanisms.

A third important aspect is the correlation between laser data and specific radiation induced events. Although particle events induced by radioactive sources, either alpha-particle sources or particle generation facilities, have inherent random aspects, it would be possible correlating laser-obtained results to particle-induced experiments.

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